COEN 6511 ASIC DESIGN — Lecturers: A.J. Al-Khalili,
Final April 13, 2002 — Time allowed 3:00 hours
Answer all questions
Calculators are allowed
Use The SPICE parameters and the Design rules provided in all of your calculations when needed
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Question 1 (10 Marks)

a) Layout the smallest inverter according to the design rules given in Appendix 1. Place a contact to each of the drain, source and gate to Metal 1. Identify each layer clearly. Indicate all dimensions on the layout.
b) Determine the effective gate capacitance.
c) Determine the effective drain capacitance.

Question 2 (12 Marks)

A Voltage Transfer Characteristic (VTC) of a CMOS inverter is shown in Fig. 1 Determine:

a) V_{oH}, V_{oL}, V_{IH}, V_{IL} and the Noise Margins of the gate
b) If the Temperature is increased by ΔT, how the shape of the VTC will change ? Explain your answer in terms of βn and βp.
c) Sketch the switching current on the VTC and determine its maximum value in terms of βn and βp.

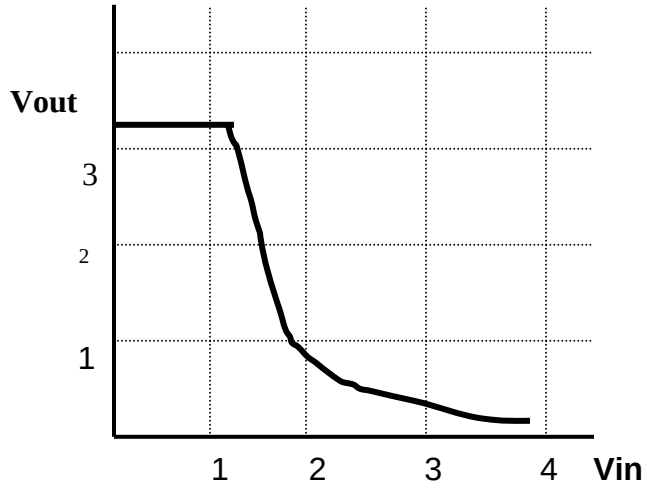

Fig. 1 VTC of the given gate

Question 3 (12 Marks)

a) A vertical cross section of a device is shown in Fig.2. What is this device.
b) Draw the layout of the device, identifying all layers clearly.
c) What would be the conductor width of power and ground wires to a 200 Mhz clock buffer that drives 20 pF load on-chip load to satisfy the metal migration consideration of J_{al}=0.5 mA/μ ? (J_{al} is the current density)
d) What is the ground bounce with the chosen conductor size. ?

The module is 500 μ from both the power and ground path and the supply voltage is 3.3 volts. Rs= 0.1 Ω/□

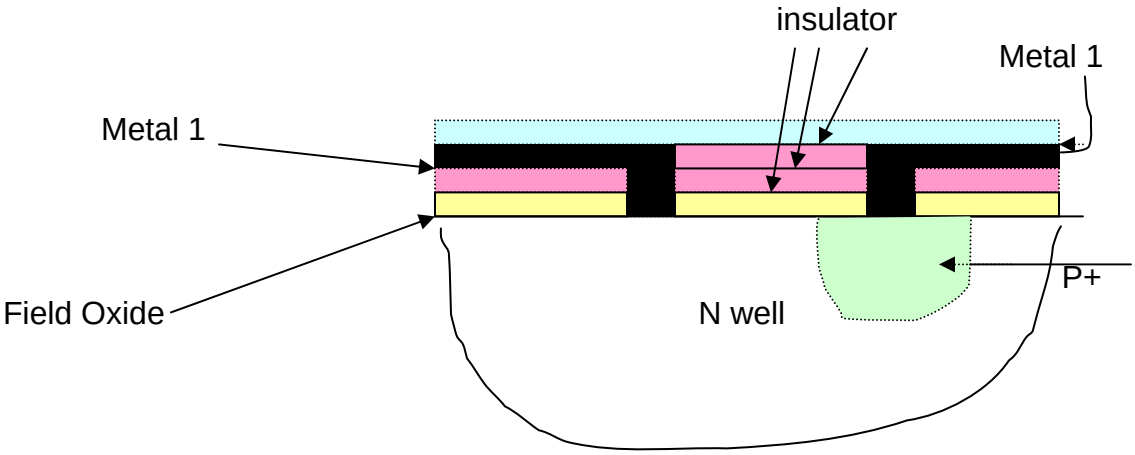

Fig. 2, The structure of Q. 3

Question 4 (12 Marks)

Design a 4-input NAND gate giving all transistor dimensions use mobility ratio, $\mu_r = 3$.

a) Using complementary CMOS logic. Make $t_r = t_f$ (ie rise time= fall time)
b) Pseudo nmos using minimum area as objective function. (delay is not important).
c) Using CASCADE logic.

Question 5 (12 Marks)

Fig. 3 is a conditional pass gate. Sizes of transistors are M1=M2= Wn/Ln=3.6/0.6.
Determine the truth table of the structure.
Assume 0 and 3.3 volts inputs, size M3 transistor for Vol=0.3 volt.
What purpose M3 serves ?

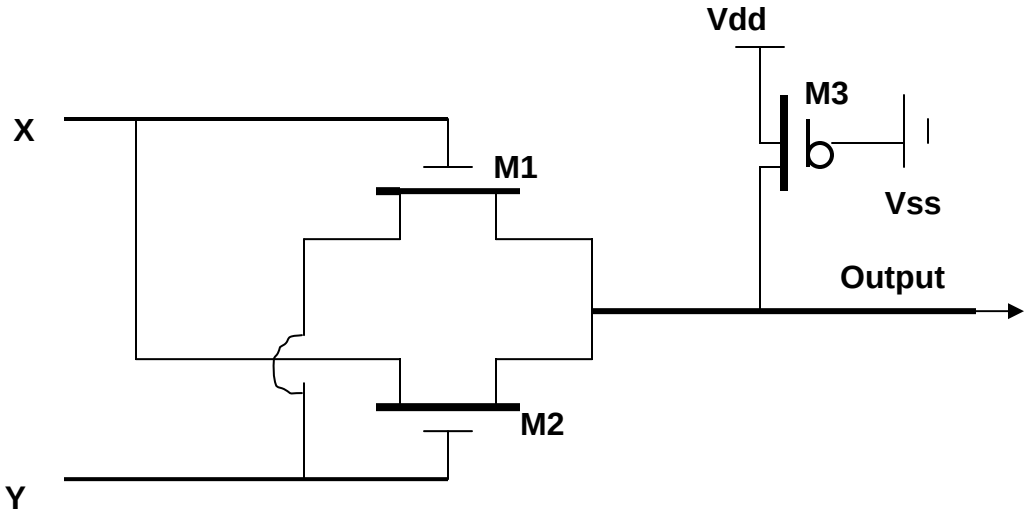

Fig. 3 Controlled passgate of Q5

Question 6 (12 Marks)

a) A dynamic register is shown in Fig. 4. Determine the set up time, the hold time and the propagation delay of the register.
b) Design a 4 input Domino Logic AND gate.
c) Using registers similar to Fig.5 and your designed AND gate design a pipe and determine its speed of operation.

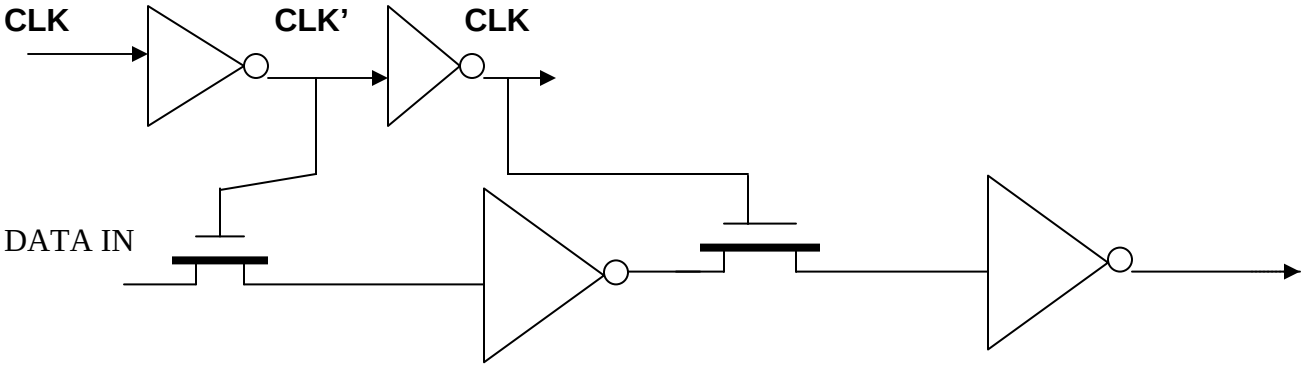

Fig.4 Dynamic Master-Slave Register of Q6

APPENDIX I
Some CMOSIS 5 design Rules (ALL dimensions in micron, μ)

Poly
Min width ……..0.6
Min Spacing ……..0.6
Poly overlap of n/p island over field …….0.45

n- island (diffusion)
min width ……0.6
max length …… 50
spacing ……...0.8
minimum width butting with p-island 0,8

p-island (diffusion)
min width ……. 0.6
max length …… 50
spacing ……. 0.8
minimum spacing butting with n-island…1.0

n-well
min width ……2.2
Active area to n-well spacing …….1.5

Contact 1
Required size……0.8 * 0.8
Min enclosure by p or n island…….0.2
Spacing ……0.6

Metal 1
Min width ……0.6
Min spacing …….0.8
Min overlap of contact 1 ……..0.2

Contact 2
Required size…….0.8 * 0.8
Min spacing……...0.6
Min spacing to contact 1……0.3
Min enclosure by metal 1 ……..0.2

Metal 2
Min width …….0.6
Min spacing ……..0.8
Min overlap of contact 2 ……..0.2

Appendix II
SPICE PARAMETERS

.MODEL CMOSN mos3 type=n

+ PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=1

+ VTO=0.6566 DELTA=6.9100E-01 LD=4.7290E-08 KP=1.9647E-04

+ UO=546.2 THETA=2.6840E-01 RSH=3.5120E+01 GAMMA=0.5976

+ NSUB=1.3920E+17 NFS=5.9090E+11 VMAX=2.0080E+05 ETA=3.7180E-02

+ KAPPA=2.8980E-02 CGDO=3.0515E-10 CGSO=3.0515E-10

+ CGBO=4.0239E-10 CJ=5.62E-04 MJ=0.559 CJSW=5.00E-11

+ MJSW=0.521 PB=0.99

+ XW=4.108E-07

+ CAPMOD=bsim XQC=0.5 XPART=0.5

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 4.1080E-07

.MODEL CMOSP mos3 type=p

+ PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=-1

+ VTO=-0.9213 DELTA=2.8750E-01 LD=3.5070E-08 KP=4.8740E-05

+ UO=135.5 THETA=1.8070E-01 RSH=1.1000E-01 GAMMA=0.4673

+ NSUB=8.5120E+16 NFS=6.5000E+11 VMAX=2.5420E+05 ETA=2.4500E-02

+ KAPPA=7.9580E+00 CGDO=2.3922E-10 CGSO=2.3922E-10

+ CGBO=3.7579E-10 CJ=9.35E-04 MJ=0.468 CJSW=2.89E-10

+ MJSW=0.505 PB=0.99

+ XW=3.622E-07

+ CAPMOD=bsim XQC=0.5 XPART=0.5

* Weff = Wdrawn - Delta_W

* The suggested Delta_W is 3.6220E-07

Some Useful Equations

PMOS:

$|V_{GS}| < |V_{tp}|$ - Cut-off, $\beta = \frac{\mu_{n,p}\varepsilon}{t_{OX}}\left(\frac{W_{n,p}}{L_{n,p}}\right)$

$|V_{GS}| - |V_{tp}| \le |V_{DS}|$ - Saturation

$|I_{DS}| = \frac{1}{2} K'_P \frac{W}{L}\left(|V_{GS}| - |V_{tp}|\right)^2\left(1 + |\lambda||V_{DS}|\right)$

$|V_{GS}| - |V_{tp}| \ge |V_{DS}|$ - Linear

$|I_{DS}| = K'_P \frac{W}{L}\left[\left(|V_{GS}| - |V_{tp}|\right)|V_{DS}| - \frac{1}{2}|V_{DS}|^2\right]$

NMOS:

$V_{GS} < V_{tn}$ - Cut-off

$V_{GS} - V_{tn} \le V_{DS}$ - Saturation

$I_{DS} = \frac{1}{2} K'_n \frac{W}{L}\left(V_{GS} - V_{tn}\right)^2\left(1 + \lambda V_{DS}\right)$

$V_{GS} - V_{tn} \ge V_{DS}$ - Linear

$I_{DS} = K'_n \frac{W}{L}\left[\left(V_{GS} - V_{tn}\right)V_{DS} - \frac{1}{2}V_{DS}^2\right]$

Transistor resistance:

R = $\left(\frac{L}{W}\right)\left(\frac{1}{K\left(V_{GS} - V_t\right)}\right)$: Linear region

R = $\left(\frac{2}{K}\right)\left(\frac{L}{W}\right)\left(\frac{1}{\lambda\left(V_{GS} - V_t\right)^2}\right)$: Saturation

Body effect equation:

$V_{t(n,p)} = V_{to(n,p)} + \gamma\left(\sqrt{|V_{SB}|}\right)$ or expanded below

$V_{t(n,p)} = V_{to(n,p)} + \gamma\left(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f}\right)$

Delay and Power:

$t_r = K\frac{C_L}{\beta_p V_{DD}}$, $t_f = K\frac{C_L}{\beta_n V_{DD}}$, K = 3 4

$t_{dr} = \frac{t_r}{2} = A_P\frac{C_L}{\beta_p}$, $t_{df} = \frac{t_f}{2} = A_n\frac{C_L}{\beta_n}$,

$t_d = \frac{t_{dr} + t_{df}}{2}$, **Power: (1)** Static: $i_p V_{DD}$

(2) Dynamic: (a) switching: $P_d = C_L V_{DD}^2 f_p$

(b) Short circuit: $P_{sc} = \frac{\beta}{12}\left(V_{DD} - 2V_t\right)^3 \frac{t_{r,f}}{t}$

Delay with Input slope:

$t_{dr} = t_{dr\_step} + \frac{t_{i/p\_fall}}{6}\left[1 - 2p\right]$, p = $\frac{V_{tp}}{V_{DD}}$ $\quad t_{df} = t_{df\_step} + \frac{t_{i/p\_rise}}{6}\left[1 - 2n\right]$, n = $\frac{V_{tn}}{V_{DD}}$

Stage ratio Equations: F/O Y = $\frac{C_L}{C_{in}} = S^N$, N = No. of stages, S = delay between stages

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Noise Margins:

$NM_L = V_{ILmax} - V_{OLmax}$

$NMH = V_{OHmin} - V_{Ihmin}$

Values of some useful constants

Boltzman constant	k	$1.38 * 10^{-23}$	J/K
Electron charge	q	$1.6 * 10^{-19}$	C
Thermal voltage	ϕ_T	26	mv (at 300 K)
Electrical permittivity (vacuum)	ε_o	$8.85 * 10^{-14}$	F/cm
Permittivity of Si O2	ε_{ox}	$3.5 * 10^{-13}$	F/cm
Permittivity of Si	ε_{si}	$1.05 * 10^{-12}$	F/cm
Magnetic permeability	μ_o	$12.6 * 10^{-7}$	Wb/Am
Room Temperature	T	300 (=27 ^{0}C)	K

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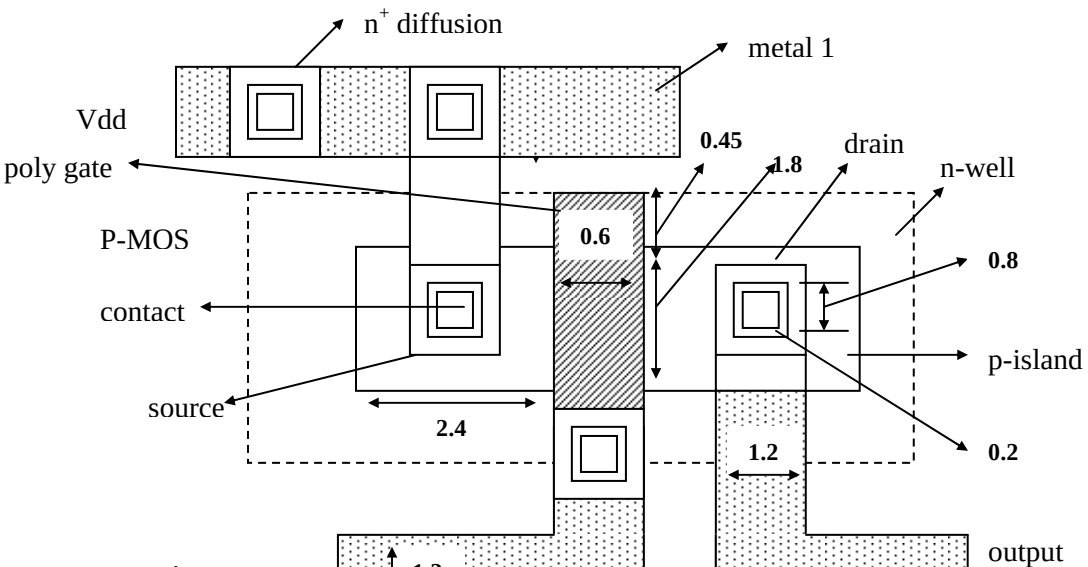
Q1
a)



$C_g = C_{ox} . (W_{eff} . L_{eff})_n + (W_{eff} . L_{eff})_p$

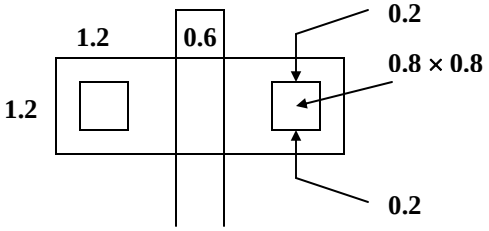
$= C_{ox} \{[(W - \Delta W)_n .(L – 2\ LD)_n] + [(W – 2\ \Delta W)_p . (L – 2\ LD)_p]\}$

$= (\varepsilon_0.\varepsilon_{sio2}/t_{ox}) \times \{[(1.2 – 0.4) \times (0.52 \times 0.047)] + [(1.2 – 2 \text{ x } 0.36).(0.6 – 2 \times 0.35)]\}$

Note the $\Delta W_p \neq \Delta W_n$ and $LD_n \neq LD_p$

$C_{ox} = 3.5 \times 10^{-15}/\mu m^2$ approximately

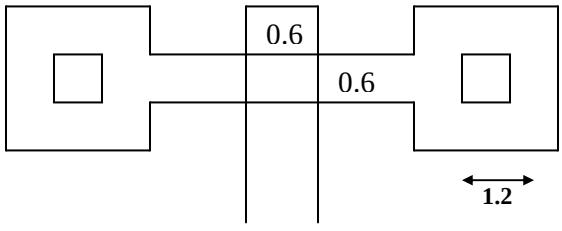
$Cg = 3.5\ fF/\mu m^2 \times \{(0.8 \times 0.5) + (0.84 \times 0.53)\}$



For p & n, Drawn L =0.6 W = 0.8 + 0.2 + 0.2 (Drawn)

Practical minimum size transistor

* Alternatively a value of W = 0.6 μ could have been chosen



Absolute minimum size Drawn transistor

Q1 c. Area of Drain of p or n transistors

$1.2 \times 1.2\ \mu^2 = 1.44\ \mu m^2$ Drawn

Perimeter of Drain pf p or n transistors

$1.2 \times 4 = 4.8\ \mu m$ Drawn

$Cd = Cdn + Cdp$

$= [(C_{JA} \times AD)_n + (C_{JSW} \times PD)_n] + [(C_{JA} \times AD)_p + (C_{JSW} \times PD)_p]$

$=[(5.62 \times 10^{-4} \times 0.1.44 \times 10^{-12}) + (5 \times 10^{-11} \times 34.8 \times 10^{-6}) + (9.35 \times 10^{-4} \times 1.44 \times 10^{-12}) + (2.9 \times 10^{-10} \times 4.8 \times 10^{-6})]$

Note that $C_{JAn} \neq C_{JAp}$ and $C_{JSWn} \neq C_{JSWp}$

Q2 a. $V_{OHmin} = 3.3$ V minimum $NM_L = |V_{ILmax} - V_{OLmax}| = 1.2 - 0.7 = 0.5$

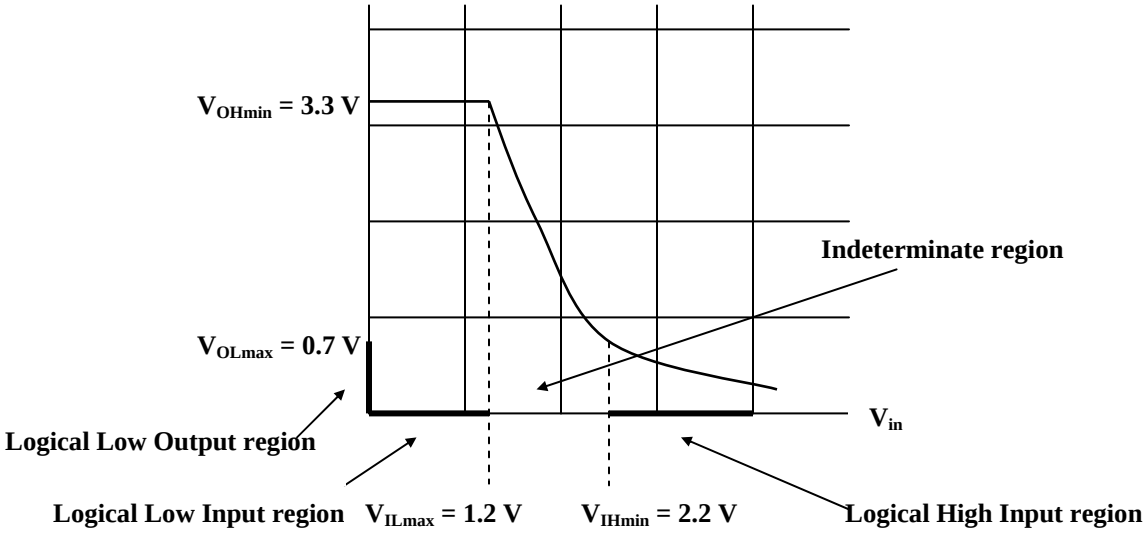
$V_{OLmax} = 3.3$ V maximum $NM_H = |V_{OHmin} - V_{IHmin}| = 3.3 - 2.2 = 1.1$

$V_{IHmin} = 2.1$ V minimum

$V_{ILmax} = 1.2$ V maximum

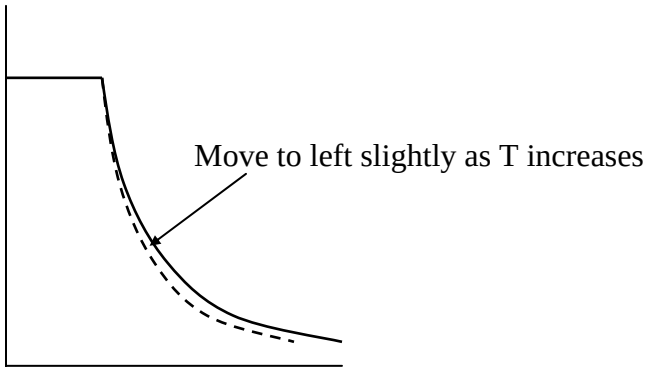
Above values are approximate obtained at 2 points

1) $V_{in} = V_{IH} \cong 1.2$ and $V_{out} = V_{OH} \cong 3.3$ $dV_{out}/dV_{in} = -1$
2) $V_{in} = V_{IH} \cong 2.1$ and $V_{out} = V_{OL} \cong 0.7$ $dV_{out}/dV_{in} = -1$



Q2 b. As temperature increases the carrier mobility decreases. Consequently βn & βp are reduced i.e. $\beta \propto T^{-1.5}$.

However, VTC depends on β_n/β_p therefore is not affected greatly keeping the shape the same. However V_{tn} & V_{tp} decrease as temperature increases, therefore VTC moves slightly to the left as temperature increases.



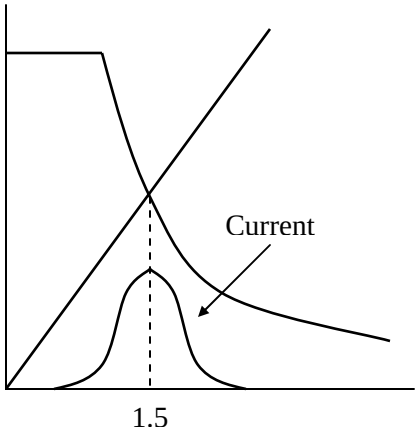
Maximum current occurs at Vinv; Vin = Vo, where both transistors are in saturation region.

$I_n = -I_p = ½ \beta_n (V_{gsn} – V_{tn})^2$

From VTC, $V_{inv} = 1.5$ 0.65

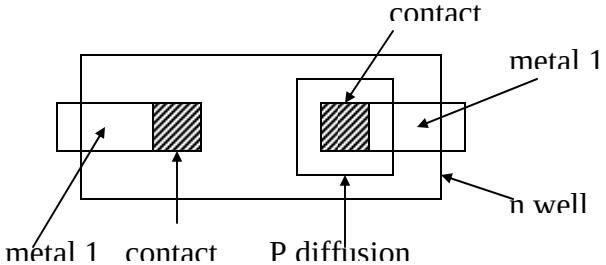
$I_{nmax} = ½ \beta_n(1.65 – V_{tn})^2$

If we use the SPICE parameters given, the $I_{nmax} \cong 0.5 \beta_n$



Q3 a) According to the cross section. It forms a pn junction, hence it should be a pn diode.

Q3 b)



Q3 c) f = 200 MHz, CL = 20 pF $J_{AL} = 0.5$ mA/μm

$P_{dynamic} = C_{TL} . V_{DD} .f$, where $C_{TL} = C_{p\ diffusion} + C_L$

Since we don't know the dimension of the P diffusion and it should be less than C_L

(i.e. $C_{p\ diffusion} << C_L = 20$ pF), We can ignore $C_{p\ diffusion}$ and take $C_{TL} = C_L = 20$ pF

$P_{dynamic} = C_L . V_{DD} .f = 20 \times 10^{-12} \times 3.3^2 \times 200 \times 10^6$

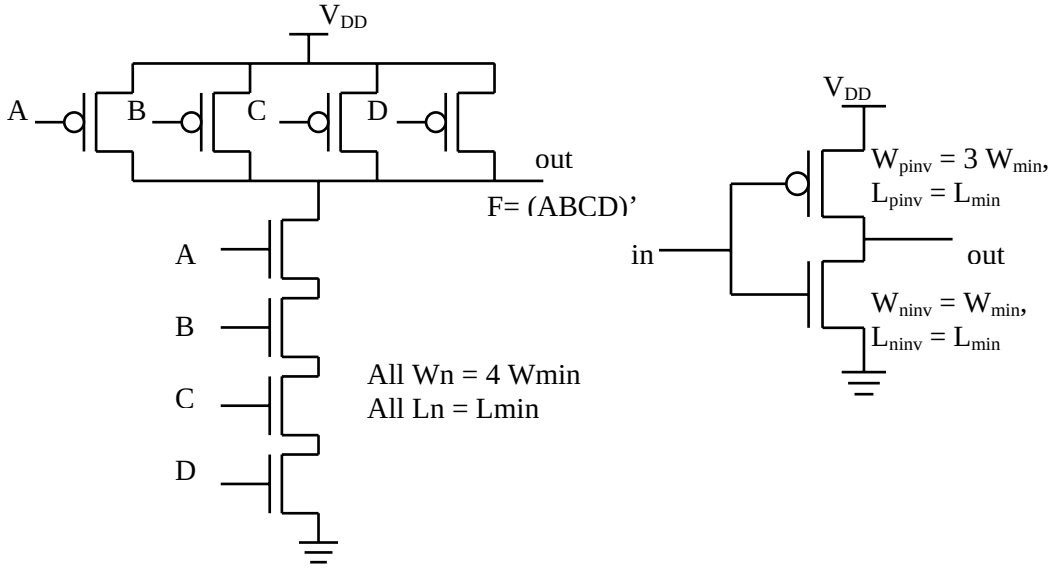
$= 0.04356$ W

$I_{dynamic} = P_{dynamic}/V_{supply} = 0.04356$ W/ 3.3V = 0.0132 A

The width of bus (minimum) = $I_{dynamic}/J_{AL}$ = 0.0132 A/0.5 mA/μ = 26.4 μm
To be more conservative, take the width of bus = 30 μm

Q3 d) The ground bounce is given by ΔV = I.R, where I is the bus current and R is the bus resistance.
I = Idynamic = 0,0132 A
$R = R0 \times L_{bus} / W_{bus}$ = 0.1 Ω × 500 μ /30 μ = 1.67 Ω
ΔV = I.R = 0.0132 A × 1.67 Ω = 0.022 V
Thus, the ground bounce is 0.022 V.

Q4 a) CMOS logic: F = (ABCD)'

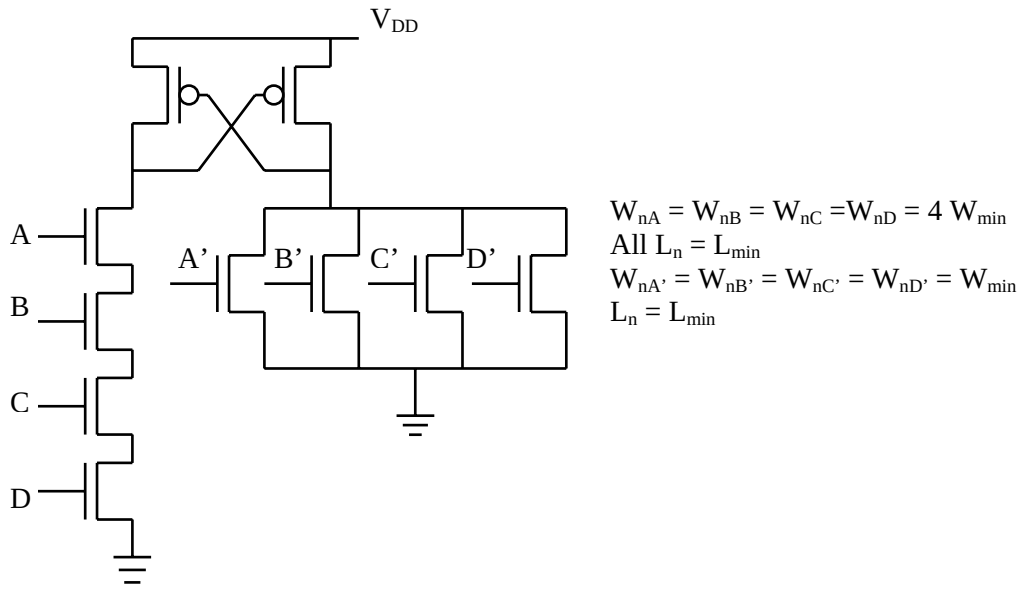


Consider an equivalent inverter first,
$\mu_r = 3$. In order to make $t_r = t_f$, $W_{pinv} = \mu_r W_{ninv}$
Take $W_{ninv} = W_{min}$, then $W_{pinv} = 3 W_{min}$
All length $L_{inv} = L_{min}$
Then size the 4-input NAND gate and get the dimensions as following:
$W_p = 3 W_{min}$, $L_p = L_{min}$, according to the worst case when only one PMOS is "on" to give the logic high output
$W_n = 4 W_{min}$, $L_n = L_{min}$ because 4 NMOS need to simultaneously be "on" to give the logic low output.

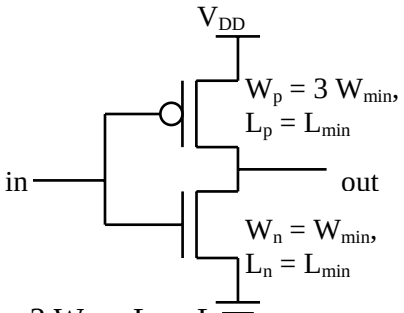
Q4. b) This is a pseudo nmos. A ratioed logic. We have been told that area is important and delay is not important at all. Therefore we aim to minimize area by taking smallest dimension. For the pseudo nmos to work $V_{OL} < V_{tn}$. In this process $V_{tn} \cong$ 0.65 Therefore selecting V_{OL} = 0.5 volt would satisfy our criteria.
Select $W_n = W_{min}$ for all transistors.
then $W_n = W_{min}$ /4 due to series connection
W_p effective = W_{min} /4 due to $\mu_r = 4$
The only parameter that can change without affecting area is L_p.

Now for the pseudo nmos to work properly, approximately we say
$[R_n/(R_n + R_p)] \times 3.3 = 0.5$ volts
or $\{(L_{min}/W_{min}/4)/[(L_{min}/W_{min}/4) + (L_p/W_{min}/4)]\} \times 3.3 = 0.5$ volt
$[Lmin/(Lmin + Lp)] \times 3.3 = 0.5$
or $L_p = 5.6\ L_{min}$ approximately

Q4. c) CASCODE logic

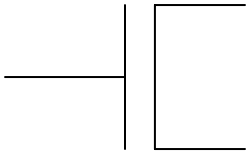


If we want tr = tf, that is sizing the gate according to the equivalent inverter below:



Then all $W_p = 3\ W_{min}$, $L_p = L_{min}$
and $W_{nA} = W_{nB} = W_{nC} = W_{nD} = 4\ W_{min}$
$W_{nA'} = W_{nB'} = W_{nC'} = W_{nD'} = W_{min}$
All lengths of nmoc are L_{min}
If we want minimum area, then we can size all the transistors with
$W_n = W_p = W_{min}$ & $L_n = L_p = L_{min}$
But in this case the delay will be larger.

Q5. a) Truth table



X	Y	output
0	0	1
0	1	0
1	0	0
1	1	1

Q5. b) Assume X = 0, Y = 1 (3.3 V), then M1 "off", M2 is "on" that makes the output be logic low, and the current acts as pseudo nmos inverter. In this case, M2 is saturated and M2 is linear, according to the conclusion of previous question for an pseudo nmos inverter when $V_{out} = V_{OL}$

$W_p/W_n = \{2K_n'[(V_{DD} - V_{tn}) \times V_{OL} - V_{OL}^2/2]\}/K_p'.(V_{DD} - |V_{tp}|)^2$

When $V_{OL} = 0.3$ V,

$W_p/W_n = 2\times 3 \times [(3.3\text{-}0.6566)\times 0.3 - 0.3^2/2]/(3.3\text{-}0.51213)^2 \cong 0.8$

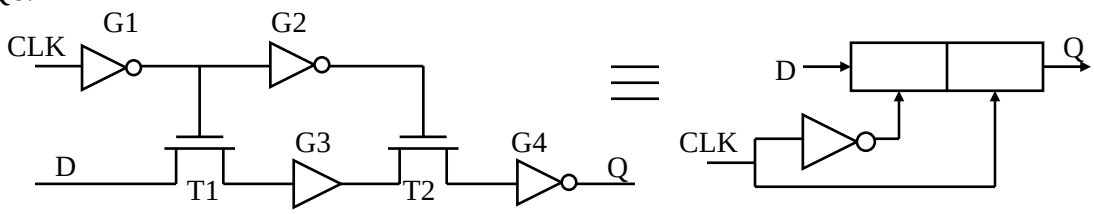
since $W_n/L_n = 3.6/0.6$, $W_p/L_p = 0.8\ W_n/L_n = 2.88/0.6$

Thus for M3, in order to get $V_{OL} = 0.3$ V, $W_{M3}/L_{M3} = 2.88/0.6$

Q5. c) The purpose of M3 is that it helps to confirm the output logic "1". If M3 does not exist, then when X =0 and Y = 0 the output is not known. Also it acts as a current source. In the same time, nmos pass transistor is not good for transmission of "1". V_{OH} will V_{DD}-V_{tn} without M3.

When X Y change for 1→0 M3 keeps output high by compensating the leakage current. Side effects $V_{OL} \neq 0$ but 0.3 volt.

Q6.

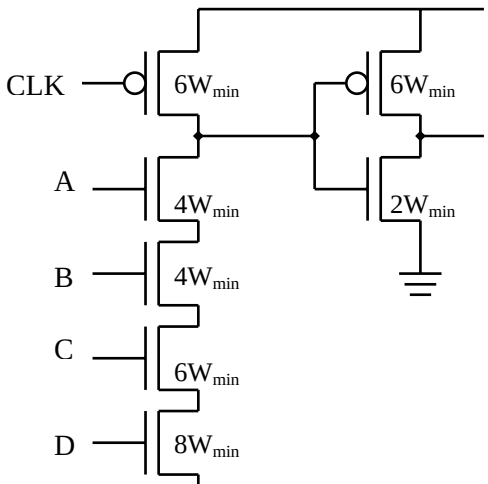


a) $t_{\_set\ up} = T1 + G3 \cong G3$

$t_{\_hold} = G1 + G2$ also G1 above is acceptable

$t_p = t_{\_setup} + t_{\_hold} + G4$

Q6. b)



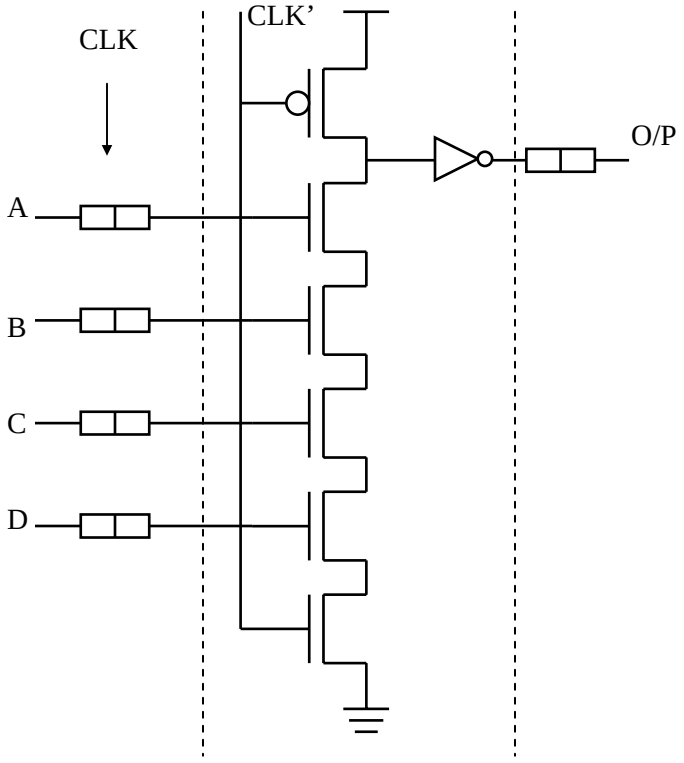
Sizing series transistors approximately to obtain 2 W_{min} inverter with $\mu_r = 3$

$t_{precharge} = 2.2\ T_p = 2.2\ R_pC_0$

$t_{AND\_series} = 2.2\ [R_AC_0 + R_BC_B + R_CC_C + R_DC_D + R_{CLK}C_{CLK}]$

$t_{AND} = t_{precharge} + t_{AND\_series}$

Q6. c) Evaluation sampling CLK (during CLK')



Data is transferred → to this side during precharge of AND

max frequency = $1/\tau_{min}$

$\tau_{min} = t_{setup\_reg} + t_{p\_reg} + [t_{AND\_series} + t_{precharge}]$

min frequency = 1/dt, where dt is the time for V_0 to reduce to V_{IH}

$C_0\ dv/dt = I_{leakage}$

Qr $dt = C_0dv/I_{leakage}$

$f_{min} = I_{leakage}/C_0\ (V_{dd} - V_{IH})$

```
*Canadian Microelectronicd Corporation
*CMOSIS5 Design Kit V2.1 for Cadence Analog Artist
*Run=n5bo
*date=1-Feb-1996

*MOS3 models for use in spectre

#ifdef n5bo
```

```
.MODEL CMOSN mos3 type=n
+PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=1
+VTO=0.6566 DELTA=6.9100E-01 LD=4.7290E-08 KP=1.9647E –04
+UO=546.2 THETA=2.6840E-01 RSH=3.5120E+01 GAMMA=0.5976
+NSUB=1.3920E+17 NFS=5.9090E+11 VMAX=2.0080E+05 ETA=3.7180E-02
+KAPPA=2.8980E-02 CGDO=3.0515E-10 CGSO=3.0515E-10
+CGBO=4.0239E-10 CJ=5.62E-04 MJ=0.559 CJSW=5.00E-11
+MJSW=0.521 PB=0.99
+XW=4.108E-07
+CAPMOD=bsim XQC=0.5 XPART=0.5
*Weff = Wdrawn - Delta_W
*The suggested Delta_W is 4.1080E-07

.MODEL CMOSP mos3 type=p
+PHI=0.700000 TOX=9.6000E-09 XJ=0.200000U TPG=-1
+VTO=-0.9213 DELTA=2.8750E-01 LD=3.5070E-08 KP=4.8740E-5
+UO=135.5 THETA=1.8070E-01 RSH=1.1000E-01 GAMMA=0.4673
+NSUB=8.5120E+16 NFS=6.5000E+11 VMAX=2.5420E+05 ETA=2.4500E-02
+KAPPA=7.9580E+00 CGDO=2.3933E-10 CGSO=2.3922E-10
+CGBO=3.7579E-10 CJ=9.35E-04 MJ=0.468 CJSW=2.89E-10
MJSW=0.505 PB=0.99
+XW=3.622E-07
+CAPMOD=bsim XQC=0.5 XPART=0.5
*Weff = Wdrawn –Delta_W
*The suggested Delta_W is 3.220E-07
#endif
```

APPENDIX I

Some CMOSIS 5 design Rules (ALL dimensions in micron, μ)

Poly

Min width ……0.6
Min Spacing ……0.6
Poly overlap of n/p island over field ……...0.45

n-island (diffusion)
Min width …….0.6
Max length ……50
Spacing …….0.8
Minimum spacing butting with p-island ……..1.0

n-well
Min width …….2.2
Active area to n-well spacing ……...1.5

Contact 1
Required size ……0.8 × 0.8
Min enclosure by p or n island …….0.2
Spacing …….0.6

Metal 1
Min width …….0.6
Min spacing ……..0.8
Min overlap of contact 1 ……..0.2

Contact 2
Required size ……0.8 × 0.8
Min spacing ……..0.6
Min spacing to contact 1 ……..0.3
Min enclosure by metal 1 …….0.2

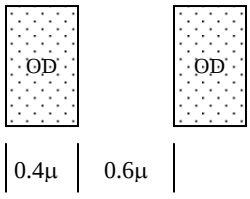
Metal 2
Min width ……..0.6
Min spacing ……...0.8
Min overlap of contact 2 ……0.2

Simplified Cmosp35 Design Rules

Thin Oxide Mask (OD) — as a Active or Diffusion Mask

OD.W.1 Min diffusion width = 0.4µ

OD.S.1 Spacing between diffusion areas = 0.6µ



Nwell Mask (NW)

NW.W.1 Min Nwell width = 1.7μ

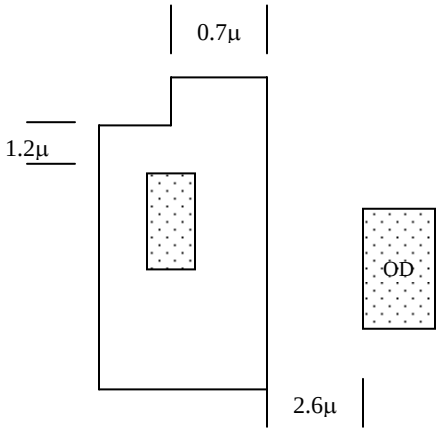
OD.C.4 Min overlap over diffusion = 1.2μ

OD.C.3 Min spacing to external diffusion = 2.6μ

(Not Shown)

NW.S.1 Min Nwell spacing (different potential) = 3μ

NW.S.2 Min Nwell spacing (same potential) = 1μ



Polysilicon Mask (PO)

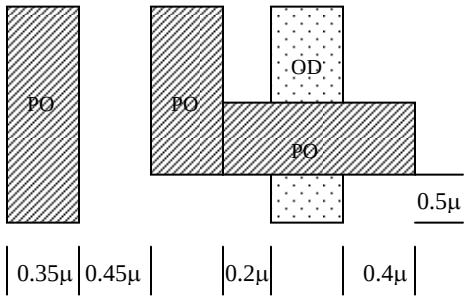
PO.Q.1 Min poly width = 0.35μ

PO.S.1 Min poly spacing = 0.45μ

PO.O.1 Min poly gate extension = 0.4μ

PO.C.1 Min poly to diffusion spacing = 0.2μ

PO.C.2 Min source/drain extension = 0.5μ



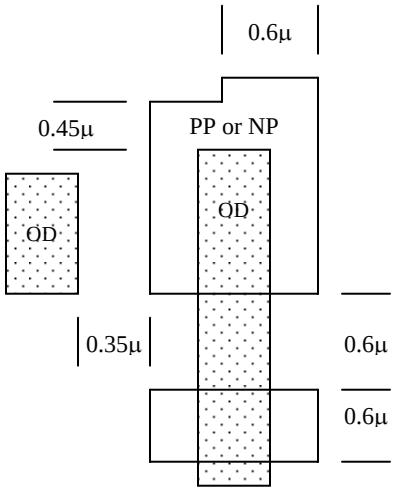
P-plus Mask (PP) or N-plus Mask (NP)

PP/NP.O.1 Min overlap over diffusion = 0.45μ

PP/NP.W.1 Min width of PP or NP =0.6μ

PP/NP.S.1 Min spacing between PP and/or NP = 0.6μ

PP/NP.C.1 Min spacing to unrelated diffusion = 0.35μ

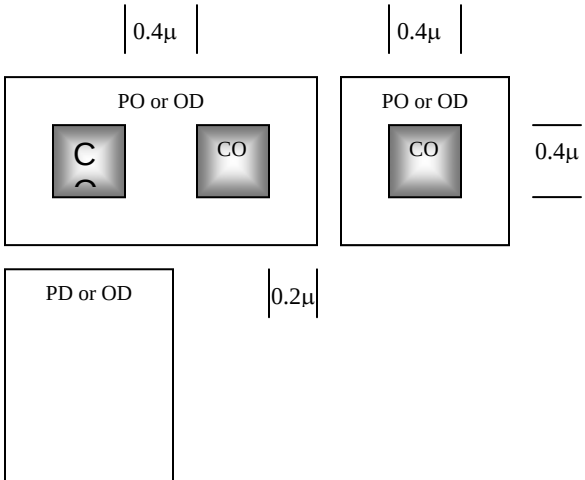


Contact Mask (CO)

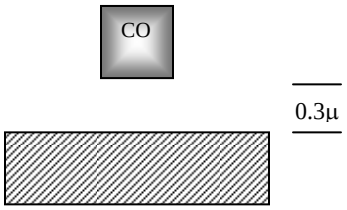
CO.W.1 Min/Max contact size = 0.4μ × 0.4μ

CO.S.1 Min contact spacing = 0.4μ

CO.E.2 Min overlap poly or diffusion = 0.2μ



CO.C.1 Min spacing to gate poly = 0.3μ

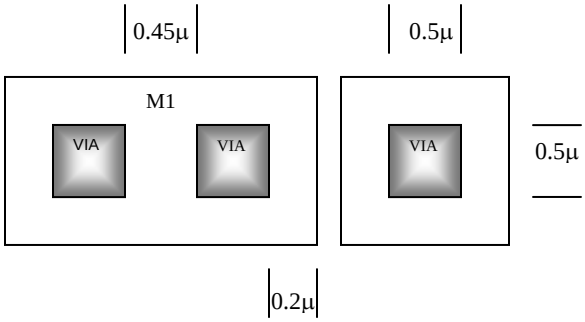


Via 1 Mask (VIAI)

VIA1.W.1 Min/Max contact size = 0.5μ × 0.5μ

VIA1.S.1 Min contact spacing = 0.45μ

VIA1.E.1 Min M1 extension over via = 0.2μ

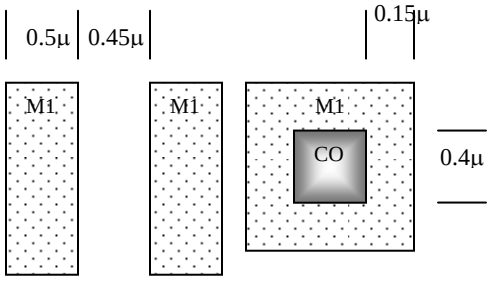


Metal 1 Mask (M1)

M1.W.1 Min metal width = 0.5μ

M1.S.1 Min metal spacing = 0.45μ

M1.E.1 Min metal extension over contact = 0.15μ

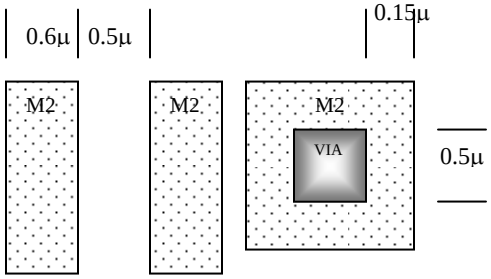


Metal 2 Mask (M2)

M2.W.1 Min metal width = 0.6μ

M2.S.1 Min metal spacing = 0.5μ

M2.E.1 Min metal extension over contact = 0.15μ



Poly2 Mask (PO2) — Used for Poly1/poly2 capacitors

PO2.W.1 Min width of PO2 for cap to plate = 0.8μ

PO2.E.1 Min extension of PO past PO2 = 1.0μ

PO2.E.2 Min extension of PO2 past CO = 0.6μ

PO2.C.1 Min clearance to CO on PO from PO2 = 1.2μ