P R O J E C T R E P O R T

A Report on
Design of 4_bit Manchester Adder

Professor	Asim Al-Khalili
Students	YangPing Zhao ID: 4580664
Students	ChangHua Chang ID: 4551664

Table of Contents

ABSTRACT

Addition is the most commonly arithmetic operation. Often it is also the speed-limited element. Therefore, careful optimization of the adder as of utmost important. This project for the course COEN 6511 is to introduce the ASIC design issues in respect of optimization. We are required to design a 4_bit adder, aiming to grasp the techniques of ASIC design. Here we select a static 4-Bit Manchester Adder as the design target to illustrate the design issues because of its high-speed and is widely usage in application. In designing we select the Speed (propagation delay) as well as Area (A) as performance index for optimization. The details of designing a 4-bit static Manchester Adder are given in this report. It involves the circuit design, schematic simulation, layout, etc. We first discuss the characteristics the main components used for building up Manchester Adder, such as C-chain circuit and XNOR circuit (use Mirror Circuit) design, then scheme 1-bit Manchester Adder, make the simulations to verify their validate. Then we configure the 4-bit Adder. In environment of CMOSIS5 and minimum drawing layout size is 0.6μ. Also we will summarize the final performance indexes.

1. Requirement for the 4-Bit Adder Project

1.1 Description of the Project

The goal of this project is to design a 4-bit adder. Input two 4-bit numbers A &B, output is the 4-bit sum and a carry. Any adder form, CRA, CLA, etc., and any logic form such as static, dynamic, or any variation of these families cad be selected.

1.2 Performance Measures

Area (A), Time (T), Power (P), or AT^2 can be selected as circuit performance. Initially specification and optimization of the design goal are needed.
Noise Margins should be at least be the 10% of the voltage swing. Make sure to validate this in the design.
Rise and Fall Times: No more then 500 *psec* for the edge of all input signals and clocks, as well as output signals (10% to 90%).

1.3 Simulation

Logic simulation, circuit simulation and re-simulation of circuit after circuit extraction are needed.

1.4 Layout

layout two gates of the design fully.
Perform DRC.
Extract the design and simulate again,
Characterize the gates, give the complete specification for the circuit.
Place and rout the complete chip, include all I/O drivers and PADs.

Any library cells from CANDENCE are allowed to use after the two gates' layout. Perform DRC on final design, extract it and simulate again to obtain performance measures.

1.5 Report

A complete report in the form of given style is needed.

2. Circuit for 4-Bit Manchester Adder

Objective: Design a high speed of 4-bit adder.

2.1. Circuit Configuration

The targeted adder circuit configuration is shown in figure 1. It consists of three blocks---PG, C-chain, and SUM.

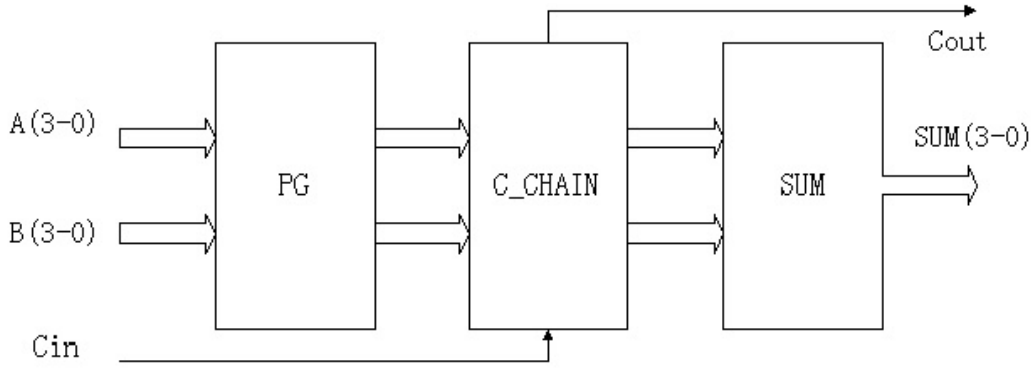

Figure 1. Adder Circuit Configuration

2.1.1 PG Block

In the PG block, P_i *(propagation)* and G_i *(generation)* can be obtained by the functions below:

$$P_i = A_i \oplus B_i$$
$$G_i = A_i \bullet B_i$$

2.1.2 C-chain Circuit Characteristics and Simulation

The C-Chain is constructed in Figure 2. We design a C_chain circuit with a voltage from Vdd to Vss, which is a little bit different from the circuit in textbook. This circuit function is ,
when $P = 1$, $G = 0$, $G' = 1$, Transistor *M2* and *M4* are off, *M3* is on, the *TG* is conducting, and C_{in} is transmitted to the output $C_{out} = C_{in}$.
when $P = 0$, $P' = 1$, the *TG* is cut off, *M4* is on $C_{out} = G$.

The schematic simulation and the final simulation after the layout extraction are shown in Figure 3 and Figure 4. The layout of c-chain is shown in Appendix 1.

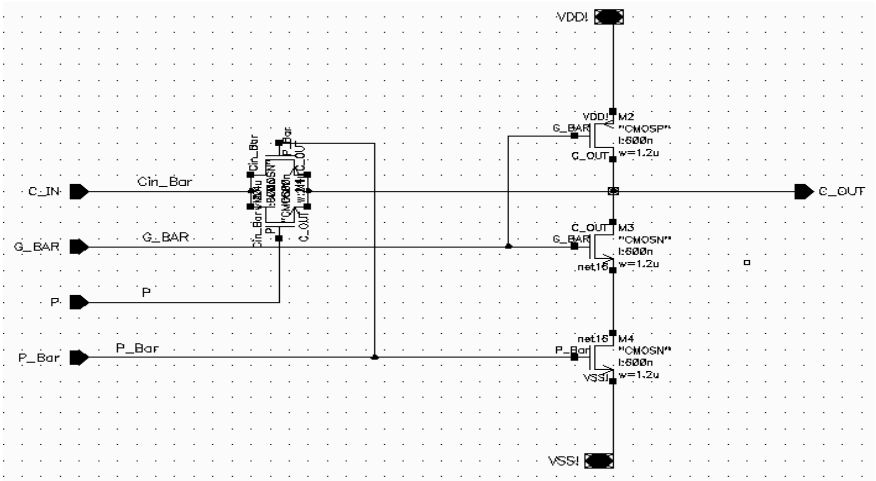

Figure 2. Circuit of C-Chain

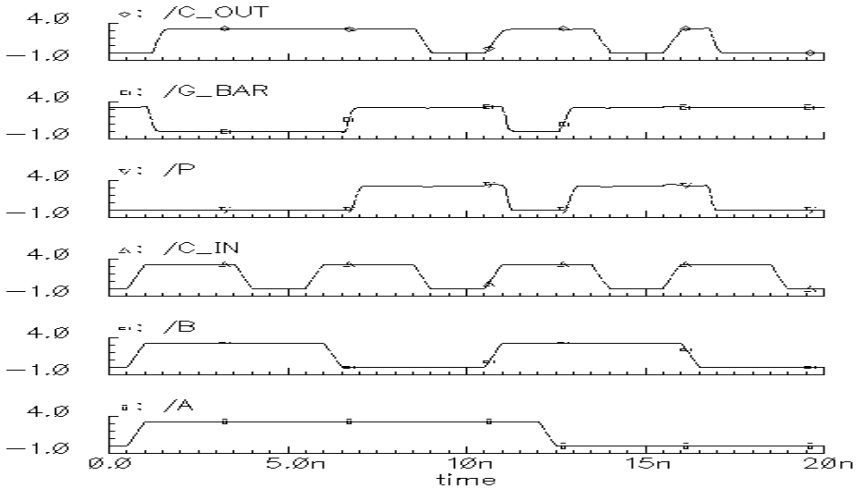

Figure 3. Simulation of C-Chain Schematic

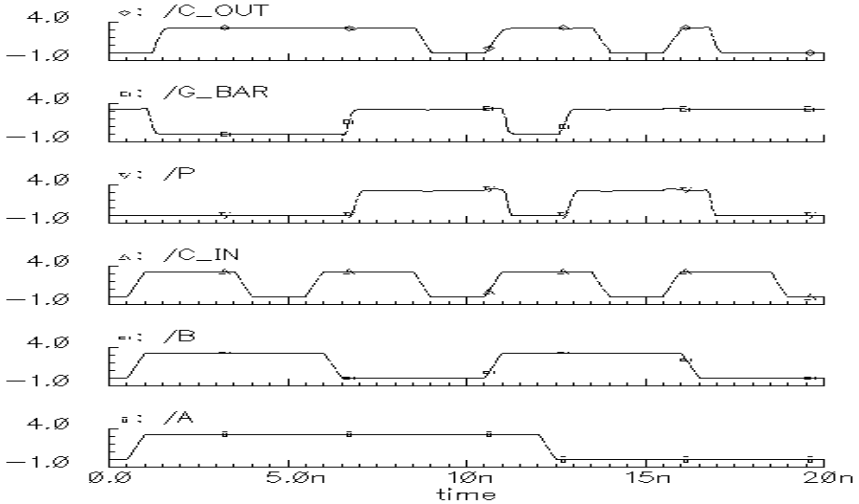

Figure 4. Simulation of C-Chain After Layout Extraction

2.1.2 SUM Block

The function of Sum is $S_i = P_i + C_{i-1}$. Its implementation is very simple, so the simulation result is omitted here.

In above two simulations, we can see that their functions are the same and the waveforms are consistent.

2. 2 XNOR Circuit Description and simulation

Because of request for faster and/or more compact circuit structures, here we select the *mirror circuit* to implement XNOR, in which the N-MOS and P-MOS arrays have the exactly the same structure and have the same characteristics as series-parallel logic formation and easy to layout. Figure 5 shows the XNOR mirror circuit. This circuit is of interest because it has shorter switching time. The time constant in Figure 5 is given by:

$$\tau_p = R_p C_2 + 2R_p C_{out}$$

Figure 5. XNOR Mirror Circuit

τ_p is less than its corresponding series-parallel logic. In addition, the layout is simpler because of the symmetry of the four branches. The mirror circuit we design is illustrated in Figure 6.

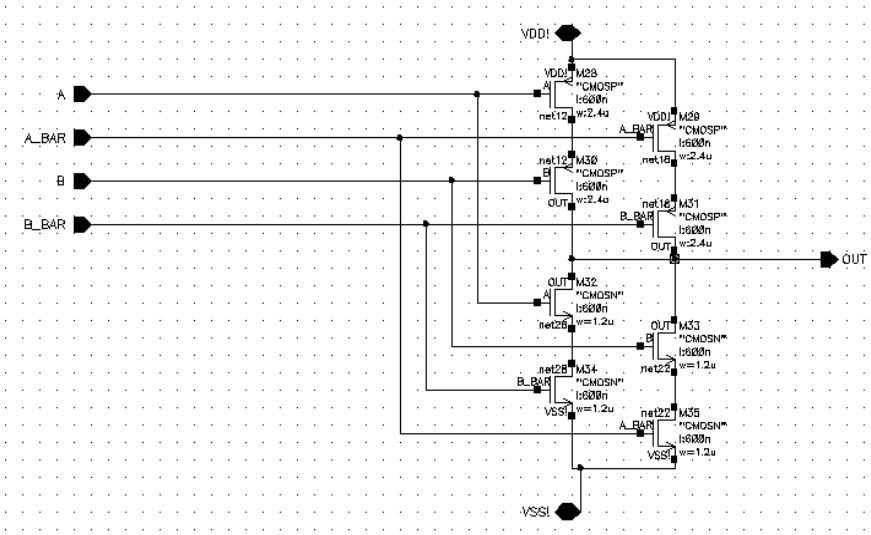

Figure 6: XNOR Circuit

Appendix 2 shows the layout of XNOR and the schematic simulation as well as the simulation after the layout extraction is shown in Figure 7 and Figure 8.

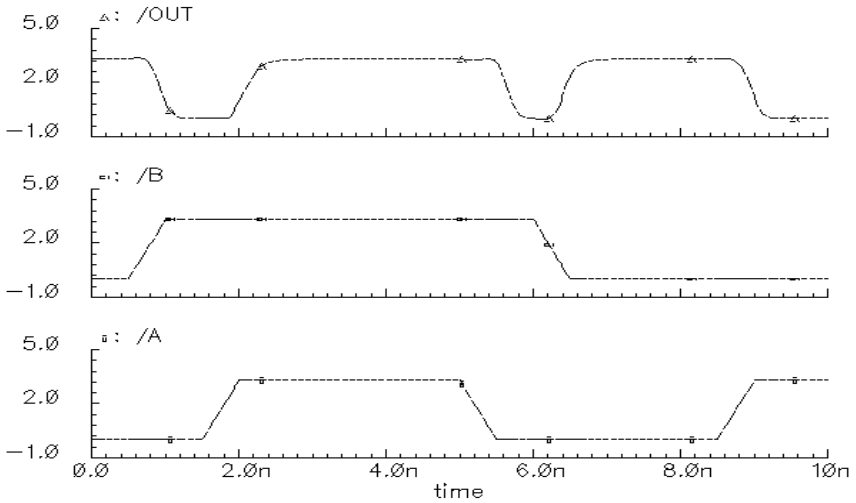

Figure 7. XNOR schematic Simulation

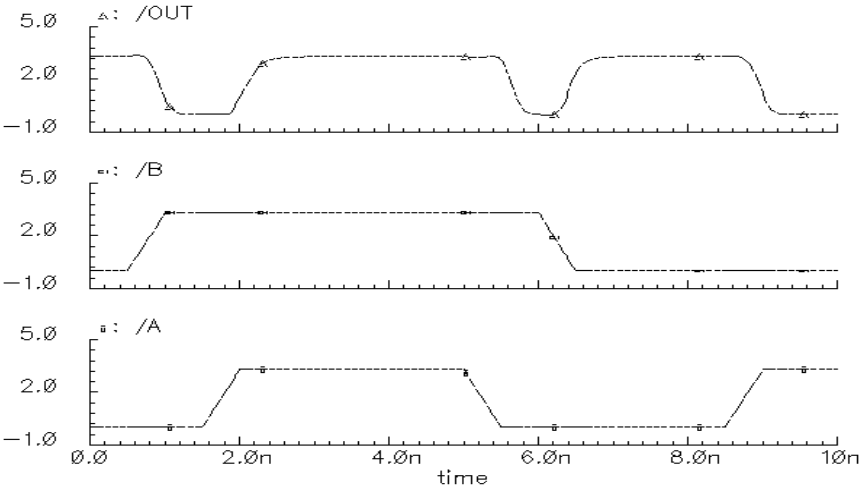

Figure 8. Simulation after Extraction of layout

3. 1-Bit Adder Configuration and Testing

3. 1 Structure and Simulation of 1Bit Adder

In design, we use C-chain, XNOR, Inverter, and NAND gates to build up 1-bit adder. The 4-bit adder is built by assembling four 1-bit adder. The characteristics of building bocks are verified first.

Figure 9 shows the 1-bit-adder circuit. Its simulation is shown in Figure 10. The logic is correct. The layout is shown in Appendix 4. Layout simulation is shown in Figure 11, the result is almost the same as schematic simulation.

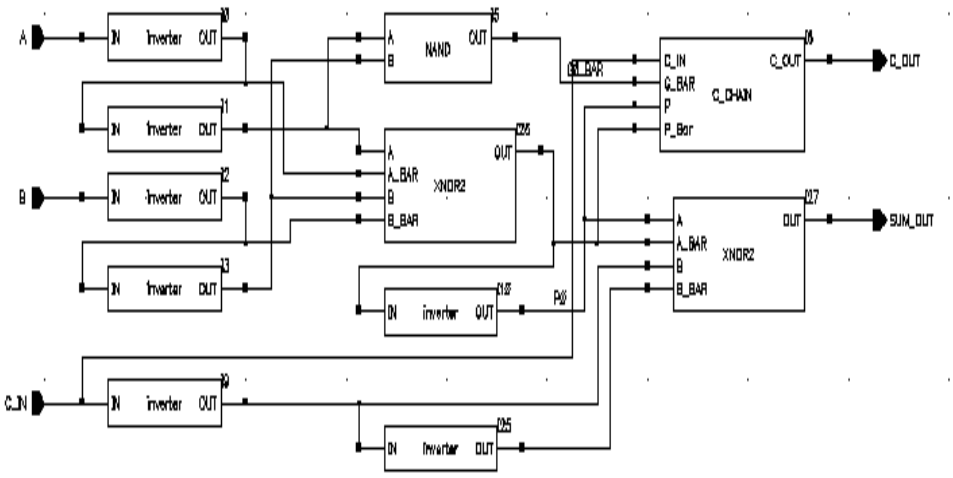

Figure 9: Circuit of 1-Bit Adder Schematic

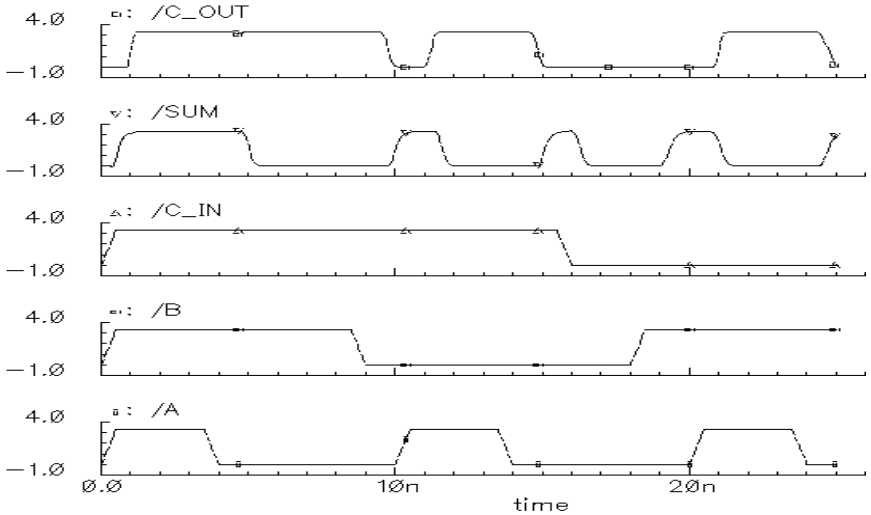

Figure 10: Schematic simulation of 1-Bit Adder

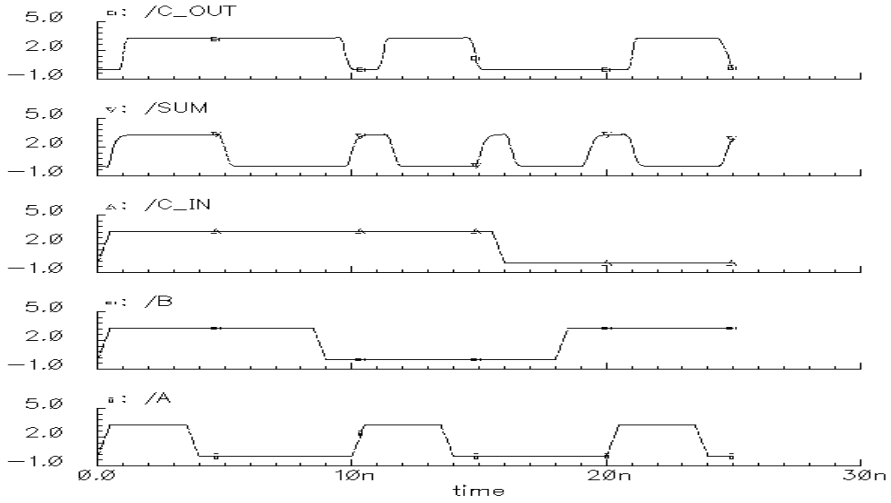

Figure 11: Simulation After Layout Extraction

3.2 Noise Margin Testing

The circuit below (Figure 12) is used to test noise margin of 1-bit adder. C_{in} connects to *Vss, A* connects to $V_{dd.}$ *B* is input signal, which is used to test and analysis DC characteristics. Its DC character is shown in Appendix 3.

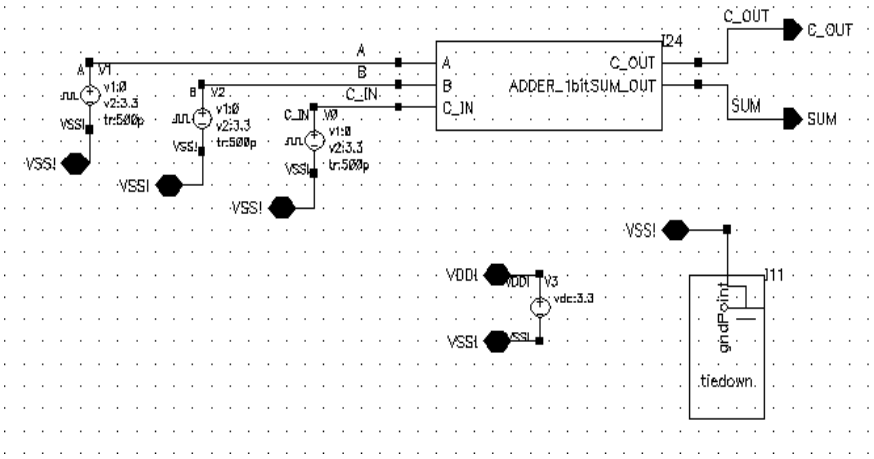

Figure 12. Noise Margin Testing

Noise Margin can be calculated from the data in Appendix 3.

$$NM_H = |V_{Ilmax} - V_{OLmax}| = |1.37 - 0.0| = 1.37\ V;$$
$$NM_L = |V_{lHmin} - V_{OHmin}| = |1.36 - 3.3| = 1.94\ V.$$

4. 4-Bit Adder Configuration and Testing

4.1 4-Bit Adder Configuration

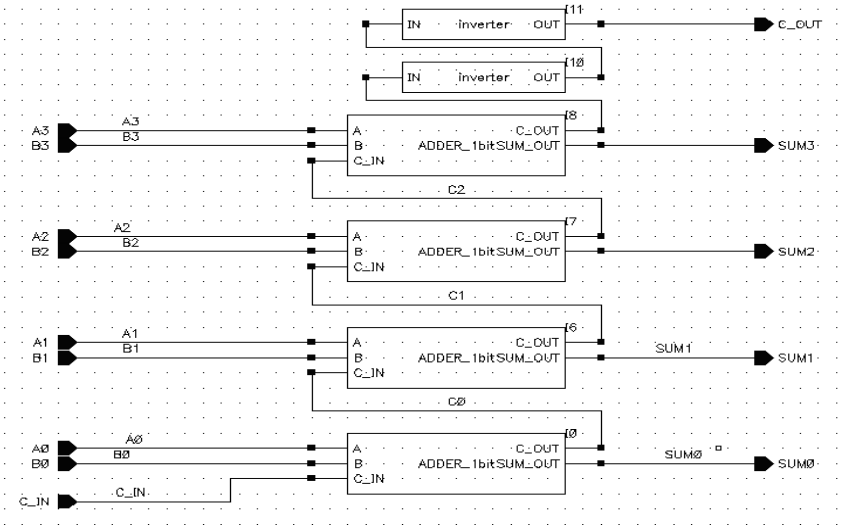

Figure 13: 4-Bit Adder circuit

The structure of 4-bit adder is composed of four 1-bit adder as shown in Figure 13.

4.2 4-Bit Adder Testing

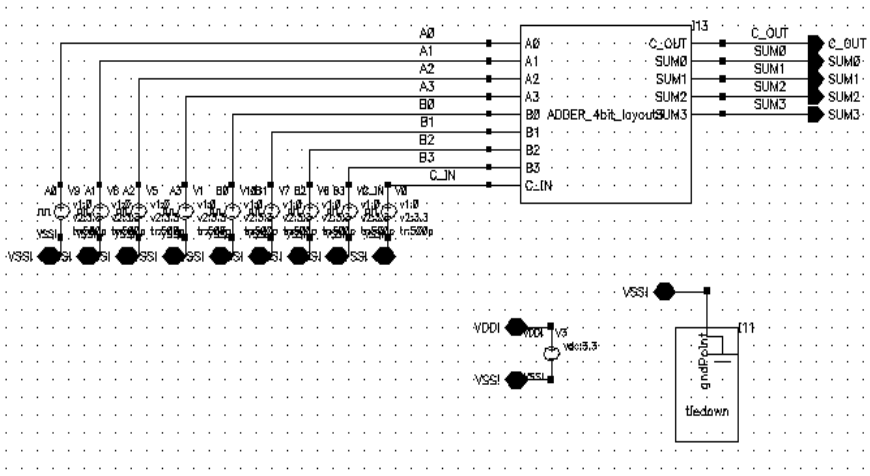

Figure 14: Testing of 4-Bit Adder

4.3 Layout of 4-Bit Adder

From layout figure in Appendix 4. *Area = 107.2 ×102.4μ^2=10977.28μ^2*

4.4 Logic Simulation of Layout

The logic simulation waveforms of are in Appendix 5.

4.5 Layout With PAD

The layout with PAD is show in Appendix 6.

5. Worst Case Testing of Adder

5.1 Description of Worst Case

The worse case occurs when P_0 P_1 P_2 P_3 all equal to "1", C_{in} is propagated to C_{out} and SUM_3 is determined by $C_{2,}$ etc. The testing circuit is shown in Figure 13. Here all *A* input set to "1" and all *B* input set to "0", when C_{in} changes the longest delay can be obtained from *SUM3* or C_{out}.

5.2 Simulation for Worst Case

The worse case testing circuit and the simulation results of schematic and layout are shown in Figure 15 and Figure 16 respectively. In layout simulation in Figure 17(also in Appendix 7, 8). The longest propagate delay occur on C_{in} to C_{out}

because of the line delay in layout. We can get the longest propagate delay from the waveform in Appendix 7.

$$t_{dr} = 1.09\ ns\ , \quad t_{df} = 1.24\ ns$$
$$T_{d\_avg} = 0.5\ (t_{dr} + t_{df})\ ns = 1.165\ ns$$

The longest rise and fall time happened on *SUM* out and can be obtained from Appendix 8.

$$t_r = 0.588\ ns\ , \quad t_f = 0.688\ ns$$

The rise time and fall time is less than 1.5ns, which satisfy design requirement.

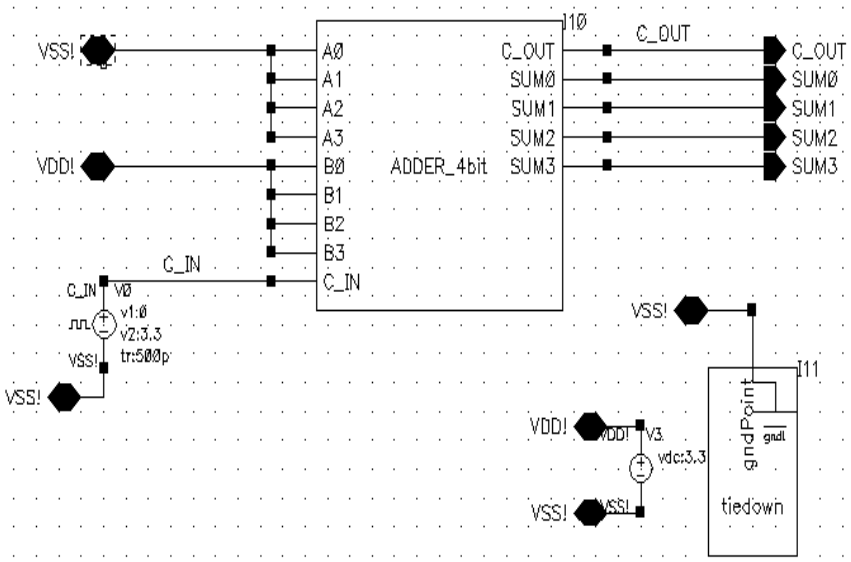

Figure 15. Testing for Worst Case

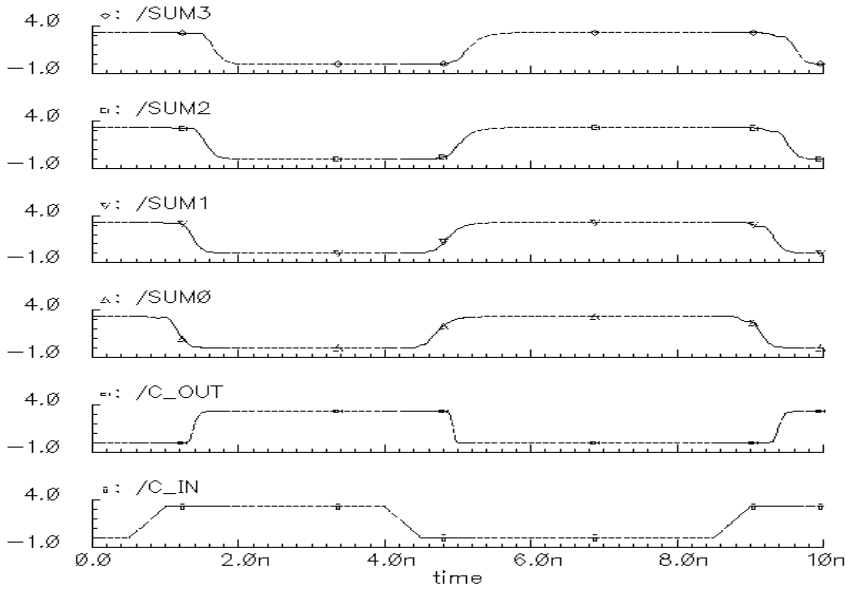

Figure 16. Schematic simulation of Worse Case

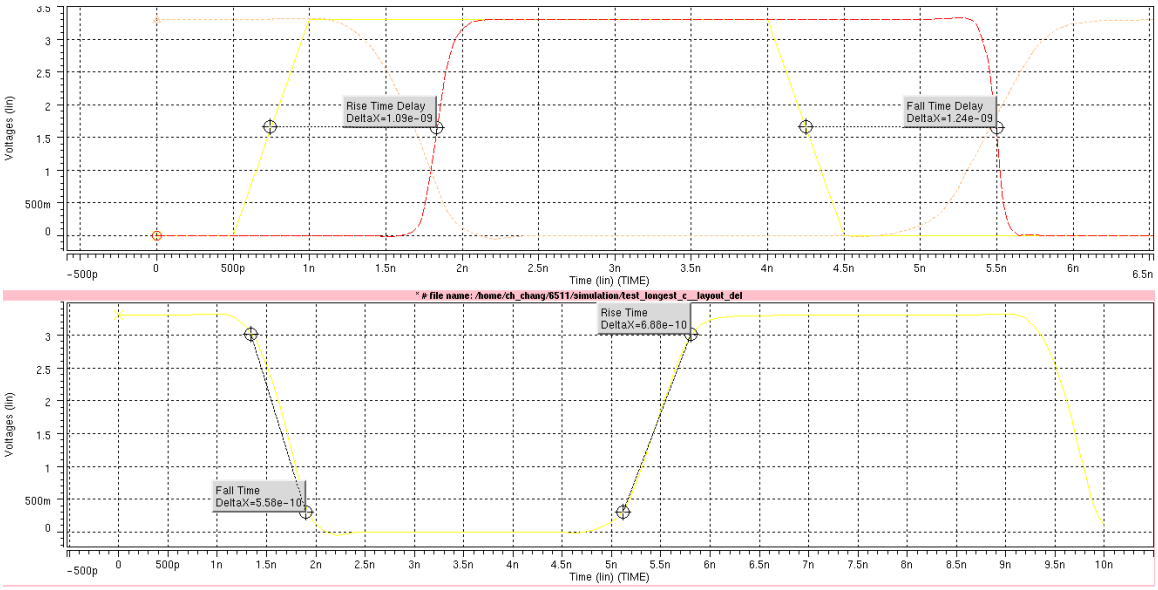

Figure 17. Layout simulation of Worse Case

6. Measurement of Power

The power estimation results on the whole Adder can be obtained from Appendix 9 as the following:

P_{avg} = 1.2476E-04 W (0.0000E+00 ~ 2.0000E-07)
P_{min} = 4.0597E-11 W (0.0000E+00 ~ 2.0000E-07, at 0.0000E+00)
P_{max} = 6.1909E-03 W (0.0000E+00 ~ 2.0000E-07, at 4.3250E-10)

7. Summary of Performance

The final performance indexes that have reached according to optimization requirement are listed below:

1). Area: $A = 10977.28\mu^2$
2). Average propagation delay time: T_{d_avg} = 1.165 ns
3). The maximum rise/full time: t_r = 0.588 ns , t_f = 0.688 ns
4). Product of Area and Time: $AT = 1.27\ (\mu^2\ ns)$
5). Product of Area Square and Time: $A^2\ T = 1.4\ (\mu^4\ ns)$
6). Average Power: P_{avg} = 1.2476E-04 W
7). Noise Margin: NM_H =1.37 V ;
NM_L =1.94 V.

8. Reference

1. Neil H. E Weste, Principles of CMOS VLSI Design --- A systems Perspective 2nd, Kamran Eshraghian, 1994.
2. Jan M. Rabaey, Digital Integrated Circuits --- A Design Perspective, Prentice-Hall, 1996.
3. John P. uyemura, CMOS Logic Circuit Design, Kluwer Academic Publishers,