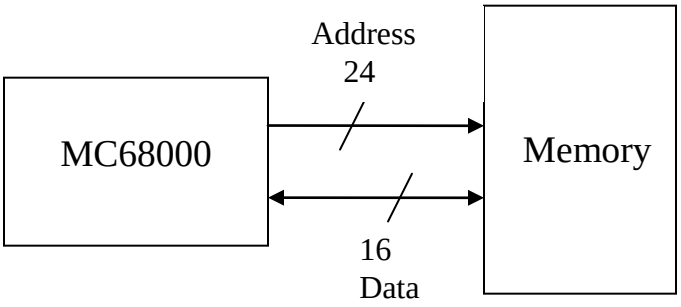
MC68000 Computer



First 1K of memory ($000000 – $0003FF) used by the processor as well as operating system for other useful purposes.

Memory

- smallest addressable unit is byte (byte organized)
- supports byte (8), word (16) and longword (32) representations
    - longword data should be aligned at word boundaries
- data allowed:
    - signed, unsigned integers
    - BCD
    - Character (operation of byte size)
    - Floating point instructions not supported but can be simulated

CPU

Data Registers: 8 of them (32 bits each), numbered 000 to 111

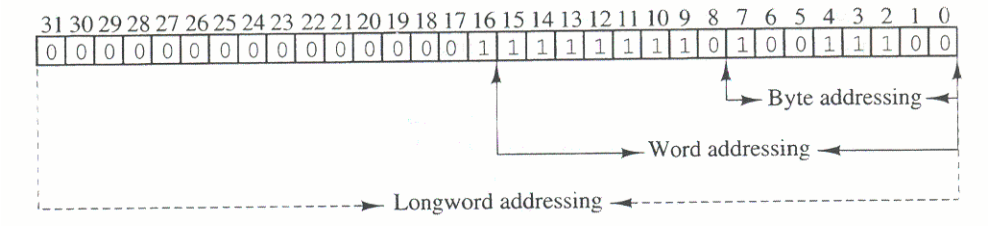


Figure 6.1 Addressing a data register

Figures from "Computer organization and the MC68000", P. E. Livadas and Ch. Ward

Address Registers: 8 of them (32 bits each), numbered 000 to 111

Address Registers A0 – A6, and A7.
A7 register is really two registers (User Stack Pointer USP, and System Stack Pointer SSP), but which one is addressed depends on the mode bit in Status Register.

Only Word and Longword operations allowed.

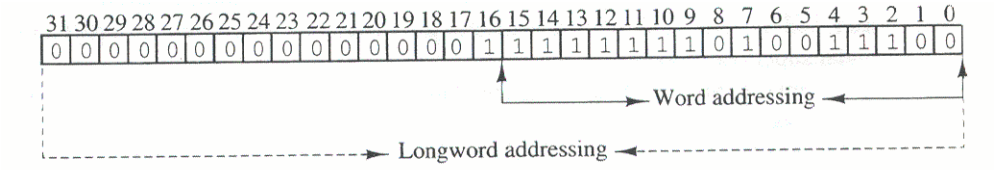


Figure 6.2 Addressing an address register.

Program Counter: 32 bits

Only Longword operations permitted

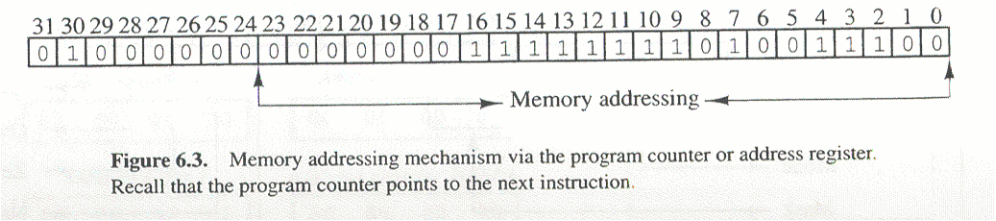


Figure 6.3. Memory addressing mechanism via the program counter or address register. Recall that the program counter points to the next instruction.

Status Register: 16 bits

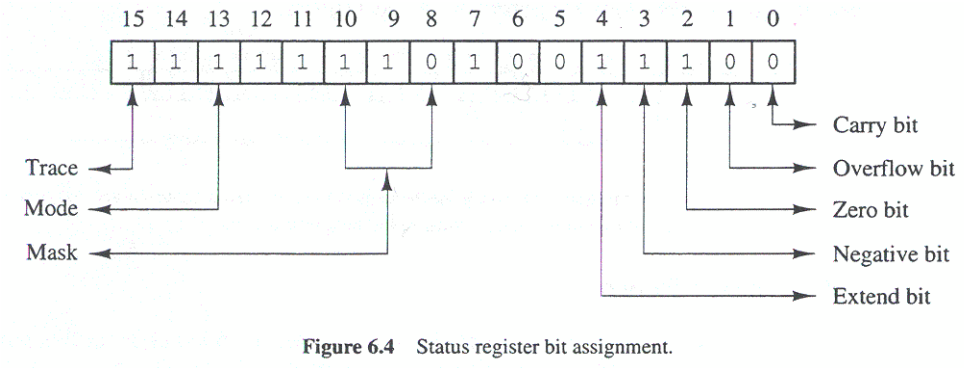


Figure 6.4 Status register bit assignment.

Figures from "Computer organization and the MC68000", P. E. Livadas and Ch. Ward

Bit 15: Trace Bit

- 0 (normal)
- 1 (trace mode)

Under trace mode the processor informs the monitor (operating system) each and every time an instruction is executed.
Monitor then runs its own code to dump register/memory.
Execution of entire program takes long time

Bit 13: Mode Bit

- 0 (User mode)
- 1 (Supervisor mode)

Under Supervisor mode, system routines are executing otherwise it is user mode where user program is running.

All instructions supported by MC6800 run only in supervisor mode but there are **privileged** instructions that cannot run in user mode.

Under User Mode: only USP accessible
Under Supervisor Mode: both USP and SSP are accessible

Bits 10, 9, and 8: Interrupt Mask bits

3 bits provide 7 levels of interrupt (level 1 to 7)

7: highest priority
1: lowest priority

If set to %110 (=6), service higher priority interrupt (i.e. 7) and ignore all lower priorities.
If set to %000 (=0), service all interrupts

Bits 0 to 4: Condition Code bits

C: Carry Bit
V: Overflow Bit
Z: Zero Bit
N: Negative Bit
E: Extend Bit

Figures from "Computer organization and the MC68000", P. E. Livadas and Ch. Ward

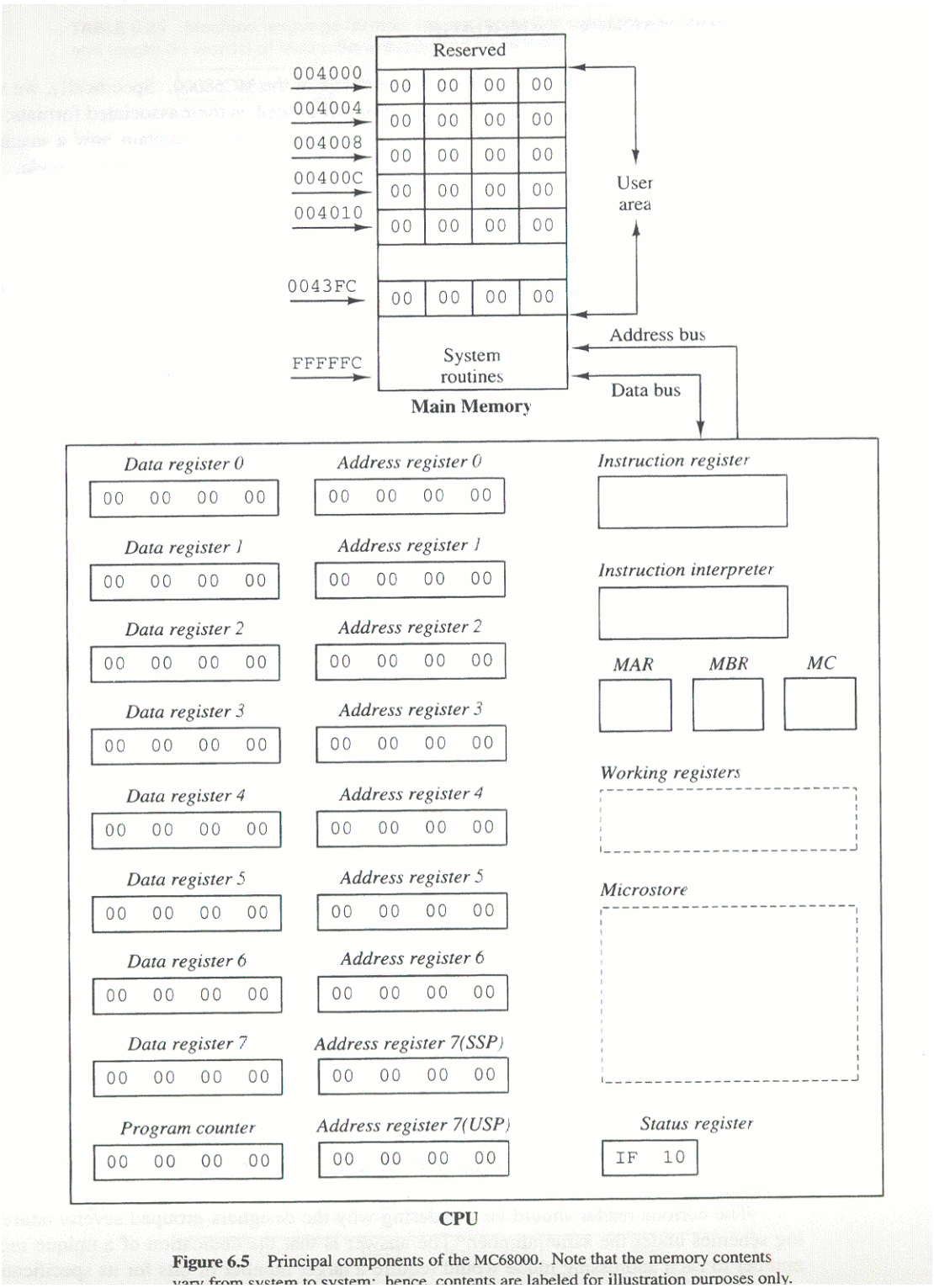


Figure 6.5 Principal components of the MC68000. Note that the memory contents vary from system to system; hence, contents are labeled for illustration purposes only.

Figures from “Computer organization and the MC68000”, P. E. Livadas and Ch. Ward