Fabrication, Layout and Design Rules

Process overview:

Oxidation
Is the process of converting silicon to silicon dioxide, which is a durable insulator. For IC manufacturing it has several uses such as selectively masking the chip components against implants or diffusion. It is also used as device and layer isolation it is also an important component in forming the gate of transistors as gate oxide. The oxidation process consumes the silicon.

Diffusion
It is the process of doping the silicon to introduce impurities. When used as part of fabrication process, it can create p, p+, n, n+ on the wafer. With normal diffusion techniques precise control is not possible and we usually use ion implant for better control. In general diffusion is good for heavy doping and creating deep junctions.

Deposition
It is the process of depositing selected material such as Polysilicon, silicon dioxide, aluminum, cupper silicon nitride over the entire wafer

Metalization
Is the process of depositing metals on silicon dioxide over the entire wafer. Different metals and alloys are deposited in new chip fabrication, replacing the old aluminum.

Etching
It is the process of selectively removing unwanted materials from the wafer surface. Two methods are used, wet etching and dry etching. Wet etching method has the disadvantage of producing undercuts. Dry etching on the other hand is good for small geometries.

Lithography
Is the process of patterning the layout to the masks. The masks have then opaque geometrical shapes corresponding to areas on the wafer to be either etched or left untouched. The masks then have two fields, the dark and clear field. Lithography can be performed optically or through ebeam.

In this site there are some animations that you might find useful.

http://www.virlab.virginia.edu/VL/MOS_kit.htm/state/related
http://www.virlab.virginia.edu/VL/MOS_kit.htm/state/19
Process and the masking Steps

The process of fabricating a wafer is different from a process to process. In here, the general procedure is shown:

We start with approximately 500µm slice of silicon ingot (already doped and at room temp. acts as semiconductor). On the same wafer many copies of the same chip is fabricated. At the end of fabrication only some of them work and that at different speed. Wafers are processed in clean rooms on automated fabrication lines.

First through a wet oxidization process a thick layer of SiO2 is formed on top of the silicon. This layer serves to isolate the substrate from whatever building blocks will be built on top of it.

Now through repeated photolithography and etching process using different masks we pattern the chip to the way that we want it.

Each masking step is highlighted to give an overall understanding of the overall process.

**nwell mask:** To fabricate an inverter, two substrates are required, the n-substrate for the pmos and the p-substrate for the nmos. Although there are processes that do create two substrates in our process, the process that we use has a p-substrate and we create a n-substrate within the p material. So the first lithographic operation defines the n-well region in the p-substrate.

The nwell mask is then used to dope some part of the substrate to n-type. Referring to the inverter layout shown below, the nwell mask is shown in dashed yellow.

Once the two substrates are formed, a thin layer of silicon dioxide is grown followed by a layer of silicon nitride. This action is used to mask the active regions from p-type and n-type implantations and to define the regions of field oxide growth.

**Device well mask:** This photolithographic step is used to leave the dielectric sandwich only in regions where the devices will be formed (drain, source and channel regions) or diffusion interconnect is required.

**n-guard mask:** is an oversized n-well mask. It is an inclusion mask. It is used to do n-implant into the nwell regions which eventually will be covered with field oxide regions. The method is used to set the threshold voltage under the field oxide to greater value than that under the gate oxide.

**p-guard:** This is an exclusion mask. It is used to define the regions which are to receive an n-implant, to set the threshold higher to reduce parasitic.

Following these steps, the field oxide is now grown into the regions not covered by the silicon nitride.

**Gate poly mask:** the Si3N4 and SiO2 are now etched away. A thin layer of high quality oxide (gate oxide 2—1 nm thick) is now deposited all over the wafer. This step is followed by a Polysilicon (0.8-0.5 µm thick) deposition step (CVD). The Polysilicon mask then is used in a lithographic step to pattern and plasma etch the poly and the silicon and at the end of this step we define the gate regions of the transistors (n and p).

**P+ mask:** drawn as inclusion mask, defines the areas that is to be doped P+. (drain, source and substrate contact region). Preference is usually for a shallow diffusion area with minimal lateral diffusion. Usually high doses are needed to make the drain of source a low resistance.

**N+ mask:** drawn as exclusion mask to define the areas to be N+ implanted. (drain, source and contact to substrate regions).
**Contact mask:** after deposition of a moderately thick layer of SiO₂ over the entire wafer, this mask is used to etch away the contact regions.

**Metalization mask:** Depending on the process used several metal layers might be used, where the steps of metallization is repeated. First a thick layer of SiO₂ is deposited as an insulator, then the metal alyer is deposited. Metallization mask is used to define the metal lines. This process might repeated for several metallization layers each of different thickness. (upto 9 layers these days)

**Passivation mask:** The final step in masking is to cover the entire wafer with thick SiO₂, then open up the boding pads area with the passivation mask.

Where to start with the layout?
The best place will be with the known dimensions. For example if you are drawing an inverter, start with either the nmos or pmos gate area. Since you know the gate length and width. Say we start with the poly mask.
Second step is that you know the width so, draw the device well.

At each point you have to check the design rules for any violations. If this is a pmos, then you need the substrate. Therefore you need an n-well.

Continue adding masks to build up the inverter, now you need the P+ mask to make the source and drain doped P+ so we have to do the P+ inclusion mask and the N+ exclusion
masks. (IN most processes, the P+ mask is sufficient and its inverse is used as the N+ mask. The N+ exclusion mask is around the P+ mask.

At each addition placed.

Below a complete inverter has been laid out. Please check the design against the design rules.

LAYOUT OF INVERTER USING CMOSIS5 TECHNOLOGY
(Numbers in red indicate rule number, numbers in black indicate size)
Note, the design uses split contacts.
Design of an inverter of size \((W/L)n=(W/L)p = 3 (W/L)\text{min}\) using the CMOSIS5 design Rules

Orange is oversized by 0.2 from each side.
Absolute Design Rules

Some CMOSIS 5 design Rules (ALL dimensions in micron, \( \mu \))

Poly
Min width .............................................. 0.6
Min Spacing ........................................... 0.6
Poly overlap of n/p island over field .................. 0.45

n-island (diffusion)
Min width .............................................. 0.6
Max length .............................................. 0.50
Spacing .................................................. 0.8
Minimum spacing butting with p-island .......... 1.0

n-well
Min width .............................................. 2.2
Active area to n-well spacing ....................... 1.5

Contact 1
Required size .......................................... 0.8 \( \times \) 0.8
Min enclosure by p or n island ................... 0.2
Spacing .................................................. 0.6

Metal 1
Min width .............................................. 0.6
Min spacing ........................................... 0.8
Min overlap of contact 1 ......................... 0.2

Contact 2
Required size .......................................... 0.8 \( \times \) 0.8
Min spacing ........................................... 0.6
Min spacing to contact 1 ......................... 0.3
Min enclosure by metal 1 ......................... 0.2

Metal 2
Min width .............................................. 0.6
Min spacing ........................................... 0.8
Min overlap of contact 2 ......................... 0.2
Check your layout!!

- Make sure your Vdd lines and Vss lines are separated at all points.
- Make sure the device wells are biased properly.
- Remove all unwanted space in your layout to have a minimum XY area.
- Did you perform DRC check on the layout?
- Did you put your design label on the layout

Design guidelines:

- Do not forget the concept of Hierarchy, modularity and locality in your design. (this also reduces your layout!!)
- Have you estimated your supply current? Have you enough Vdd and Vss pads to insure proper operation (electro migration, latchups etc. )
- Did you calculate the width of your Vdd and Vss busses for current capacity handling?
- Make sure to use many small vias instead of one large one. (avoid current crowding, electromigration ( aluminum spiking and ).
- Always use metal interconnects for global and intermediate interconnect. Try to use metal for local interconnect whenever possible.
- For large designs, use separate power/gnd pads for the I/O cells (reduce gnd and Vdd bounce as much as possible to feed through the circuit)
**Thin Oxide Mask (OD)** — as a Active or Diffusion Mask

OD.W.1 Min diffusion width = 0.4μ
OD.S.1  Spacing between diffusion areas = 0.6μ

**Nwell Mask (NW)**

NW.W.1  Min Nwell width = 1.7μ
OD.C.4  Min overlap over diffusion = 1.2μ
OD.C.3  Min spacing to external diffusion = 2.6μ
(Not Shown)
NW.S.1  Min Nwell spacing (different potential) = 3μ
NW.S.2  Min Nwell spacing (same potential) = 1μ

**Polysilicon Mask (PO)**

PO.Q.1  Min poly width = 0.35μ
PO.S.1  Min poly spacing = 0.45μ
PO.O.1  Min poly gate extension = 0.4μ
PO.C.1  Min poly to diffusion spacing = 0.2μ
PO.C.2  Min source/drain extension = 0.5μ

**P-plus Mask (PP) or N-plus Mask (NP)**

PP/NP.O.1  Min overlap over diffusion = 0.45μ
PP/NP.W.1  Min width of PP or NP =0.6μ
PP/NP.S.1  Min spacing between PP and/or NP = 0.6μ
PP/NP.C.1  Min spacing to unrelated diffusion = 0.35μ

**Contact Mask (CO)**
**CO.W.1**  Min/Max contact size = $0.4 \mu \times 0.4 \mu$

**CO.S.1**  Min contact spacing = $0.4 \mu$

**CO.E.2**  Min overlap poly or diffusion = $0.2 \mu$

**CO.C.1**  Min spacing to gate poly = $0.3 \mu$

**Via 1 Mask (VIA1)**

**VIA1.W.1**  Min/Max contact size = $0.5 \mu \times 0.5 \mu$

**VIA1.S.1**  Min contact spacing = $0.45 \mu$

**VIA1.E.1**  Min M1 extension over via = $0.2 \mu$

**Metal 1 Mask (M1)**

**M1.W.1**  Min metal width = $0.5 \mu$

**M1.S.1**  Min metal spacing = $0.45 \mu$

**M1.E.1**  Min metal extension over contact = $0.15 \mu$

**Metal 2 Mask (M2)**

**M2.W.1**  Min metal width = $0.6 \mu$

**M2.S.1**  Min metal spacing = $0.5 \mu$

**M2.E.1**  Min metal extension over contact = $0.15 \mu$

**Poly2 Mask (PO2) — Used for Poly1/poly2 capacitors**

**PO2.W.1**  Min width of PO2 for cap to plate = $0.8 \mu$

**PO2.E.1**  Min extension of PO past PO2 = $1.0 \mu$
PO2.E.2 Min extension of PO2 past CO = 0.6μ
PO2.C.1 Min clearance to CO on PO from PO2 = 1.2μ

**Colour Codes used (CMOS 4B)**

- **CP** Polysilicon, defines, transistor gates
- **CP+, P+ Diffusion** (Doted Blue), defines areas to be doped P+
- **CN+, N+ Diffusion** (Dotted Red), defines areas to be doped N+
  This is an exclusion mask
- **CM1, Metal 1** (Doted Black), defines Metal 1 metallization
- **CP, P guard,** an Exclusion mask. It is drawn around the N-well mask.
  This is used to increase p-substrate doping around field oxide
  It provides better isolation between devices.
- **CF, Field,** defines active device area,
  ie, drain gate and source area.
- **CM2, Metal 2** defines metal 2 metallization
- **CC, (Contact cut),** defines contact areas from metal1 to diffusion, poly.
- **Via** defines contact areas for different metallization layers.
- **Nwell** Doted Yellow, defines the n-well region
**λ-Based Design rule**

**A. N-well**
- A.1 Minimum size \( \frac{\lambda}{10} \)
- A.2 Minimum spacing 6
  (Same potential)
- A.3 Minimum spacing 8
  (Different potentials)

**B. Active (Diffusion)**
- B.1 Minimum size 3
- B.2 Minimum spacing 3
- B.3 N-well overlap of \( p^+ \) 5
- B.4 N-well overlap of \( n^+ \) 3
- B.5 N-well space to \( n^+ \) 5
- B.6 N-well space to \( p^+ \) 3
C. PolyI
C.1 Minimum size 2
C.2 Minimum spacing 2
C.3 Spacing to Active 1
C.4 Gate extension 2

D. p-plus/n-plus
D.1 Minimum overlap of Active 2
D.2 Minimum size 7
D.3 Minimum overlap of Active in abutting contact 1
D.4 Spacing of p-plus/n-plus to n+/p+ gate 3
E. Contact
   E.1 Minimum size  2
   E.2 Minimum spacing (Poly)  2
   E.3 Minimum spacing (Active)  2
   E.4 Minimum overlap Active)  2
   E.5 Minimum overlap of Poly  2
   E.6 Minimum overlap of Metal  1
   E.7 Minimum spacing to Gate  2

F. Metal 1
   F.1 Minimum size  3
   F.2 Minimum spacing  3

G. Via
   G.1 Minimum size  3
   G.2 Minimum spacing  3
   G.3 Minimum Metal I overlap  1
   G.4 Minimum Metal II overlap  1

H. Metal II
   H.1 Minimum size  3
   H.2 Minimum spacing  4

I. Via2
   I.1 Minimum size  2
   I.2. Minimum spacing  3

J. Metal III
   J.1 Minimum size  8
   J.2. Minimum spacing  5
   J.3 Minimum Metal II overlap  2

K. Passivation
   K.1 Minimum opening  100µ
   K.2 Minimum spacing  150µ
Layout of an inverter with the $\lambda$-based design rule