A novel and low-cost multi-stage approach for the fabrication of silicon nano-structures

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ABSTRACT

A new multi-stage technique for the fabrication of arrays of silicon nano-structures is introduced; the growth mechanism of the developed nano-structures is investigated. In this technique, surface of silicon wafers were textured using anisotropic etching method to generate pyramid structures. The textured surfaces were then etched by electrochemical anodic etching. During anodic electrochemical etching in HF solution, the etching initiated at the edge of the pyramids and progressed inward through the faces. The four 1 1 1 faces of the pyramids etched forming a pore at each face. To develop the nano-structures, at the final fabrication stage, the interconnected walls have been etched using NaOH. Results show that the tip of pyramids corresponds to the tip of nano-structures. A good correlation between the number of pyramids per unit surface area and that of the nano-structures was observed. It was also observed that the nano-structure formed only for high pyramid surface coverage. The effect of anodic electrochemical parameters such as current density and etching time on the fabrication of the silicon nano-structure was investigated. Longer electrochemical etching resulted in thinner interconnect walls, needing shorter NaOH etching time to form and reveal the nano-structure array.

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1. Introduction

Electrochemical etching of silicon in HF solution has attracted a great attention for the fabrication of various micro-structures such as porous silicon [1], trenches [2], and pillars [3,4]. Recently, fabrication of one-dimensional n-type silicon nanowires from porous silicon has been developed using photo-assisted electrochemical etching [5]. This fabrication method uses oxidation and/or wet etching as post-processing techniques leading to the creation of pillars and nanowires.

In order to pre-determine the location of the fabricated silicon nanowires, in the conventional method, the silicon surface is first patterned using lithography technique followed by wet etching [6,7]. This technique leads to the creation of inverted pyramids on the silicon surface followed by the formation of porous silicon starting at the pit of these inverted pyramids.

In this work, a new non-lithographical method was used for the fabrication of silicon nano-structure arrays. In this approach, the pyramid shape seeding points were first created on the surface of the silicon. Each of these pyramids will become the tip of the silicon nano-structures created in the subsequent fabrication stages. However, the anisotropic etching creates randomly distributed pyramids on silicon surface; the position of the created nano-structures in the subsequent fabrication stages is pre-determined by the location of these pyramids. This method of synthesizing silicon nano-structure arrays is appealing because the process is non-lithographic and can lead to a low-cost route for fabricating micro/nanoelectronic devices.

The detailed studies on growth mechanism of the nanowires helped develop methods to control the array density and nano-structure size characteristics. To the best of our knowledge this is the first report of implementing the electrochemical anodic etching on the textured pyramids surface with no lithography technique aimed at fabrication of silicon nano-structure arrays.

The influence of NaOH fine-etching time on the morphology and geometry of the nano-structure arrays was investigated in our previous work [8]. Here we report the impact of anodic electrochemical conditions and pyramid surface coverage on the fabrication of silicon nano-structure array.

2. Experimental procedure

Silicon wafers with (1 0 0) orientation (10–20 Ω cm) were purchased from Silicon Inc. and were used for all experiments. All experiments were carried out on p-type silicon, so that, due to the existence of hole majority carriers, no illumination of the sample is required. All samples were cleaned prior to experiments using the RCA process [9]. 25 wt.% tetramethylammoniumhydroxide (TMAH)
was purchased from Sachem Inc. and diluted with DI water to reach the desired 1.5 wt.% concentration used in all experiments. 95% isopropyl alcohol (IPA) was purchased from VWR International and added to the etching solution to obtain 1.5 wt.% and 6 wt.% weight concentrations. 99.5% ethanol, and 97+% NaOH were purchased from Sigma–Aldrich. 48.8% HF was purchased from ACP Chemicals Inc. Canada. The anodic electrochemical etching was performed using Allied Research galvanostat potentiometer. The developed nano-structures were characterized using Hitachi S-4700 field emission scanning electron microscopy (FE-SEM). The population density of structures and surface coverage measurements were all obtained by performing image analysis of the SEM photos using Image J image processing program developed by the US National Institute of the Health.

This novel approach requires three stages of fabrication to create the desired nano-structure array. The three stages are as follows:

1. Anisotropic wet etching to create textured silicon surface.
2. Anodic electrochemical etching of the textured silicon to create a porous layer.
3. Fine-etching of porous silicon layer to achieve the desired nano-structure array.

2.1. The fabrication process flow

2.1.1. Fabrication of the pyramids (1st stage)

Surface of a 1 cm² samples of silicon wafer were textured using anisotropic etching process in 1.5 wt.% TMAH for 30 min. Pyramids with various sizes were developed on the surfaces of the samples. During the process IPA was added to TMAH solution in order to remove the hydrogen bubbles from surface of the sample faster to facilitate the etching process. As we have reported in the earlier work, the concentration of the added IPA will influence the size and surface coverage of the pyramids [10]. In this stage we have used samples etched in TMAH with added various IPA concentrations (0, 1.5, and 6 wt.%). The samples were used to study the effect of pyramids concentrations on the developed final nano-structures.

2.1.2. Creation of porous silicon (2nd stage)

An anodic electrochemical etching was performed on the textured silicon surface to create a layer of porous silicon. The etching was done in a two-electrode Teflon cell with metal base plate to form a back ohmic contact. A thin layer (~1 μm) of aluminum was deposited on the back side of the silicon wafer to obtain an ohmic contact. The silicon wafer is served as working electrode (anode) and the platinum mesh served as counter electrode (cathode). Experiments were performed with various anodic current densities and etching time in such a way that the total charge participating in the reaction, Q, was kept constant at 144 C/cm². Q can be calculated by multiplying the current density (0.08 C/s cm² = 0.08 A/cm²) times the etching time (1800 s). Therefore, two parameter values that affect this total charge are (1) the current density, and (2) the etching time. In order to keep this charge constant, if the value of one parameter increases then the other parameter value must decrease and vice versa. The etching solution (electrolyte) consisted of 1:3 (HF:ethanol) mixture for all experiments. Ethanol was added as a surfactant to facilitate the detachment of the hydrogen bubbles from the surface of the silicon, therefore, resulting in the formation of a more uniform porous layer.

2.1.3. The creation of silicon nano-structure array (3rd stage)

Alkaline solution, consisting of a diluted NaOH (0.2 M), was used to fine-etch the porous silicon layer in order to achieve the desired nano-structure. In this fabrication stage, the walls connecting the pillars in the porous silicon were etched until the desired nano-structure array was achieved. A few drops of IPA were applied to the surface of the sample (porous silicon) to increase its wet-ability before immersing it into the NaOH solution. The temperature was kept constant at 35 °C, and some agitation was applied using a magnet stirrer.

3. Results and discussion

3.1. Characterization of the textured silicon surface

Samples with different pyramid surface coverage (during the first stage of anisotropic etching) were achieved as a result of various IPA concentrations. Fig. 1(a) illustrates the SEM image of a sample textured using 1.5 wt.% concentration for IPA (high surface coverage). Fig. 1(b) illustrates the use of image analysis of SEM image to calculate the surface coverage and the number of pyramids per unit area.

Table 1 summarizes the influence of various IPA concentrations on the resulting pyramids surface coverage and the number of pyramids per unit area. In order to obtain an average of the measured values, the same experiment was repeated a few times. As it may
be observed from Table 1, as the IPA concentration increases so do the average pyramids surface coverage and the average number of pyramids per unit area.

These results were used to correlate the morphology and density of the fabricated nano-structure array to that of the pyramid-textured surface. The density of the pyramids and how closely packed they were, influenced the creation of the nano-structure array in subsequent fabrication stages.

3.2. Characterization of the porous silicon layer created at 2nd stage

To investigate the effect of anodic electrochemical etching parameters on the desired nano-structure, experiments were conducted with various anodic current density and anodic etching time but under constant total charge, Q = 144 C/cm². The HF:ethanol concentration ratio was kept constant at 1:3 for all experiments.

3.2.1. Pores initiation and growth mechanism

Fig. 2 illustrates the progress of the pore formation during the anodic etching stage. The textured surface illustrated in Fig. 2(a) was prepared under the texturing condition of sample 2 listed in Table 1. Fig. 2(b) shows the pore formation progress after 1 min. It was observed, that the pore formation initiated from the edge of the pyramids. Image 2(c) is the top view of the silicon sample after 3 min of anodic etching. The etching had initially started at the edges (Fig. 2b), followed by the etching of the pyramid faces. The tip of the pyramid identified in Fig. 2(c) by a square, has remained passivated and unetched. The arrows in Fig. 2(c) identify the four 1 1 1 faces of the pyramid where the etching took place during the porous formation. Fig. 2(d) shows the cross sectional view of the same sample where the two arrows illustrate the etched pyramid faces.

As it has been reported in the literature, in the case of the inverted pyramids textured surface, the pore formation started from the pit of the inverted pyramids due to the higher electric field [11]. Here we report that the pore formation initiation point to be the edges of the pyramids and not the sharp tips. This may be attributed to the roughness that had been created as a result of the anisotropic etching during the first fabrication stage. It has been reported that the roughness of the (1 1 1) planes leads to the formation of di-vacancies and tri-vacancies [12,13]. During anodizing etching, the dangling bonds on silicon surface are terminated by hydrogen atoms in the forms of mono, di, and trihydride in HF solution [14]. However, the number of hydride depends on the orientation and roughness of the surface [14,15]. The dihydride (Si−H₂) and trihydride (Si−H₃) termination on silicon surface results in a stronger polarization of the back Si−Si bonds. This polarization is considered to be responsible for weakening the back Si−Si bonds and therefore, facilitate their removal. The initiation of the etching at the edges of the pyramids followed by the 1 1 1 faces may be attributed to the trihydride termination of the surface atoms which leads to the preferentially attacked 1 1 1 faces.

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Calculated surface coverage and number of pyramids per 1000μm² using image analysis.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Sample 1</td>
</tr>
<tr>
<td>IPA concentration (wt.%)</td>
<td>0</td>
</tr>
<tr>
<td>Average Surface coverage of pyramids (%)</td>
<td>48</td>
</tr>
<tr>
<td>Average no. of pyramids per 1000 μm²</td>
<td>31</td>
</tr>
</tbody>
</table>
3.2.2. Porous formation under various anodic etching conditions with constant charge passed

The effect of various anodic current density and anodic etching time (at constant charge passed) on the formation of silicon porous layer were investigated using sample 2 (Table 1) as the substrate. Furthermore, the impacts of these anodic conditions on the fabrication of the desired silicon nano-structure array in the subsequent stages were studied. The current density and the etching time were altered such a way that Q remained the same for all experiments.

Fig. 3(a) illustrates top view of the morphology of the porous silicon layer created on sample 2 using 80 mA/cm², and 30 min for anodic current density and etching time respectively. The figure shows the porous silicon consisting of pillars and walls connecting them. It also shows the passivated and unetched tip of the pyramids after 30 min of etching time. The circled area in Fig. 3(a) is magnified and illustrated in Fig. 3(b) identifying the pillars and the wall. Fig. 3(c) illustrates the 45° tilted view of Fig. 3(a).

This morphology may be attributed to the etching of the edges followed by the faces of the pyramids.

Table 2 lists the experimental parameter values used for anodic current density and etching time.

Image analysis was performed on the SEM images of the anodically etched samples to obtain the average number of pillars per unit area, the average surface coverage of pillars, as well as the porous layer depth also listed in Table 2.

Experiments showed that, at current higher than 80 mA/cm², the samples were polished and no porous silicon layer was created. It can also be observed from Table 2 that, as the current density decreased and etching time increased (under constant charge passed condition), the average number of pillars per unit area, pillars surface coverage, as well as the porous layer depth increased.

Comparing the results in Table 1 with those in Table 2, one may observed that, for the same surface area, the number of created pillars is less than the number of pyramids. This may be due to the completely etched of the smaller pyramids during the anodic etching stage.

3.3. Characterization and analysis of the nano-structure array created at 3rd stage

3.3.1. Effect of anodic etching conditions with constant Q

As it was listed earlier in Table 2, samples with different morphology of porous layer were obtained as a result of various anodic etching conditions. The porous silicon layer can be removed using different alkaline solutions like KOH, NaOH, and TMAH [16,17]. In this work we have used low concentration of NaOH (caution should be taken to keep etching rate low enough to avoid destroying the nano-structures) to remove the interconnected walls between the pillars to reveal the nano-structures. Fig. 4 illustrates the effect of anodic etching conditions on the number of pillar (pre-NaOH etching) as well as the number of nano-structures (post-NaOH etching) per 1000 µm². It can be observed that, with a constant charge passed, a combination of lower current density and higher etching time results in higher number of pillars.

However, only a specific anodic etching condition (80 mA/cm² and 30 min) results in the creation of nano-structure arrays at the end of the final stage of the fabrication. In fact, further away from this optimal condition, almost no nano-structure was achieved. As the anodic current was reduced the pore diameter decreased resulting in the creation of thicker walls. On the other hand, as the etching time increased, the depth of the pores increased as well. A combination of thicker wall (connecting the pillars) and deeper pores created at the 2nd fabrication stage may hinder the formation of the nano-structures in the 3rd stage.
Table 3
Measured geometric characteristics of nano-structures for samples under different etching times.

<table>
<thead>
<tr>
<th>Anodic etching time (min)</th>
<th>Tip diameter (nm)</th>
<th>Length (μm)</th>
<th>Rod diameter (μm)</th>
<th>Aspect ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) 30</td>
<td>50</td>
<td>15</td>
<td>2</td>
<td>7.5</td>
</tr>
<tr>
<td>(b) 15</td>
<td>100</td>
<td>10</td>
<td>3</td>
<td>3.3</td>
</tr>
<tr>
<td>(c) 5</td>
<td>500</td>
<td>4</td>
<td>2.5</td>
<td>1.6</td>
</tr>
</tbody>
</table>

Fig. 4. Number of pillars per 1000 μm² and number of nano-structures per 1000 μm² at various anodic etching conditions.

Fig. 5. The nano-structure array fabricated under constant 80 mA/cm² and various etching time: (a) anodic etching time (30 min), NaOH etching time (2.5 min), (b) anodic etching time (15 min), NaOH etching time (4 min), and (c) anodic etching time (5 min), NaOH etching time (5 min).
3.3.2. Effect of anodic etching condition at various Q values

As it was shown in Fig. 4, the nano-structures were obtained only under certain anodic etching condition (80 mA/cm², 30 min). In order to investigate the effect of anodic etching conditions with various Q on the creation of nano-structure arrays, the current density was kept constant at 80 mA/cm², while the anodic etching time was changed. Shallower pores with thicker walls were fabricated under 80 mA/cm² current density when etched the samples for 5 and 15 min. However, to achieve the nano-structures, the NaOH fine-etching time needed to be increased in order to compensate for the thicker walls. Fig. 5 illustrates the nano-structures when the anodic current density was kept at 80 mA/cm² for various anodic etching times. The NaOH fine-etching time was increased to obtain the desired nano-structure arrays.

Table 3 summarizes the influence of the anodic etching time on the geometry and aspect ratio of the fabricated nano-structure arrays. The longer the anodic etching time, the higher aspect ratio was achieved. It can also be observed from Table 3 that as the anodic etching time is increased, the tip diameter of the nano-structure becomes smaller.

3.3.3. Effect of pyramid surface coverage

In order to investigate the effect of pyramid surface coverage on creation of nano-structure array, samples with various surface coverage were fabricated (as detailed in Section 3.1). Then the samples listed in Table 1 were anodically etched under the best set of anodic etching conditions, 80 mA/cm² and 30 min (as illustrated in Fig. 4) followed by etching in NaOH solution.

Fig. 6 shows the relation between the surface concentration of pyramids to the concentration of produced nano-structures. It was observed, that there is a correlation between the pyramid surface coverage and the number of generated nano-structures. As the pyramid surface coverage increases, the number of nano-structure also increases. It may also be noted, that number of nano-structures decreases dramatically as the pyramid surface coverage gets below 80%. This may be attributed to the fact that, as pyramids surface coverage decreases, the spaces between the pyramids increase. This results in random pores creation in the empty space between the pyramids. The creation of random pores with smaller diameters (and therefore thicker walls) hinders the removal of the walls (to generate nano-structures) at the NaOH etching stage. The number of nano-structures is increased as the rate of pyramid surface coverage goes above 80%. However, at much higher rates, the ratio of the pyramid to nano-structure stayed practically the same. This shows that the number of nano-structures per a certain surface area may be increased (higher density) without having an impact on the conversion rate.

4. Conclusions

Silicon nano-structure array was fabricated through a novel low-cost multi-stage approach. The pyramid structures practically covered the entire silicon surface as a result of anisotropic wet etching technique. This stage was followed by electrochemical anodic etching. The etching initiated at the four edges of the pyramids and progressed inward through 111 faces. The pores are grown vertically along the [1 0 0] direction at each face. In the final stage the interconnected porous walls are etched, to form the nano-structure array.

The first fabrication stage is a vital step toward the fabrication of silicon nano-structure arrays. The highly packed pyramids surface coverage is a prerequisite for fabrication of silicon nano-structure array, as the number of nano-structures drops dramatically below 80% and no nano-structures were obtained at low surface coverage values of around 50%.

Experiments revealed that, for a constant charge passed, as the current density decreases the pillar density increases. On the other hand, the higher number of pillars per surface area does not necessarily result in higher number of nano-structures. Accordingly, the optimal current density value seems to be around 80 mA/cm² as greater values resulted in no nano-structure formation (due to surface polishing) and at lower values, the creation of thick walls prevented the transformation of the created pillars into nano-structures.

The anodic etching time may be used as a practical parameter to control some nano-structure characteristics such as length and thickness.

The fabricated nano-structure arrays may have wide applications in MEMS/NEMS, energy storage and harvesting, solar cells and electron emitters in field emission devices.

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References


Biographies

Bahareh Yaghootkar was born in Iran on June 2, 1979. She received the BS and MS degrees in Electrical and Electronics Engineering from Azad University, Iran, in 2003 and UTM, Malaysia, in 2009, respectively. During 2003–2004, she was with Nanoelectronics Inc., Iran, as a QC engineer. In 2009, she was a research engineer at the National University of Singapore in the field of BioMEMs. She is presently pursuing her PhD degree at the Department of Electrical and Computer Engineering at Concordia University, Canada. The research area of her interest mainly includes fabrication and characterization of silicon nano-structures.

Mahmoud Amouzgar graduated from McGill University in Electrical Engineering in 1989. He has worked in the industry for over 15 years mostly in Telecom and Software Engineering fields. He completed his master’s degree in software engineering from SMU (Dallas) in 2000. He joined Dallas Community College in 2002 developing and teaching IT and computer programming courses for few years as a faculty member. He started his PhD in Electrical Engineering at Concordia University in 2009. His main research focus is on improving the efficiency of solar cells and sensors while lowering their material and fabrication costs using nanoscience and nanotechnology.

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