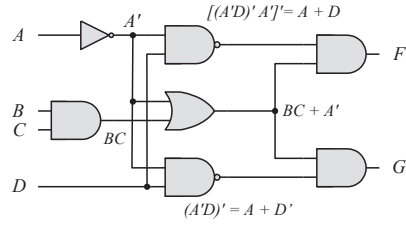
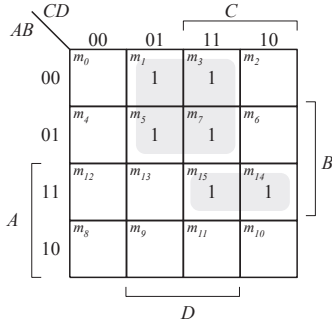


4.2

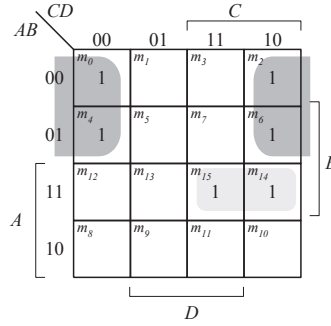


$$F = (A + D)(A' + BC) = A'D + ABC + BCD + A'D + ABC$$

$$F = (A + D')(A' + BC) = A'D' + ABC + BCD' = A'D' + ABC$$



$$F = A'D + ABC + BCD = A'D + ABC$$



$$G = A'D' + ABC + BCD' = A'D' + ABC$$

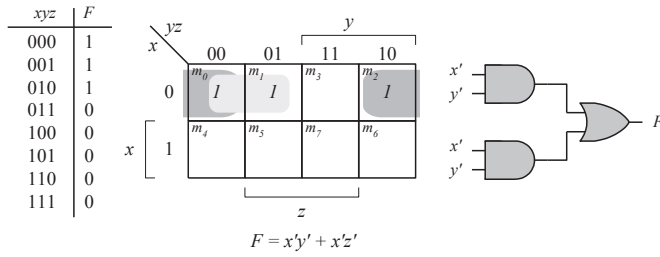
4.3

(a) $Y_i = (A_i S' + B_i S)E'$ for $i = 0, 1, 2, 3$

(b) 1024 rows and 14 columns

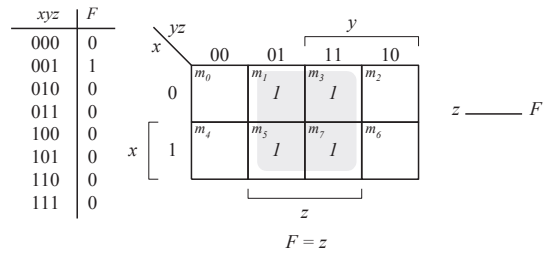
4.4

(a)

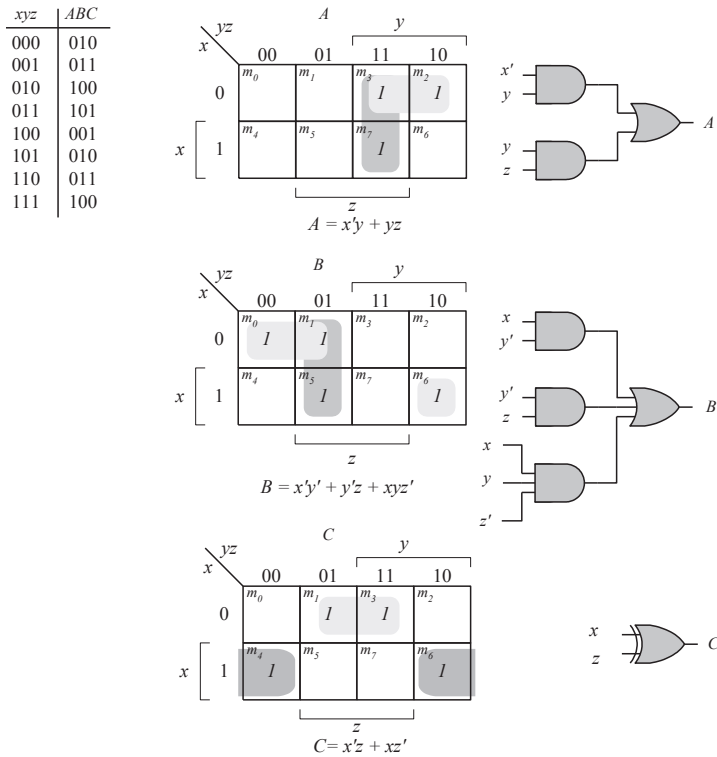


$$F = x'y' + x'z'$$

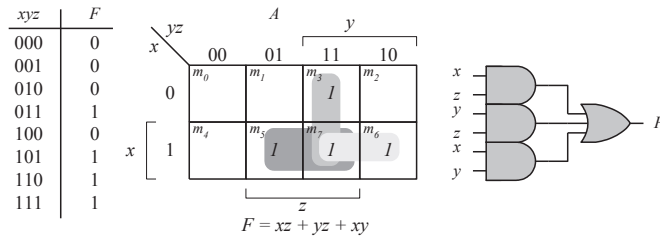
(b)



4.5



4.6



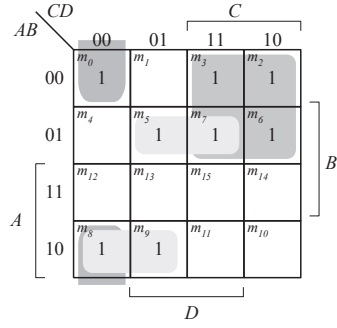
```

module Prob_4_6 (output F, input x, y, z);
  assign F = (x & z) | (y & z) | (x & y);
endmodule

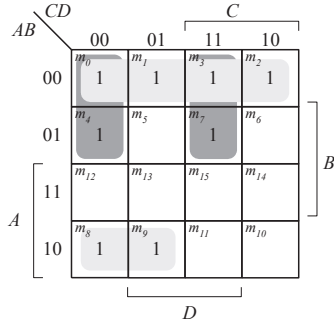
```

4.9

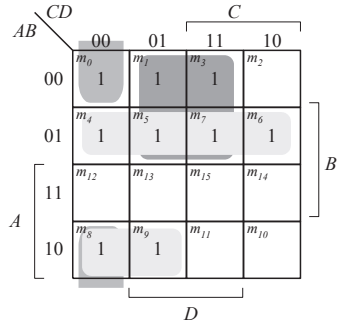
ABCD	a	b	c	d	e	f	g
0000	1	1	1	1	1	1	0
0001	0	1	1	0	0	0	0
0010	1	1	0	1	1	0	1
0011	1	1	1	1	0	0	1
0100	0	1	1	0	0	1	1
0101	1	0	1	1	0	1	1
0110	1	0	1	1	1	1	1
0111	1	1	1	0	0	0	0
1000	1	1	1	1	1	1	1
1001	1	1	1	1	0	1	1



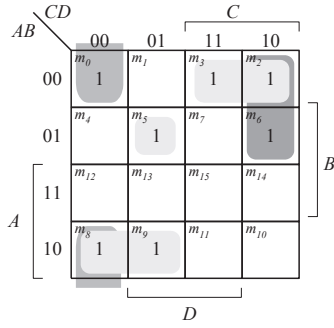
$$a = A'C + A'BD + B'C'D' + AB'C'$$



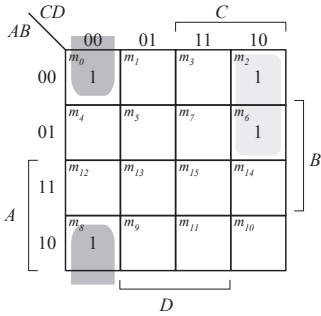
$$b = A'B' + A'C'D' + A'CD + AB'C'$$



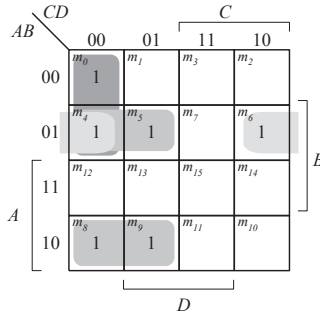
$$c = A'B + A'D + B'C'D' + AB'C'$$



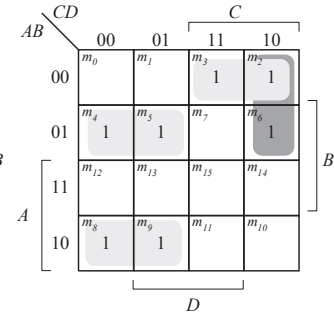
$$d = A'CD' + A'B'C + B'C'D' + AB'C' + A'BC'D$$



$$e = A'CD' + B'C'D'$$



$$f = A'BC' + A'C'D' + A'BD + AB'C'$$



$$g = A'CD' + A'B'C + A'BC' + AB'C'$$

4.13	Sum	C	V
(a)	1101	0	1
(b)	0001	1	1
(c)	0100	1	0
(d)	1011	0	1
(e)	1111	0	0

4.14 xor AND OR XOR
 $10 + 5 + 5 + 10 = 30 \text{ ns}$

4.15 $C_4 = G_3 + P_3C_3 = G_3 + P_3(G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0)$
 $= G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$

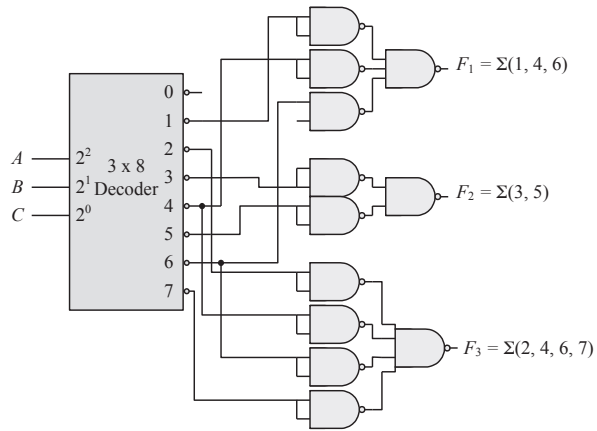
4.16 (a)
 $(C_iG_i + p_i)' = (C_i + G_i)P_i = G_iP_i + P_iC_i$
 $= A_iB_i(A_i + B_i) + P_iC_i$
 $= A_iB_i + P_iC_i = G_i + P_iC_i$
 $= A_iB_i + (A_i + B_i)C_i = A_iB_i + A_iC_i + B_iC_i = C_{i+1}$
 $(P_iG_i) \oplus C_i = (A_i + B_i)(A_iB_i)' \oplus C_i = (A_i + B_i)(A_i' + B_i') \oplus C_i$
 $= (A_i'B_i + A_iB_i') \oplus C_i = A_i \oplus B_i \oplus C_i = S_i$

(b)
Output of NOR gate $= (A_0 + B_0)' = P'_0$
Output of NAND gate $= (A_0B_0)' = G'_0$
 $S_1 = (P_0G'_0) \oplus C_0$
 $C_1 = (C'_0G'_0 + P'_0)'$ as defined in part (a)

4.17 (a)
 $(C_iG_i + P_i)' = (C_i + G_i)P_i = G_iP_i + P_iC_i = A_iB_i(A_i + B_i) + P_iC_i$
 $= A_iB_i + P_iC_i = G_i + P_iC_i$
 $= A_iB_i + (A_i + B_i)C_i = A_iB_i + A_iC_i + B_iC_i = C_{i+1}$
 $(P_iG_i) \oplus C_i = (A_i + B_i)(A_iB_i)' \oplus C_i = (A_i + B_i)(A_i' + B_i') \oplus C_i$
 $= (A_i'B_i + A_iB_i') \oplus C_i = A_i \oplus B_i \oplus C_i = S_i$

(b)
Output of NOR gate $= (A_0 + B_0)' = P'_0$
Output of NAND gate $= (A_0B_0)' = G'_0$
 $S_0 = (P_0G'_0) \oplus C_0$
 $C_1 = (C'_0G'_0 + P'_0)'$ as defined in part (a)

4.27

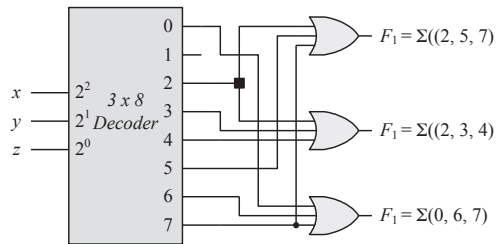


4.28 (a)

$$F_1 = x(y + y')z + x'y'z' = xyx + xy'z + x'y'z' = \Sigma(2, 5, 7)$$

$$F_2 = xy'z' + x'y = xy'z' + x'y'z + x'y'z' = \Sigma(2, 3, 4)$$

$$F_3 = x'y'z' + xy(z + z') = x'y'z' + xyz + xyz' = \Sigma(0, 6, 7)$$



(b)

4.30

Inputs								Outputs			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z	V
0	0	0	0	0	0	0	0	x	x	x	0
1	0	0	0	0	0	0	0	0	0	0	1
x	1	0	0	0	0	0	0	0	0	1	1
x	x	1	0	0	0	0	0	0	1	0	1
x	x	x	1	0	0	0	0	0	0	1	1
x	x	x	x	1	0	0	0	0	1	0	1
x	x	x	x	x	1	0	0	0	1	0	1
x	x	x	x	x	x	1	0	0	1	0	1
x	x	x	x	x	x	x	1	0	1	1	1

If $D_2 = 1$, $D_6 = 1$, all others = 0
 Output $xyz = 100$ and $V = 1$

4.31

