DIGITAL DESIGN COEN 312	Instructor: Drs. A. J. Al-Khalili & M. Nekili
Final exam. May 2000	Time Allowed 3:00 hrs.
No. of pages: 2	
No Calculators, books or notes are allowed	

Question 1

a) Consider the circuit given in Fig. 1 below. Assume each gate, including the inverter has a 12 ns t_{pd}. The inputs are currently POR = 111. How does the OUT responds when Q makes a sudden change from HI to LO.
b) A safe has 20-button keyboard. In order to unlock the safe, a teller must simultaneously press buttons 2,7,8,13, and 19. If extra buttons are pressed at the same time, the safe will not unlock. When a button is pressed, it can send a HI output to a logic circuit. Design a combinational circuit where HI output will represent the unlocked safe. Assume you have independent access to each digitized key.
c) Prove the De Morgan Theorem.

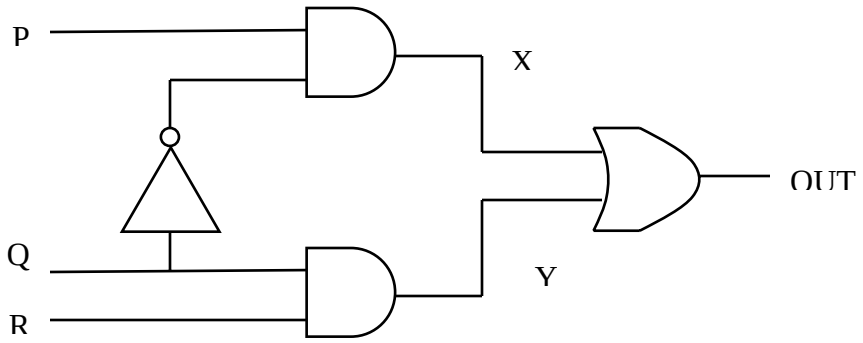


Fig. 1 Circuit for timing Analysis of Q.1a

Question 2

a) Design a full subtractor
b) Implement a) above using 4→1 Multiplexers and minimal extra logic if required.
c) Implement a) above using 3→8 decoder and minimal extra logic if required

Question 3

a) What size of ROM is required to implement a BCD to 7-segment decoder.
b) Design a BCD to 7-segment decoder. Given the content of the Rom IN A TABLE FORMAT. With each word as, abcdefg. Please refer to Fig. 2 below for the segment's destination. Assume that the illegal numbers will be displayed as E.

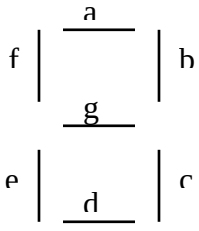


Fig. 2. 7-Segment Display of Q3

Question 4

a) Design an adder that can add two BCD numbers.
b) Give a circuit Diagram

Question 5

An engine needs to go through four strokes, all of equal duration.
On the 1st stroke the inlet valve opens and outlet valve is closed.
On the 2nd stroke the valve is closed.
On the 3rd stroke a spark is delivered.
On the 4th stroke the outlet valve is opened for the exhaust to vent.
Then the first stroke comes again and the cycle repeats.

Design a controller for the system with a clock for the input and with 3 outputs:
O1 to open inlet
O2 to open outlet
O3 to ignore spark
Assume that if the control to open a valve is not asserted the valve closes (ie. Spring loaded).

Question 6

a) Analyze the circuit given in Fig. 3 below fully (give excitation equations, transition table, state table and state diagram):
b) Initially Do has been set to "1" (for one clock period). Draw the timing diagram for y0, y1, y2 for 5 clock cycles. Assume each Flip flop has a delay of 10 ns.

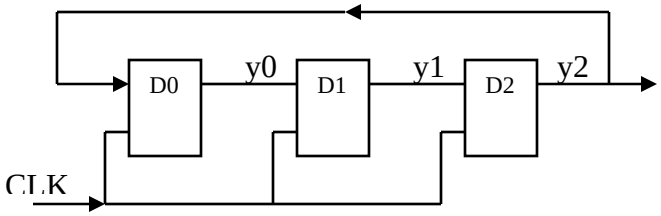
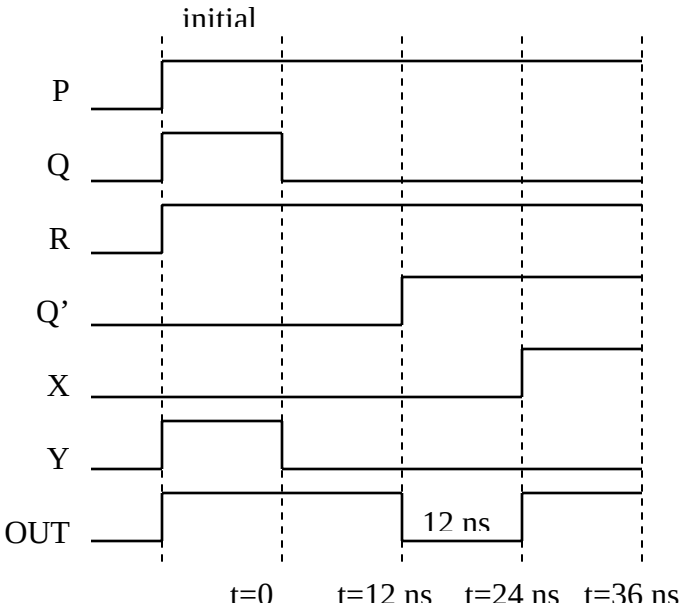


Fig. 3. Circuit to be analyzed in Q.6.

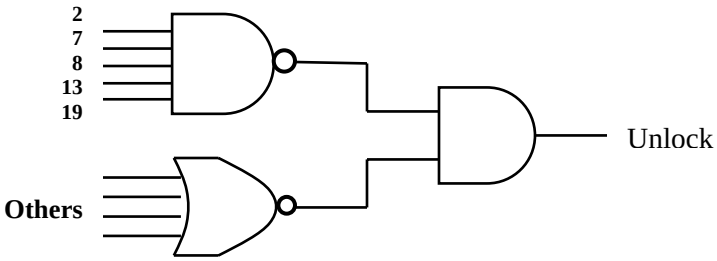
Solutions

Question 1

a)



b)



c) (A.B)' = A' + B' By Truth Table

A	B	A.B	(A.B)'	A'	B'	A' + B'
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

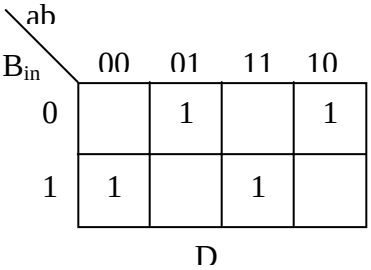
Equal

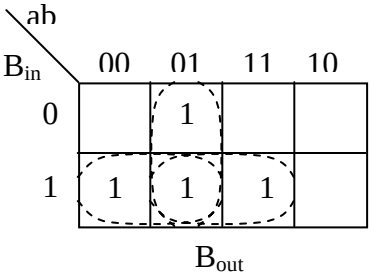
Question 2

a) $B_{out} = a'B_{in} + a'b + bB_{in}$

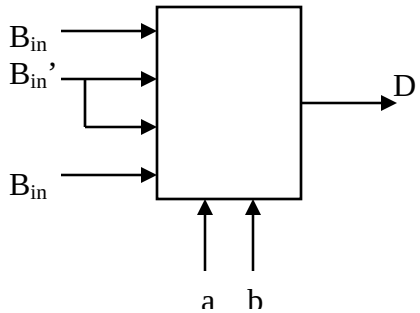
$D = a \oplus b \oplus B_{in}$

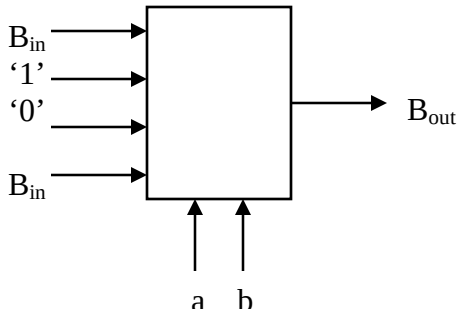
a	b	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



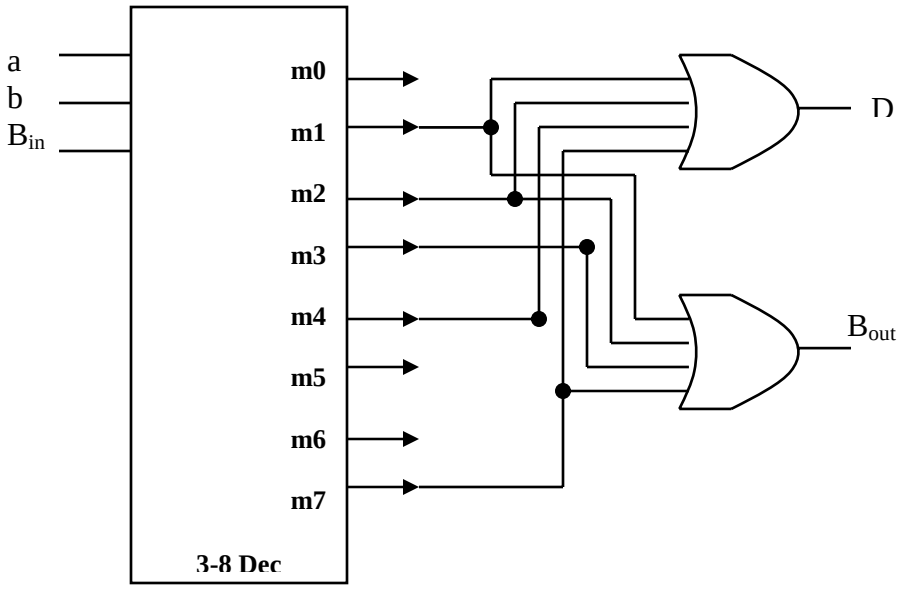


b)





c)



Question 3

a) 10 words of 7 bits = 70 bits with error bits

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1
E	1	0	1	0	1	0	0	1	1	1	1
	1	0	1	1	1	0	0	1	1	1	1
	1	1	0	0	1	0	0	1	1	1	1
	1	1	0	1	1	0	0	1	1	1	1
	1	1	1	0	1	0	0	1	1	1	1
	1	1	1	1	1	0	0	1	1	1	1

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	1	1	1
11	1	1	1	1
10	1	1	1	1

a = B + C +BD +B'D'

CD \ AB	00	01	11	10
00	1	1	0	1
01	1	0	0	1
11	1	1	0	0
10	1	0	0	0

b = (A' + B')(A' + C')(B' + C' + D)

CD \ AB	00	01	11	10
00	1	1	0	1
01	1	1	0	1
11	1	1	0	0
10	0	1	0	0

c = (A' + B')(A' + C')(B + C' + D)

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	1	1	0
11	1	0	1	1
10	1	1	1	1

d = (A + B' + C + D)(A + B + C + D)
(A + B' + C' +D')

CD \ AB	00	01	11	10
00	1	0	1	1
01	0	0	1	0
11	0	0	1	1
10	1	1	1	1

e = (A + C)(A + B' + C)(B + C + D')

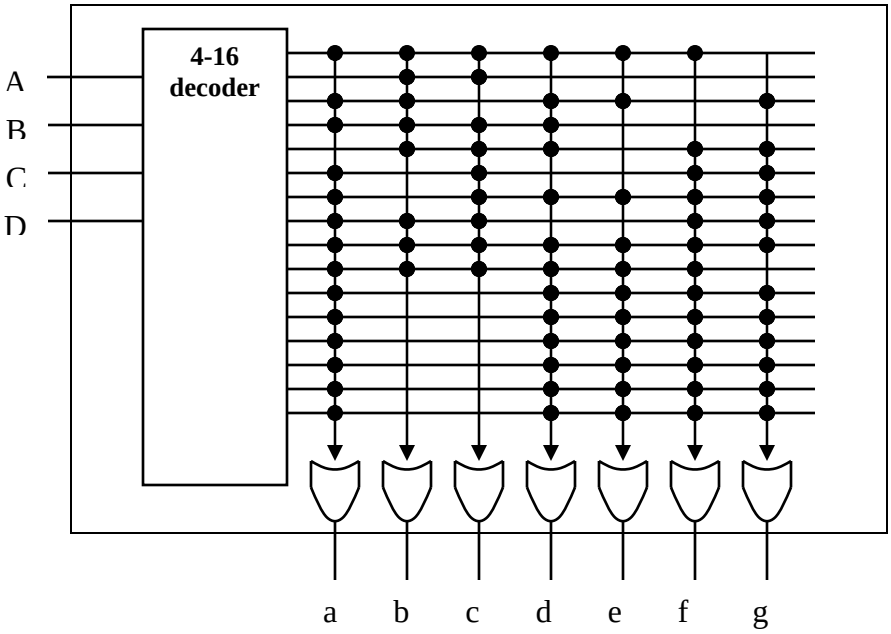
CD \ AB	00	01	11	10
00	1	1	1	1
01	0	1	1	1
11	0	0	1	1
10	0	1	1	1

f= (A + B + D')(A + B + C)(A + C' + D')

CD \ AB	00	01	11	10
00	0	1	1	1
01	0	1	1	1
11	1	0	1	1
10	1	1	1	1

g = (A + B + C)(A + B' + C' + D')

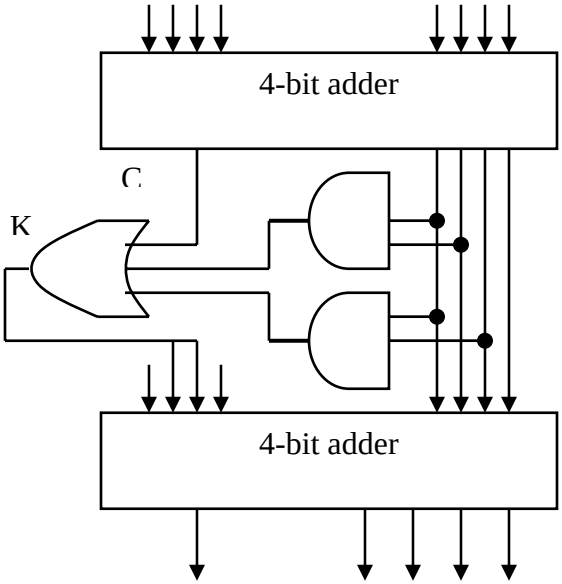
ROM Implementation:



Question 4

Adding two BCD numbers, give a maximum of 19, i.e 9 + 9 + 1 = 19.

Decimal	K	A B C D (BCD)	C	X3 X2 X1 X0 (Binary)
0	0	0 0 0 0	0	0 0 0 0
1	0	0 0 0 1	0	0 0 0 1
2	0	0 0 1 0	0	0 0 1 0
3	0	0 0 1 1	0	0 0 1 1
4	0	0 1 0 0	0	0 1 0 0
5	0	0 1 0 1	0	0 1 0 1
6	0	0 1 1 0	0	0 1 1 0
7	0	0 1 1 1	0	0 1 1 1
8	0	1 0 0 0	0	1 0 0 0
9	0	1 0 0 1	0	1 0 0 1
10	1	0 0 0 0	0	1 0 1 0
11	1	0 0 0 1	0	1 0 1 1
12	1	0 0 1 0	0	1 1 0 0
13	1	0 0 1 1	0	1 1 0 1
14	1	0 1 0 0	0	1 1 1 0
15	1	0 1 0 1	0	1 1 1 1
16	1	0 1 1 0	1	0 0 0 0
17	1	0 1 1 1	1	0 0 0 1
18	1	1 0 0 0	1	0 0 1 0
19	1	1 0 0 1	1	0 0 1 1

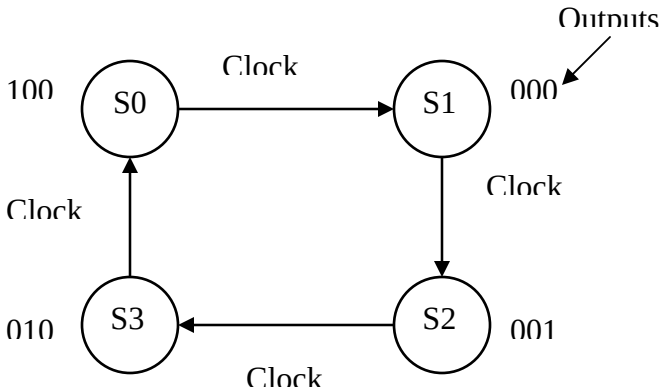


It can be seen that from 0-9 the two additions are equal. For numbers greater than 9, we had add a 6 (0110) to the binary addition to get the BCD addition.

From above Truth Table, we have:
K = C + X3X2 +X3X1.

Question 5

There are four states, are for each stroke, output are O1 O2 O3.



This is a simple counter S0→S1→S2→S3→S0→…

Present state		Next state		Outputs		
y0	y1	$y0^+$	$y1^+$	O1	O2	O3
0	0	0	1	1	0	0
0	1	1	0	0	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0

Use D FlipFlop

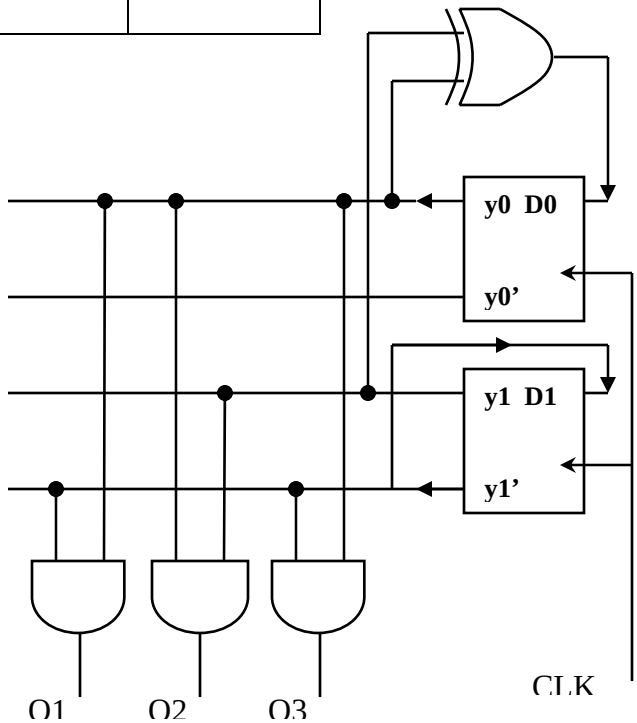
$y0^+ = D0 = y0 \oplus y1$

$y1^+ = D1 = y1'$

$O1 = y0'y1'$

$O2 = y0y1$

$O3 = y0\ y1'$



Question 6

a) Excitation Equations

$y0^+ = D0 = y2$

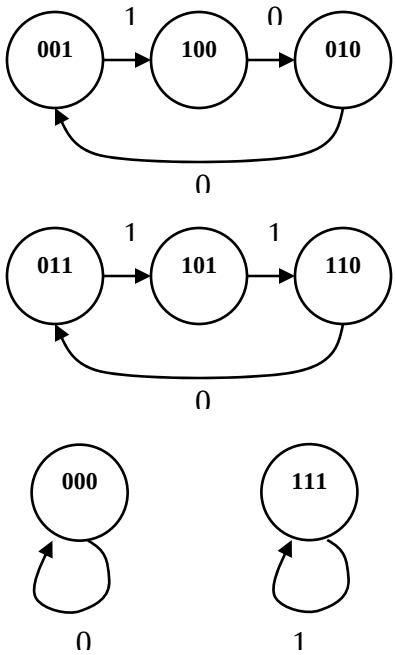
$y1^+ = D1 = y0$

$y2^+ = D2 = y1$

Output = Z = y2

Transition Table and State Table

Present State y0 y1 y2	Next state $y0^+$ $y1^+$ $y2^+$	Output Z
0 0 0	0 0 0	0
0 0 1	1 0 0	1
0 1 0	0 0 1	0
0 1 1	1 0 1	1
1 0 0	0 1 0	0
1 0 1	1 1 0	1
1 1 0	0 1 1	0
1 1 1	1 1 1	1



State Diagram

Timing Diagram