Digital Design COEN 312 Instructors: A.J. Al-Khalili & M. Nekili
Final, May 2000 Time allowed 3:00 hrs
No. of pages: 2

No Calculators , books or notes are allowed.

Question1.

a) Consider the circuit given in Fig.1 below. Assume each gate, including the inverter has a 12ns t_{pd}. The inputs are currently PQR=111. How does the OUT responds when Q makes a sudden change from HI to LO.

b) A safe has 20-button keyboard. In order to unlock the safe, a teller must simultaneously press buttons 2,7,8,13,and 19. If extra buttons are pressed at the same time, the safe will not unlock. When a button is pressed, it can send a HI output to a logic circuit. Design a combinational circuit where HI output will represent the unlocked safe. Assume you have independent access to each digitized key.

c) Prove the De Morgan Theorem.

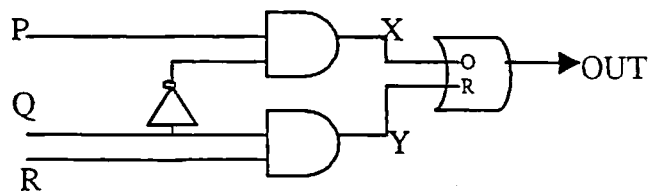

Fig. 1. Circuit for timing Analysis of Q.1a

Question2.

a) Design a full subtractor

b) Implement a) above using 4→1 Multiplexers and minimal extra logic if required.

c) Implement a) above using 3→8 decoder and minimal extra logic if required.

Question3.

a) What size of ROM is required to implement a BCD to 7- segment decoder.

b) Design a BCD to 7-segment decoder. Give the content of the ROM in a table format. With each word as , abcdefg. Please refer to Fig.2 below for the segment's designation. Assume that the illegal numbers will be displayed as E.

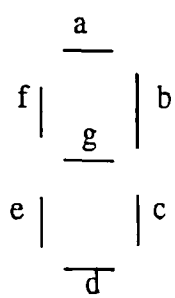

Fig.2. 7-Segment Display of Q3.

Question4.

a) Design an adder that can add two BCD numbers.
b) Give a circuit Diagram.

Question5.

An engine needs to go through four strokes, all of equal duration.
On the 1st stroke the inlet valve opens and the outlet valve is closed.
On the 2nd stroke the valve is closed.
On the 3rd stroke a spark is delivered.
On the 4th stroke the outlet valve is opened for the exhaust to vent.
Then the first stroke comes again and the cycle repeats.

Design a controller for the system with a clock for the input and with 3 outputs:
O1 to open inlet
O2 to open outlet
O3 to ignite spark.
Assume that if the control to open a valve is not asserted the valve closes (ie. spring loaded).

Question 6.

a) Analyze the circuit given in Fig.3 below fully(give excitation equations, transition table, state table and state diagram):
b)Initially Do has been set to "1"(for one clock period). Draw the timing diagram for y0,y1,y2 for 5 clock cycles. Assume each Flip Flop has a delay of 10 ns.

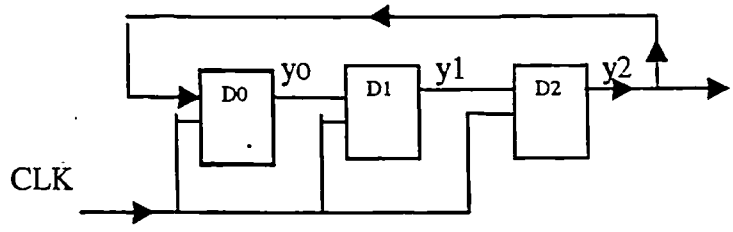

Fig. 3. Circuit to be analyzed in Q.6.

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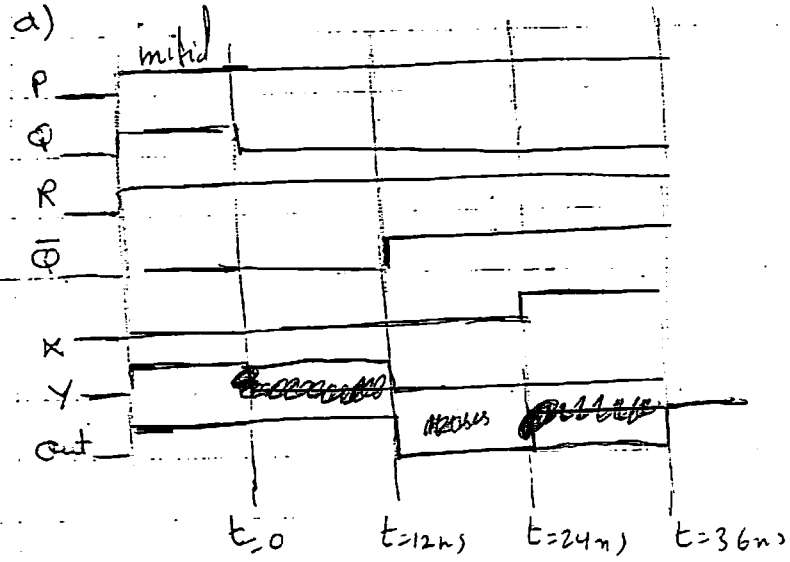
Q1

a)



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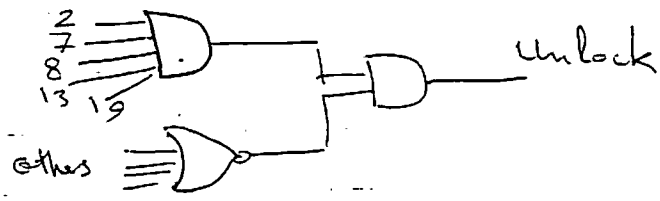
b)



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c)

$\overline{A \cdot B} = \bar{A} + \bar{B}$ — By Truth Table.

A	B	A·B	$\overline{A \cdot B}$	$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}$
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

Equal

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Q2

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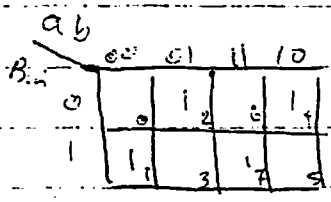
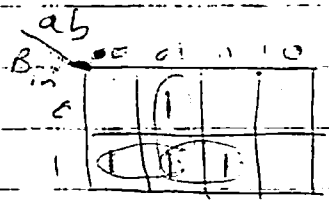
a)

a	b	B_{in}	D	B_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

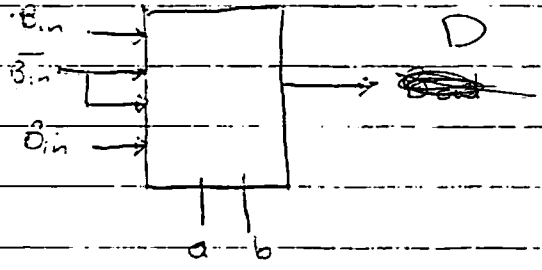


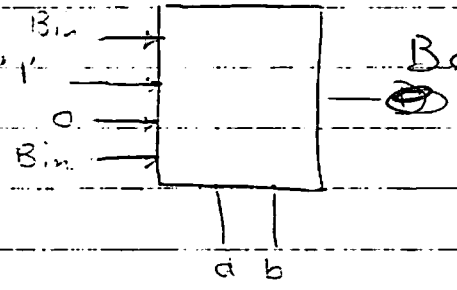


$B_{out} = \bar{a} B_{in} + \bar{a} b + b B_{in}$

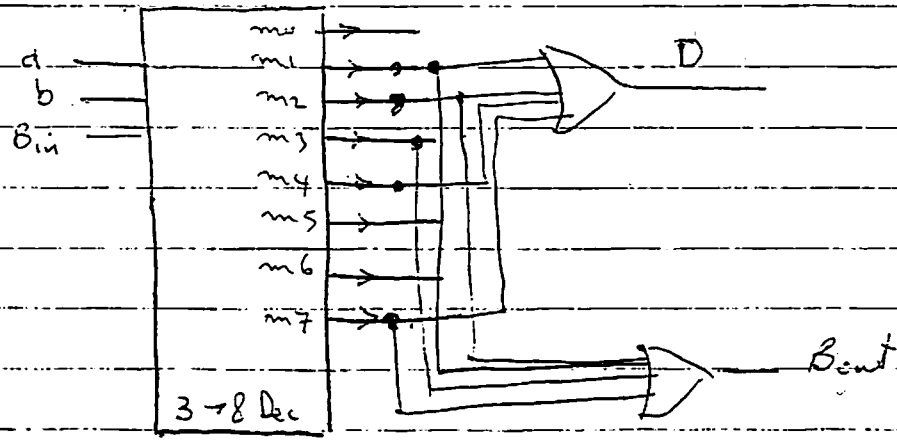
$D = a \oplus b \oplus B_{in}$

b)





c)



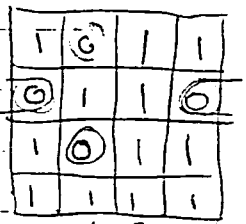
Q3

5th May, 2000

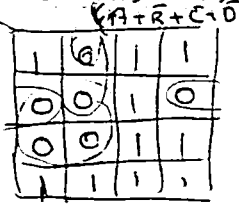
a) 10 words of 7 bits = 70 bits with error bits

b)

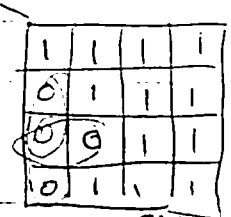
Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1
E	1	0	1	0	0	0	0	1	1	0	1
E	1	0	1	1	0	0	1	1	0	0	0
E	1	1	0	0	0	1	0	1	0	1	0
E	1	1	0	1	1	0	0	0	1	1	0
E	1	1	1	0	0	0	0	0	0	0	0
E	1	1	1	1	0	0	0	1	1	1	0



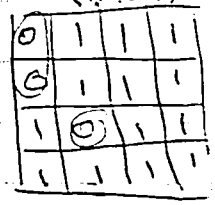
$d = (A+\bar{B}+C+D)(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+\bar{D})$



$e = (A+C)(A+\bar{B}+$
$(B+C+\bar{D})$

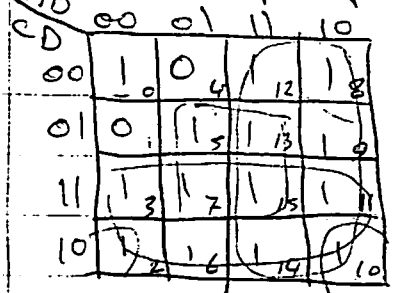


$f = (A+B+\bar{D})(A+B+$
$(A+\bar{C}+D)$

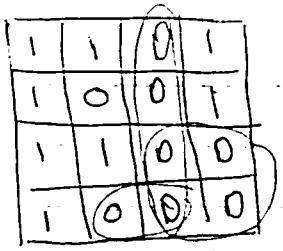


$g = (A+B+C)($
$(A+\bar{B}+\bar{C}+\bar{D})$

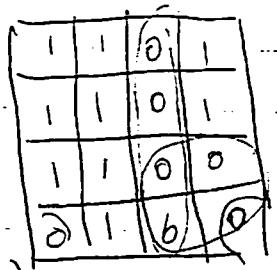
As an example of the design then d is



$d = B + C + BD + \bar{B}\bar{D}$

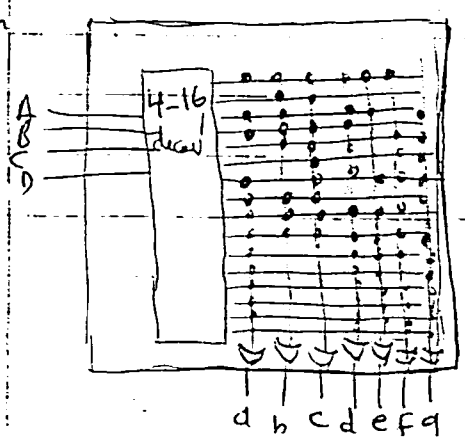


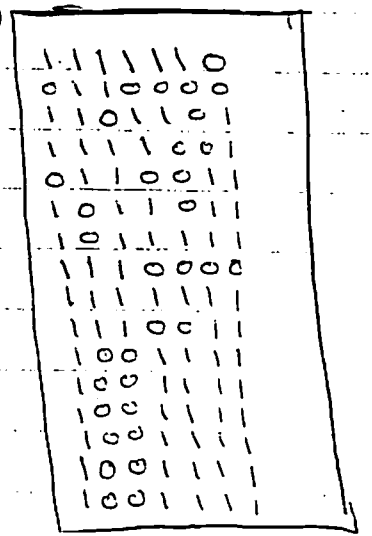
$b = (\bar{A}+\bar{B})(\bar{A}+\bar{C})(\bar{B}+\bar{C}+D)$



$c = (\bar{A}+\bar{B})(\bar{A}+\bar{C})(B+\bar{C}+D)$

c) ROM Implementation





Q4 May 5, 2000

Adding two BCD numbers gives a maximum of 19

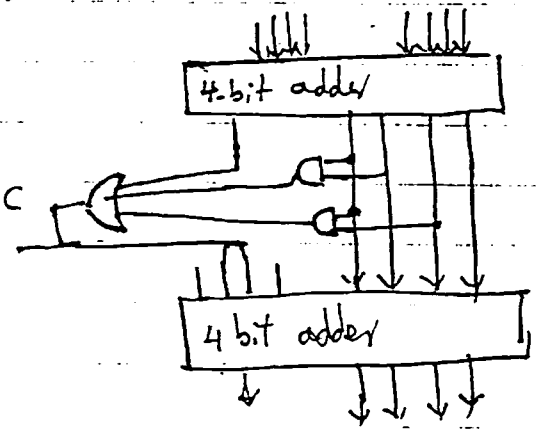
i.e. $9 + 9 + 1 = 19$

Decimal	K	A B C D (BCD)	C	$X_3 X_2 X_1 X_0$ (Binary)
0	0	0 0 0 0	0	0 0 0 0
1	0	0 0 0 1	0	0 0 0 1
2	0	0 0 1 0	0	0 0 1 0
3	0	0 0 1 1	0	0 0 1 1
4	0	0 1 0 0	0	0 1 0 0
5	0	0 1 0 1	0	0 1 0 1
6	0	0 1 1 0	0	0 1 1 0
7	0	0 1 1 1	0	0 1 1 1
8	0	1 0 0 0	0	1 0 0 0
9	0	1 0 0 1	0	1 0 0 1
10	1	0 0 0 0	1	0 1 0 0
11	1	0 0 0 1	1	0 1 0 1
12	1	0 0 1 0	1	0 1 1 0
13	1	0 0 1 1	1	0 1 1 1
14	1	0 1 0 0	1	1 0 0 0
15	1	0 1 0 1	1	1 0 0 1
16	1	0 1 1 0	1	1 0 1 0
17	1	0 1 1 1	1	1 0 1 1
18	1	1 0 0 0	1	1 1 0 0
19	1	1 0 0 1	1	1 1 0 1

It can be seen that from 0 → 9 the two additions are equal for numbers greater than 9 we had add a 6 (0110) to the binary addition to get the BCD addition

From above Truth Table we have:

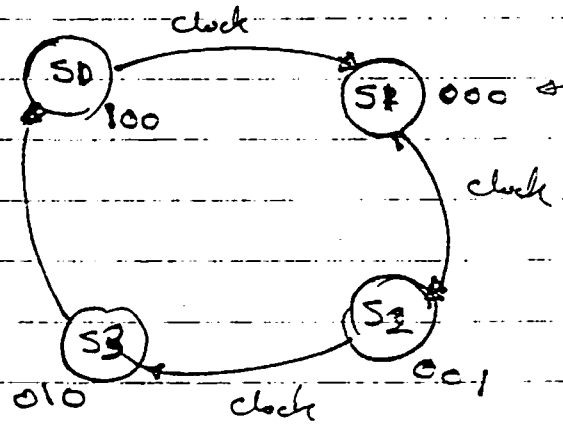
$$K = C + X_3 X_2 + X_3 X_1$$



Q5 May 5, 2000

There are four states, one for each stroke,

outputs are O1 O2 O3



This is a simple counter $S_0 \rightarrow S1 \rightarrow S2 \rightarrow S_3 \rightarrow S_0 \rightarrow \cdots$

Present state		Next State		Outputs		
y_0	y_1	y_0^+	y_1^+	O_1	O_2	O_3
0	0	0	1	1	0	0
0	1	1	0	0	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0

Use D Flip Flop

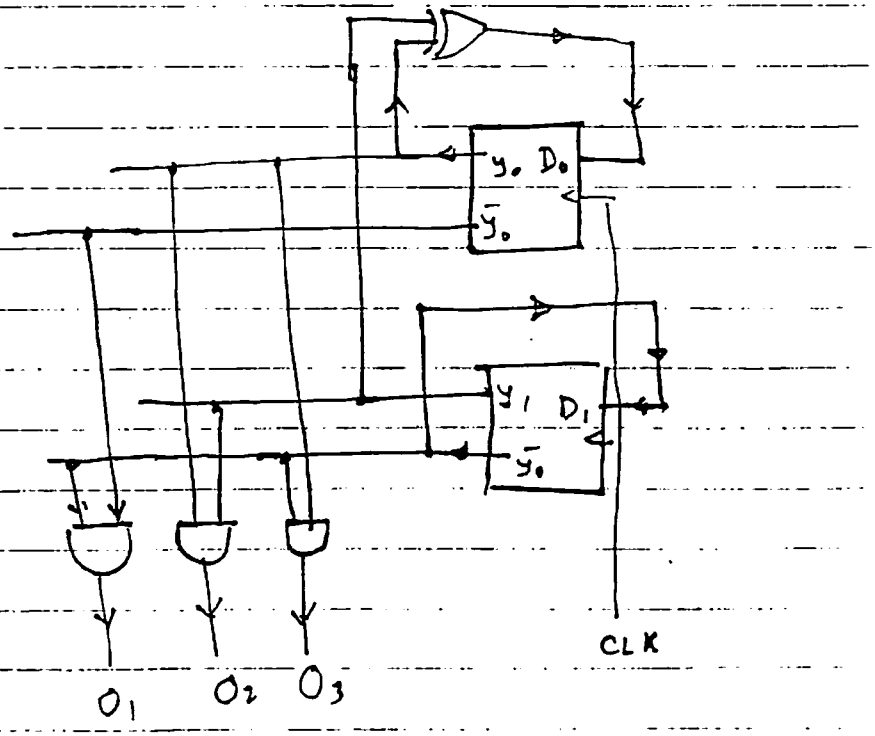
$y_0^+ = D_0 = y_0 \oplus y_1$

$y_1^+ = D_1 = \bar{y}_1$

$O_1 = \bar{y}_0 \cdot \bar{y}_1$

$O_2 = y_0 \cdot y_1$

$O_3 = y_0 \cdot \bar{y}_1$



Q6

May 5th, 2000

a)

Excitation Equations

$Y_0^+ = D_0 = Y_2$

$Y_1^+ = D_1 = Y_0$

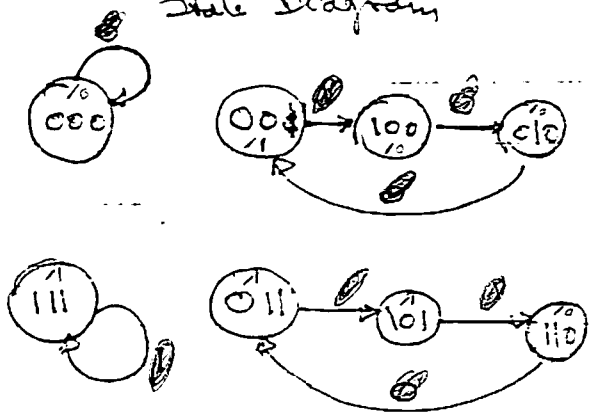
$Y_2^+ = D_2 = Y_1$

Output $= Z = Y_2$

Transition Table and State Table

Present State			Next State			output
Y_0	Y_1	Y_2	Y_0^+	Y_1^+	Y_2	Z
0	0	0	0	0	0	0
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	1	1	0
1	1	1	1	1	1	1

State Diagram



Timing Diagram