COEN 312 DIGITAL DESIGN Lecturers: A.J. Al-Khalili, M. Nekili,
Final April 29, 2002 C. Taillefer, K. Nayan
Answer all questions Time allowed 3:00 hours
No calculators, notes or books are allowed

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Question 1:

a) Using Boolean Algebra, minimize the following functions (step by step):
i) **F= A' + AB** ; ii) **F=(A'+B)(A+B').**; iii) **F=BC + AC + A'B'C** (3 marks)

b) List all possible **prime implicants** and **essential prime implicants** for the function **F** = $\sum$**(0, 2, 4, 5, 8, 12, 13, 15)** with don't care conditions **d** = $\sum$**(1, 3, 14)**. Show groupings on a **Karnaugh map** accompanied with their algebraic forms. (4marks)

c) Express P and Q in Figure 1 as functions of A, B and C and then simplify them. (3 marks)

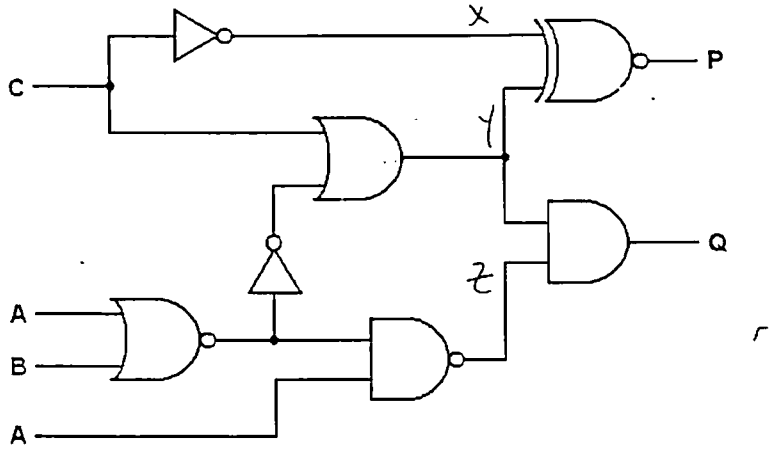

Figure 1

Question 2:

2.1 Use **DeMorgan's** theorem to express the equivalence function
F= xy + x'y' with:
i) **NAND** only. ii) **NOR** only.
Show the different steps and the logic diagram. (4 marks)

2.2 Consider the circuit in Fig. 2. Draw the **timing diagram** of F when inputs A, B and C go from 000 to 111 (binary counting) assuming each gate has a propagation delay of 10ns. (4 marks). Assume F is initially 0.

Determine the minimum time between two input changes, for the circuit to operate properly. To help, you may add intermediate nodes to the timing diagram. (2 mark)

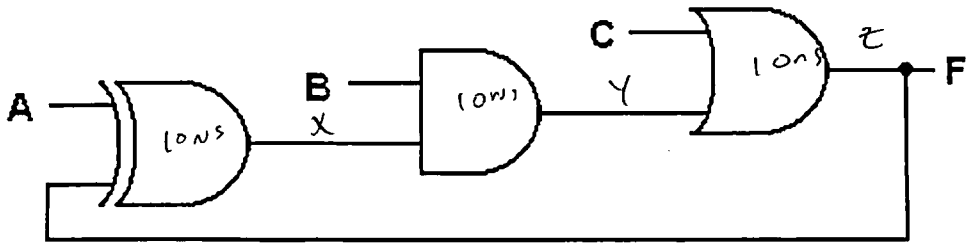

Figure 2

Question 3:

a) A Function F, can be approximated by $F= at^2 + b$ where a=2, b= 1 and t is 2-bit binary input that can take a value of 0,1or 2 only. Design and implement the circuit. (4 Marks)

b) Design a 4-bit Binary Squarer.(ie the circuit has one input $A=a_3a_2a_1a_0$ and the output is the A^2). (6 Marks)

Question 4:

a) What is the difference between ROM, PROM, PAL, and the PLA. (2 Marks)

b) A sequential circuit is to be implemented using **2 JK Flip Flops and a PLA**. The excitation equations are:

$J_A= Bx'$ $K_A = Bx$

$J_B = x$ $K_B = (A \oplus x)$

Where A and B are the present states and x is an external input. Implement the circuit, giving PLA personality matrix (programming table) and showing your programming of the PLA clearly by placing an • on the programmable nodes. (5 Marks)

c) Implement the following function F, using only 2 to 1 multiplexers:

$F= AB + CD$ (3 Marks)

Question 5:

As an engineer, you have been contracted by the ACME Candy Corporation to design the control circuitry for a 15-cent candy bar machine. The machine accepts only nickels (5-cents) and dimes (10-cents). There will be two inputs to your control system: ***N*** and ***D***. When a nickel is put into the machine, the input signal ***N*** is asserted high. When a dime is inserted in the machine, the input signal ***D*** is asserted high. The control unit must be a synchronous sequential circuit. You may assume that the inputs (***N*** and ***D***) will be logic high for exactly one clock period.

The control unit will produce two outputs. When 15-cents or more is placed into the machine, an output ***CB*** (*C*andy *B*ar) will be set to logic 1 and the unit will return to idle state. When more than 15-cents (i.e. 20-cents,) has been deposited into the machine, a signal ***CH*** (*Ch*ange) will be asserted to return (Change) to the vendor and the unit will return to idle state waiting for the next transaction.

The ACME Candy Corporation requires that you construct the control unit using only D-type flip-flops and any other combinational logic.

It is not physically possible for the ***N*** and ***D*** inputs to be '1' at the same time. However, if this ever occurs your system must return to the "initial" state. Furthermore, an active low reset should be incorporated into your system at the circuit level, resetting to the "initial" state. (10 Marks)

1) Draw the State Transition Diagram for the candy bar control unit.

2) Derive the State Transition Table.

3) Draw the sequential circuit diagram.

Question 6:

Analyze the circuit shown in Figure 3. Derive the state transition table and diagram including all inputs and outputs. (10 Marks)

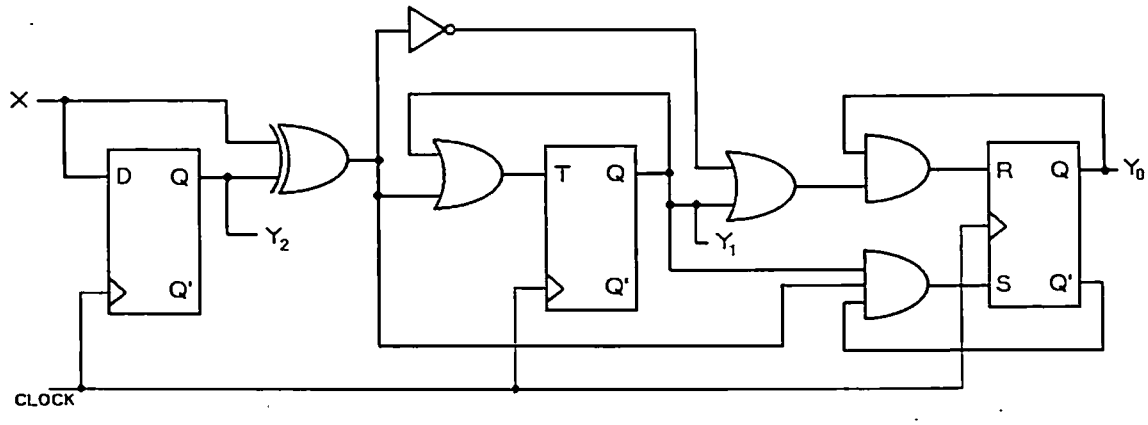

Figure 3

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winter 2002
Dr. Nekili

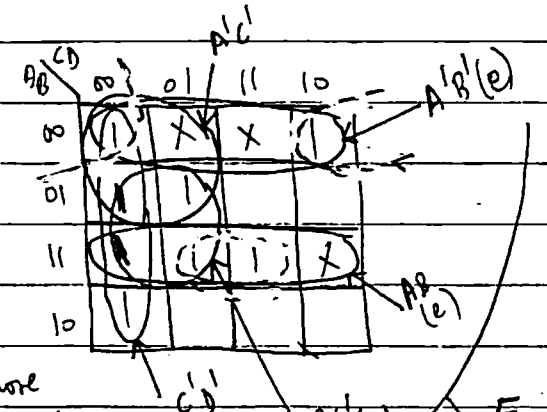
Question #1,

a/ i/ $F = A' + AB = (A'+A)\cdot(\bar{A}+B) = 1\cdot(\bar{A}+B) = \bar{A}+B$ (1/1)

ii/ $F = (A'+B)(A+B') = A'A + BA + B'A' + BB' = AB + A'B'$ (1/1)

iii/ $F = BC + AC + A'B'C = C(B + A + \bar{A}\bar{B}) = C(B+A+\bar{B}) = C(A+(B+\bar{B})) = C$ (1/1)

b/



map: (1/1) (minterms & X correct)

grouping: 1/1 (graphical)

Algebraic P.I.: 1/1

essentials: 1/1

may be more essentials depending on function coverage of P.I.

5 posible P.I. + 2 possible P.I if X=0

4 Essential PI (AB, $\bar{A}\bar{B}$, $\bar{C}\bar{D}$, $B\bar{C}$)

c/ $P = [(A+B+C)\odot\bar{C}]$ (0.5/0.5)

$= [(AB+C)\cdot\bar{C} + A+B+C]'$

$= [AC+BC+C+\bar{A}\bar{B}\bar{C}]'$ (1/1)

$= [(A+B+1)C + \bar{A}\cdot\bar{B}\cdot\bar{C}]'$

$= [C + \bar{A} + B\cdot\bar{C}]'$ (use K-map or absorption)

$= (C + \bar{A}\bar{B})'$

$= (A+B)\cdot C'$

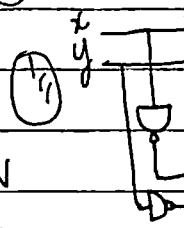
same for $Q = A+B+C$.

Question #2,

2.1 $F = xy + x'y' = [xy + x'y']'' = [(xy)' + (x'y')']'$ (1/1)

NAND NAND

NAND



logic diagram alone = 0

→ use of DEMORGAN important (not optional)

→ graphic method not accepted.

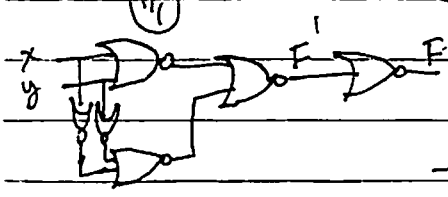
$F = xy + x'y' = [(x'+y')\cdot(x+y)]'$

$= (x'+y')' + (x+y)'$ (1/1)

→ # $F' = [(x'+y')' + (x+y)']'$

NOR NOR

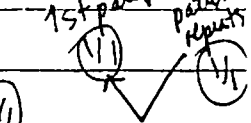
NOR



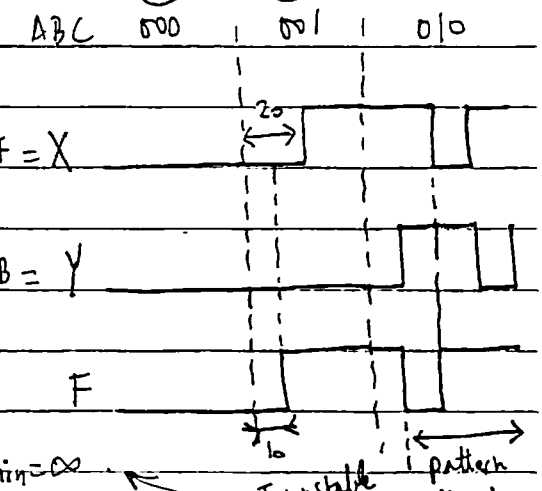
(1/1)

→ F = NOR(F, F)

marking scheme



2.2



(2/2) $t_{min} = \infty$ F unknown for rest of combinat. F unstable

1.3 d

t	F
t_1 t_0	F_3 F_2 F_1 F_0
0 0	0 0 0 0
0 1	0 0 1 1
1 0	1 0 0 1
1 1	X X X X

F_minimum value = 0

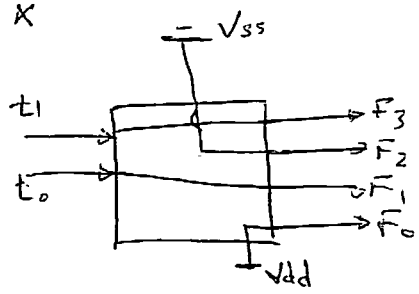
F_maximum value = 9 4 binary bits

$F_0 = 1$

$F_1 = t_0$

$F_2 = 0$

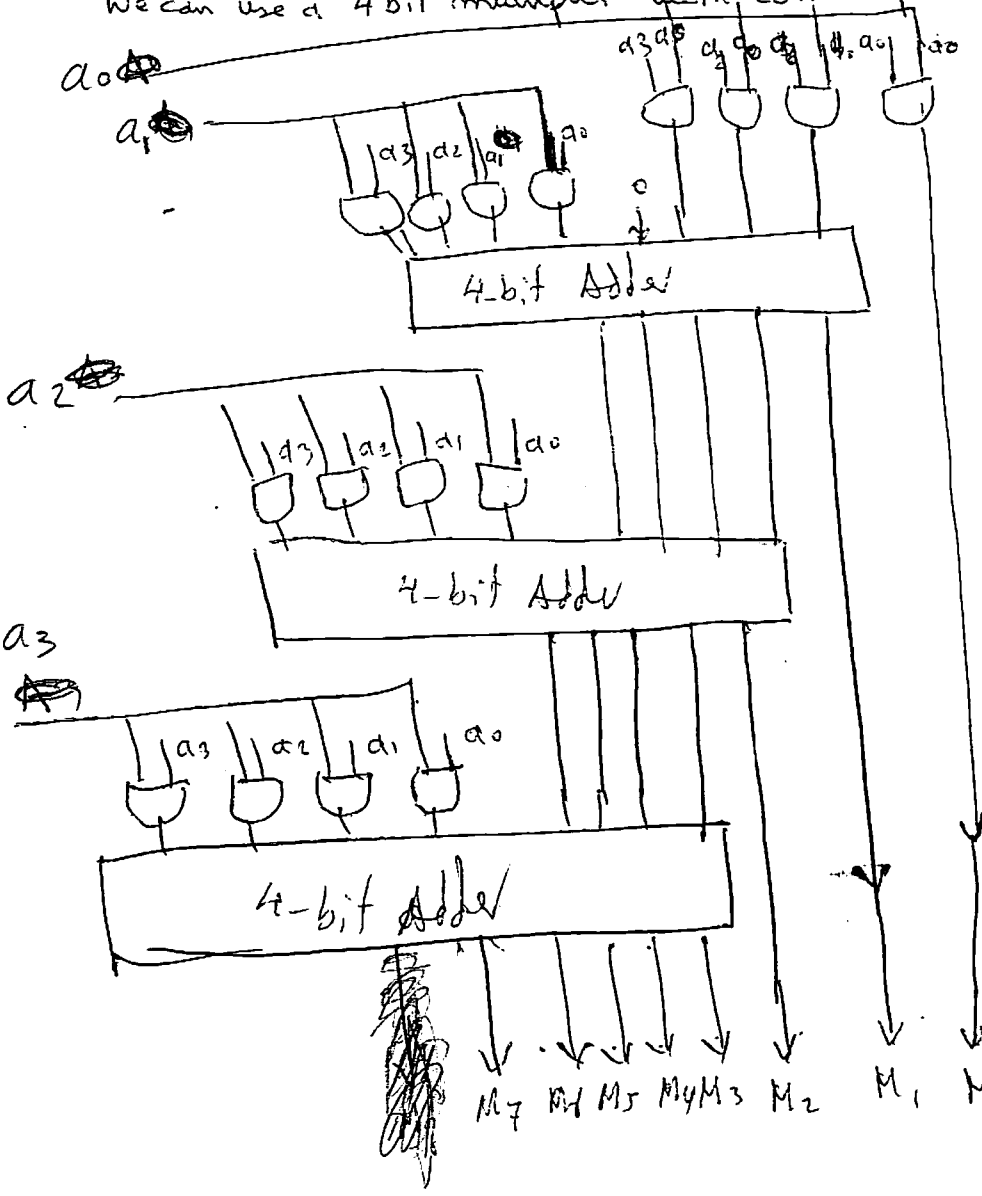
$F_3 = t_1$



4 - marks

Q3b

We can use a 4 bit multiplier with both input connected as A



6 mark

Q4

a)

	AND gate	OR gate
ROM	Fixed	Fixed
PROM	Fixed	Programmable
PAL	Programmable	Fixed
PLA	Programmable	Programable

2 Marks

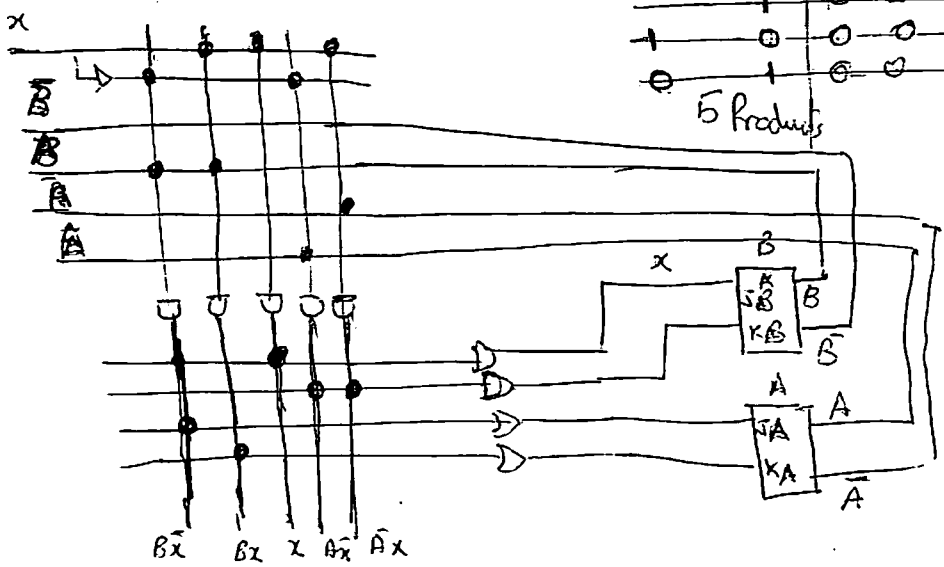
Q4 b)

$J_A = Bx'$ $K_A = Bx$

$J_B = x$ $K_B = (A \oplus x)$

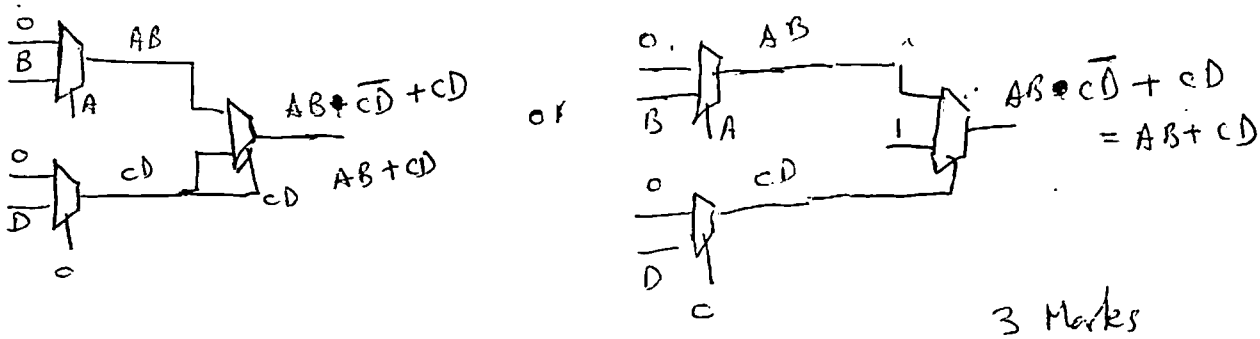
A	B	x	J_A	K_A	J_B	K_B
0	0	1	1	0	1	0
0	1	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	1
1	1	1	0	0	0	1

5 Products



5 Marks

Q4c)



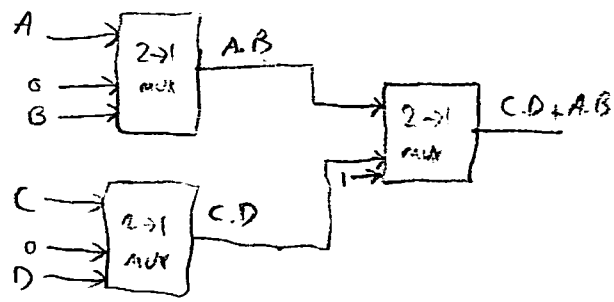
3 Marks

Using the technique discussed in the class:

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

0

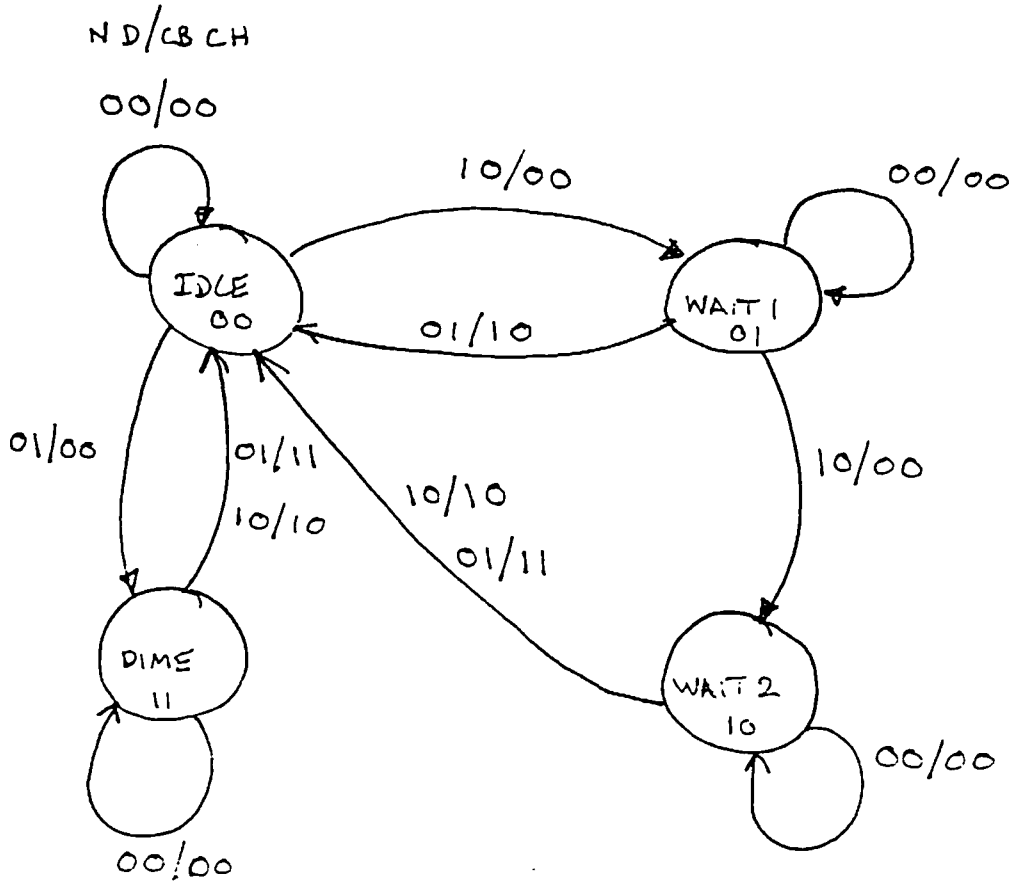
B



AB	C.D	A.B + C.D
0	0	0
0	1	1
1	0	1
1	1	1

C.D

1

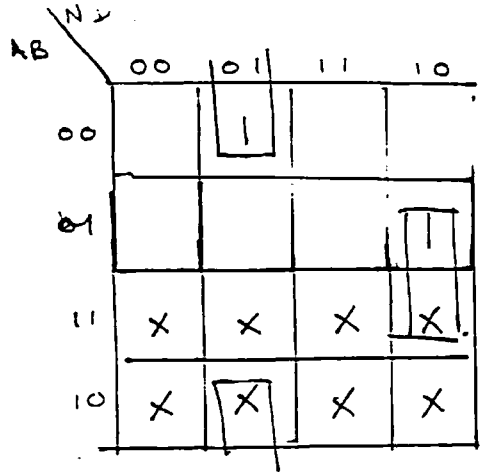


The states "DIME" and "WAIT 2" are equivalent and one can reduce the model by removing one of them.

This can also be seen from the table, although intuitively one can conclude that.

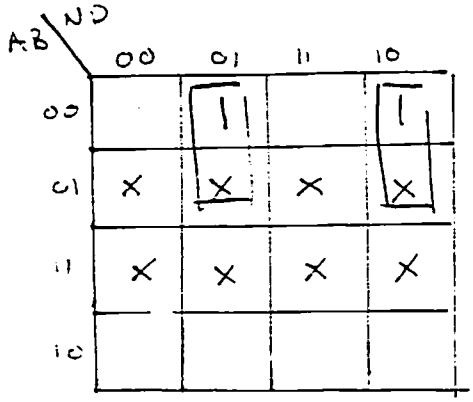
PRESENT STATES		INPUTS		NEXT STATES		FF INPUTS				OUTPUTS	
A	B	N	D	A(t+1)	B(t+1)	JA	KA	JB	KB	CB	CH
0	0	0	0	0	0	0	X	0	X	0	0
0	0	0	1	1	1	1	X	1	X	0	0
0	0	1	0	0	1	0	X	1	X	0	0
0	0	1	1	0	0	0	X	0	X	0	0
0	1	0	0	0	1	0	X	X	0	0	0
0	1	0	1	0	0	0	X	X	1	1	0
0	1	1	0	1	0	1	X	X	1	0	0
0	1	1	1	0	0	0	X	X	1	0	0
1	0	0	0	1	0	X	0	0	X	0	0
1	0	0	1	0	0	X	1	0	X	1	1
1	0	1	0	0	0	X	1	0	X	1	0
1	0	1	1	0	0	X	1	0	X	0	0
1	1	0	0	1	1	X	0	X	0	0	0
1	1	0	1	0	0	X	1	X	1	1	1
1	1	1	0	0	0	X	1	X	1	1	0
1	1	1	1	0	0	X	1	X	1	0	0

JA



$JA = B'N'D + BND'$

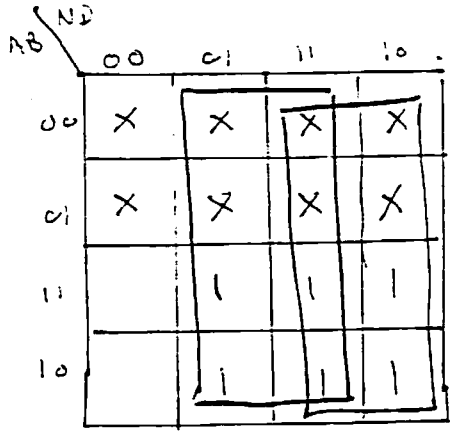
JB



$JB = A'N'D + A'ND'$

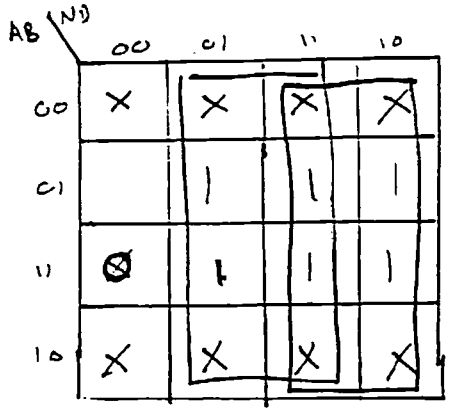
$= A' \cdot (N \oplus D)$

KA



$KA = N + D$

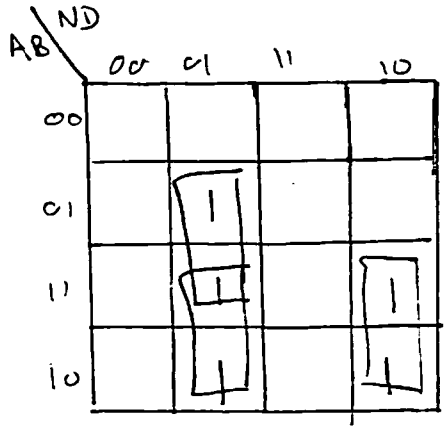
KB



$KB = N + D$

OUTPUTS:

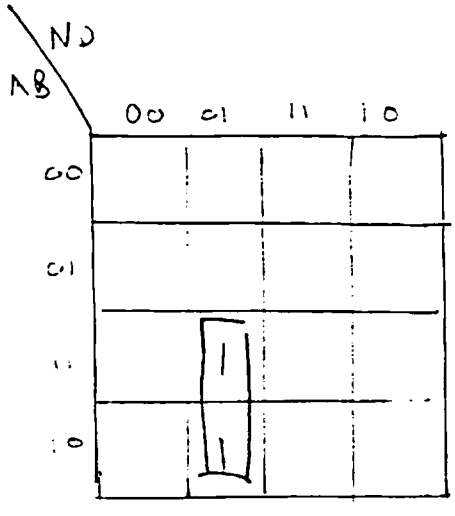
CB



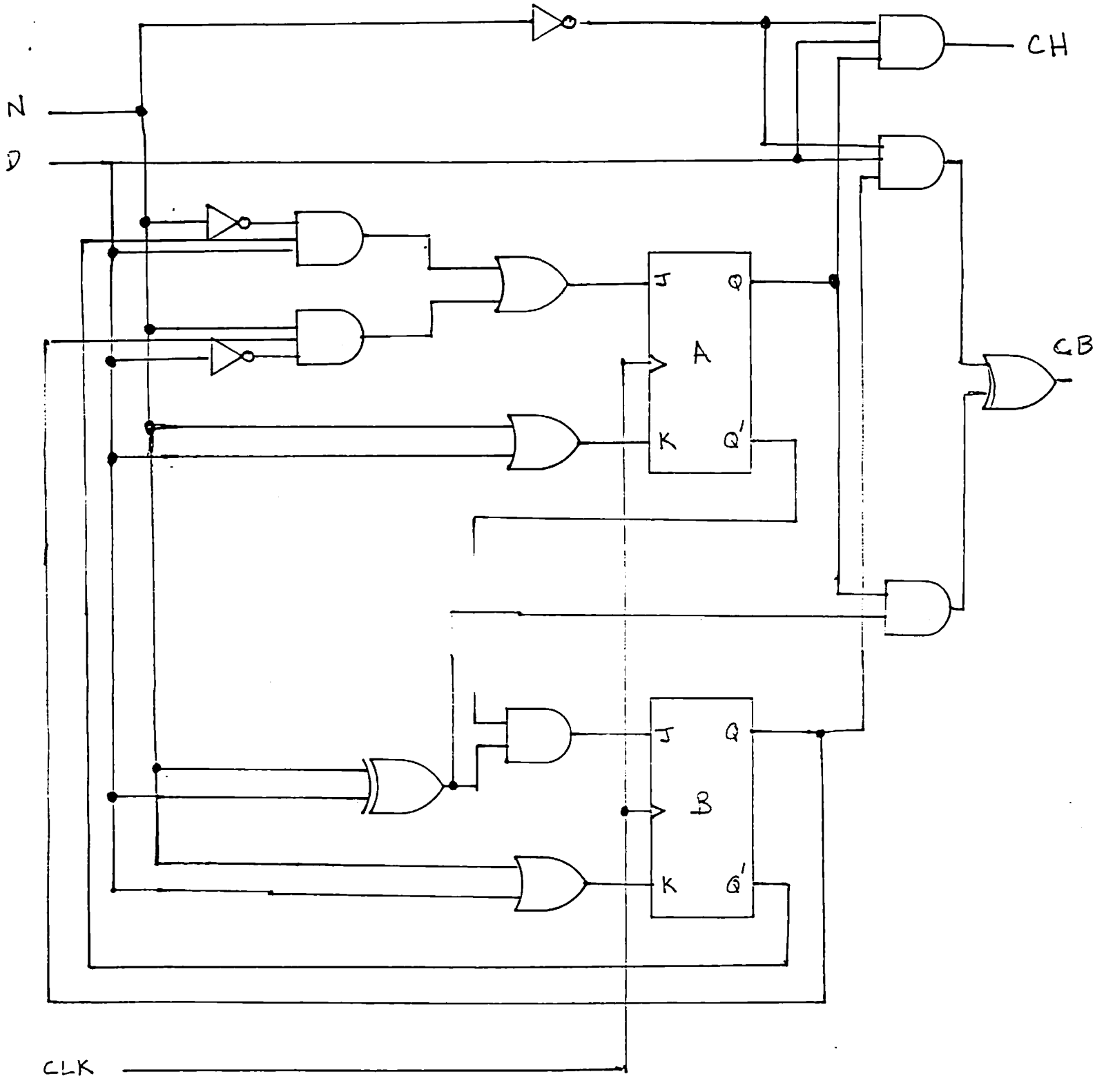
$$CB = BN'D + \overset{A}{\cancel{B}}N'D + AND'$$

$$= BN'D + A \cdot (N \oplus D)$$

CH



$$CH = AN'D$$


N
D
CH
CB
J
Q
A
K
Q'
J
Q
B
K
Q'
CLK

Q6

$$T = Y_1 + (Y_2 \oplus x)$$
$$R = Y_0 [Y_1 + (Y_2 \oplus x)']$$
$$S = Y_1 . Y_0' . (Y_2 \oplus x)$$

Present State												Next State		
Y_2	Y_1	Y_0	x	D	$Y_2 \oplus x$	$Y_1 + (Y_2 \oplus x)$ T	$(Y_2 \oplus x)'$	$Y_1 + (Y_2 \oplus x)'$	$Y_0 [Y_1 + (Y_2 \oplus x)']$ R	$Y_1 . Y_0' . (Y_2 \oplus x)$ S	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1	1	0	0	0	0	0
0	0	0	1	1	1	1	0	0	0	0	1	1	0
0	0	1	0	0	0	0	1	1	1	0	0	0	0
0	0	1	1	1	1	1	0	0	0	0	1	1	1
0	1	0	0	0	0	1	1	1	0	0	0	0	0
0	1	0	1	1	1	1	0	1	0	1	1	0	1
0	1	1	0	0	0	1	1	1	1	0	0	0	0
0	1	1	1	1	1	1	0	1	1	0	1	0	0
1	0	0	0	0	1	1	0	0	0	0	0	1	0
1	0	0	1	1	0	0	1	1	0	0	1	0	0
1	0	1	0	0	1	1	0	0	0	0	0	1	1
1	0	1	1	1	0	0	1	1	1	0	1	0	0
1	1	0	0	0	1	1	0	1	0	1	0	0	1
1	1	0	1	1	0	1	1	1	0	0	1	0	0
1	1	1	0	0	1	1	0	1	1	0	0	0	0
1	1	1	1	1	0	1	1	1	1	0	1	0	0

Outputs same as present state