

Course: Digital Systems Design	Course Number: COEN312/1	Section: CC
Examination: Final	Date: Aug. 16, 2012	Time: 3 hours
Instructor: Dr. M.R. Soleymani		
Books and Material: No material, no calculator allowed (only one crib sheet)		
Special Instructions: Try all questions.		

1) A 12-bit register contains 100101000011. What is the value of its content:

- as a 3-digit BCD number? (1 Mark)
- in Octal? (1 Mark)
- as a 12-bit (unsigned) binary number? (1 Mark)

2) Consider the following function:

$$F = (x' + y + z')(x + y')(x + z)$$

- find F' (the complement of F). (1 Mark)
- implement F' using NAND gates only. (2 Marks)
- implement F' using NOR gates only. (2 Marks)

Only non-inverted inputs are available.

3) Consider the function:

$$F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 10, 13).$$

- List all *prime implicants*. (give their expression) (2 Mark)
- List all *essential prime implicants*. (1 Mark)
- Find the minimal sum of products form for F. (2 Marks)
- Find the minimal product of sums form for F. (2 Marks)

4) Using a multiplexer design a circuit with a 4-bit input whose output is one when the input is divisible by 2 or 3 or both (5 Marks).

5) Using a decoder design a circuit whose output is $y = 3x + 5$ where x is a 3-bit input (5 Marks).

6) In the circuit shown in Figure 1, the propagation delay of the AND, OR and INVERTER gates are 3 ns., 2 ns. and 1 ns., respectively. The inputs are initially $A = B = C = 0$. Assume that at time t_0 the inputs are changed to $A = B = C = 1$. Draw the signal at different points D and E (3 Marks).

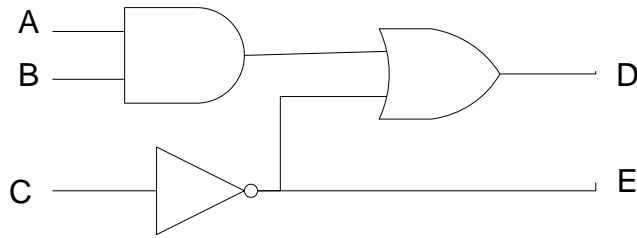


Figure 1

- 7) A sequential circuit has two JK flip-flops with the following flip-flop input equations:

$$J_A = K_A = Bx$$

$$J_B = x, K_B = A \oplus B.$$

- a. Draw the state transition table for the above circuit (4 Marks).
 - b. Draw the state diagram (3 Marks).
- 8) Using JK flip-flops design a synchronous counter that counts 0, 2, 4, 6, 1, 5, 0. Make sure that unused states are correctable (7 Marks).
- 9) Design the sequential circuit having the following state diagram using D flip-flops (5 Marks).

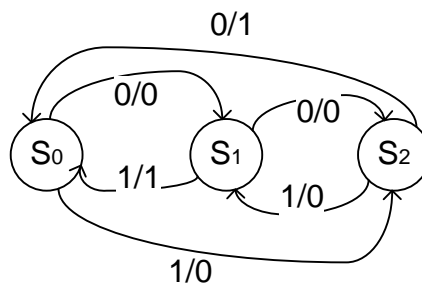


Figure 2

- 10) Consider a $256K \times 64$ memory board.
- a. How many address lines are needed? (1 Mark)
 - b. How many $1K \times 8$ ROM chips are needed for constructing the board (1 Mark).
 - c. What is the size of the decoder? (1 Mark)