| Course: Digital Systems Design | | Course Number: COEN212/1 | Section: CC |
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| Examination: Final | Date: Aug. 19, 2013 | Time: 3 hours | # of pages: 2 |
| Instructor: Dr. M.R. Soleymani | | | |
| Books and Material: No material, no calculator allowed (only one crib sheet) | | | |
| Special Instructions: Try all questions. | | | |

1) A 12-bit register contains 100101000011. What is the value of its content:

   a) as a 3-digit BCD number? (1 Mark)
   b) in Octal? (1 Mark)
   c) as a 12-bit (unsigned) binary number? (1 Mark)
   d) Find two's complement of the number (1 Mark).
   e) Convert the number to Gray code (1 Mark).

2) Consider the following function:

$$F = (x' + y + z')(x + y')(x + z)$$

   a) find $F'$ (the complement of F). (1 Mark)
   b) implement $F'$ using NAND gates only. (2 Marks)
   c) implement $F'$ using NOR gates only. (2 Marks)

   Only non-inverted inputs are available.

3) Consider the function:

$$F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 10, 13).$$

   a) List all *prime implicants*. (give their expression) (2 Mark)
   b) List all *essential prime implicants*. (1 Mark)
   c) Find the minimal sum of products form for F. (2 Marks)
   d) Find the minimal product of sums form for F. (2 Marks)

4) Using a multiplexer design a circuit with a 4-bit input whose output is one when the input is divisible by 3 (4 Marks).

5) Using a decoder design a circuit whose output is $y = 3x + 5$ where $x$ is a 3-bit input (4 Marks).

6) In the circuit shown in Figure 1, the propagation delay of the AND, OR and INVERTER gates are 30 ns., 20 ns. and 10 ns., respectively. The inputs are

initially $A = B = C = 0$. Assume that at time $t_0$ the inputs are changed to $A = B = C = 1$. Draw the signal at points D and E (3 Marks).

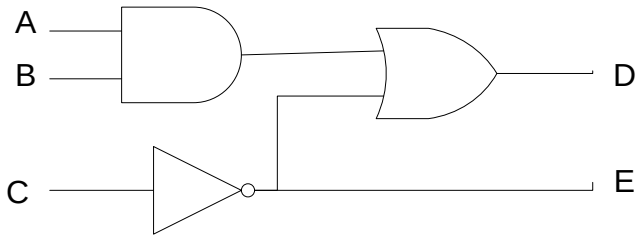


Figure 1

7) A sequential circuit has two JK flip-flops with the following flip-flop input equations:

$$J_A = K_A = Bx$$
$$J_B = x,\ K_B = A \oplus B.$$

   a. Draw the state transition table for the above circuit (4 Marks).
   b. Draw the sate diagram (3 Marks).

8) Using JK flip-flops design a synchronous counter that counts 0, 2, 4, 6, 1, 5, 0 Make sure that unused states are correctable (7 Marks).

9) Design the sequential circuit having the following state diagram using D flip-flops (5 Marks).

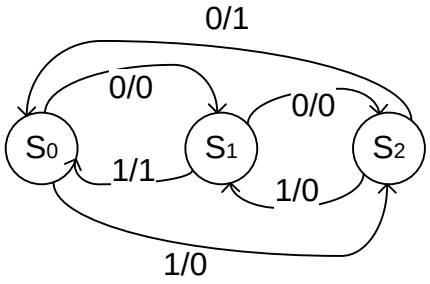


Figure 2

10) Consider a $2M \times 32$ memory board.
   a. How many address lines are needed? (1 Mark)
   b. How many $250K \times 8$ ROM chips are needed for constructing the board (1 Mark).
   c. What is the size of the decoder? (1 Mark)