Course: Digital Systems Design		Course Number: COEN212/1	Section: CC
Examination: Final	Date: Aug. 20, 2014	Time: 3 hours	# of pages: 3
Instructor: Dr. M.R. Soleymani			
Books and Material: No material, no calculator allowed			
Special Instructions: Try all questions.			

1) a) The numbers A=0101 and B=0110 are represented as 4-bit signed binary using 2's complement. Add them together. Show all the steps. Does the addition results in overflow? How do you detect it by looking at the numbers and the carry? (2 Marks)
   b) Subtract B=1100 from A=1101. Show all the steps and values. Convert the result to decimal. A and B are signed binary numbers using 2's complement (2 Marks).

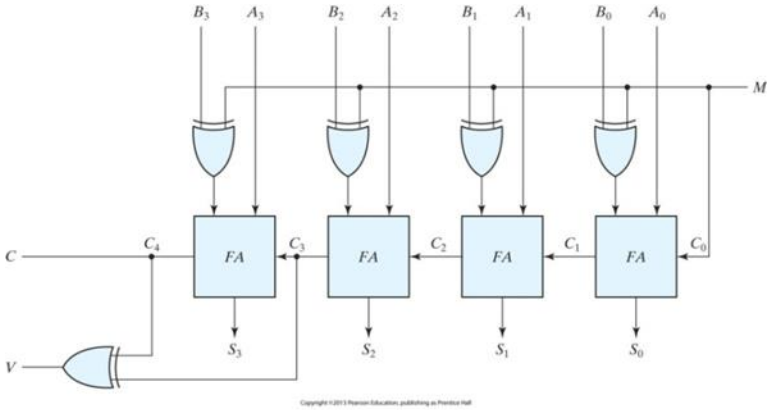


Figure 1: 4-bit adder-subtractor

   c) Using adder-subtractor of Figure 1, perform **addition** of the numbers A = 1010 and B = 0101Find two's complement of the number (1 Mark). State the values on the inputs ($B_3B_2B_1B_0$, $A_3A_2A_1A_0$, and M), and outputs ($S_3S_2S_1S_0$, C, V). What do the values C and V indicate? (2 Marks).
   d) Using adder-subtractor of Figure 1, perform **subtraction** of the numbers A = 0101 and B = 1010 (A-B). State the values on the inputs ($B_3B_2B_1B_0$, $A_3A_2A_1A_0$, and M), and outputs ($S_3S_2S_1S_0$, C, V). What do the values C and V indicate? (2 Marks)

2) Consider the following function:

$$F = AB + AC' + A'B'C$$

   a) find F' (the complement of F). (1 Mark)
   b) implement F' using NOR gates only. (2 Marks)
   c) implement F' using NAND gates only. (2 Marks)

3) Consider the function:

$$F(A, B, C, D) = \sum(3, 8, 9, 10, 11, 12, 14, 15).$$

a) List all *prime implicants*. (give their expression) (2 Mark)
b) List all *essential prime implicants*. (1 Mark)
c) Find the minimal sum of products form for F. (1 Marks)
d) Find the minimal product of sums form for F. (2 Marks)

4) Design a 4-to-1 multiplexer using multiple 2-to1 multiplexers (3 Marks).
Hint: You need three 2-to-1 multiplexers.

5) Using a multiplexer design a circuit with a 4-bit input whose output is one when the input is divisible by 3 (3 Marks).

6) Using full adders design a circuit whose output is $y = 3x^2 + 5$ where x is a 3-bit input (4 Marks).

7) In the circuit shown in Figure 2, the propagation delay of the NAND and XOR gates are 10 ns. and 20 ns., respectively. The input A of the circuit of Fig. 3 is a 2 MHz signal shown below. Draw the timing diagram of the output B (3 Marks).

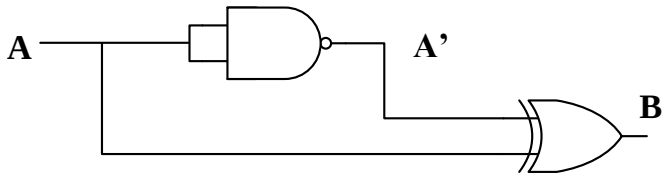


Figure 2

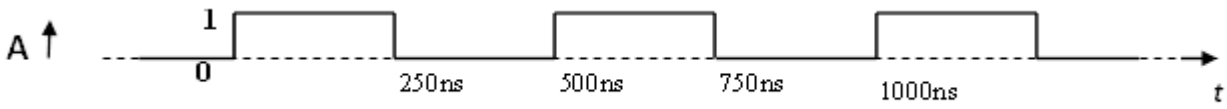


Figure 3

8) A sequential circuit has two JK flip-flops with the following flip-flop input equations:

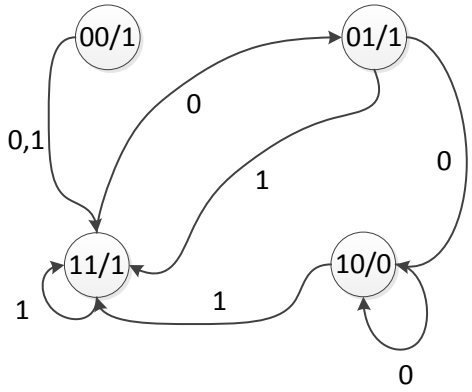
$$J_A = K_A = Bx$$

$$J_B = x, K_B = A \oplus B.$$

a. Draw the state transition table for the above circuit (3 Marks).
b. Draw the sate diagram (2 Marks).

9) Using JK flip-flops design a synchronous counter that counts 0, 1, 3, 5, 7, 2, 0 Make sure that unused states are correctable (6 Marks).

10) Design the sequential circuit having the following state diagram using JK flip-flops (5 Marks).



11) Consider a $2M \times 32$ memory board.

a. How many address lines are needed? (1 Mark)
b. How many $250K \times 8$ ROM chips are needed for constructing the board (1 Mark).