Department of Electrical and Computer Engineering
COEN 212 Dec.15, 2016
Answer all Questions. Exam Duration 3 hour
Examiners : A. J. Al-Khalili and S. Das
No books / papers or electronic devices are allowed.

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Question 1

For a) and b) below use Boolean Algebra.

a)Given F1 and F2 below, determine optimal (**F1 . F2)** and (**F1 + F2)** (2 Marks)

F1= AB + C'

F2= A'C' + B'C'

b) Minimize the following Boolean Function: (2Marks)

F(A,B,C,D)= ABC' + BC'D' + AC'D + ABC + BCD' + ACD'

c) Given F(A,B,C) = AB +A C' + BC (3 Marks)

i) Implement f in **NOR-NOR** format

ii) Implement f in **AND-OR-INVERT** format

Obtain optimum implementation.

Question 2

a) **Design** a digital combinational circuit that implements (8 Marks)

$$F = (N-2)^2 \quad \text{where} \quad N \text{ is an integer } 0 \le N \le 6$$

Show your design steps clearly starting with the Truth Table.
Draw the final circuit.

b) What size of a ROM is required for the implementation of F?

(2 Marks)

Question 3

a) Using a 2 to 1 MUX implement AND, OR and XOR gates. (1 Marks)

b) Implement the Full Adder given below using minimum 2 to 1 MUXes only:

S (A,B,C) = A⊕ B ⊕ C

C_{out} (A,B,C) = A . B + C . (A ⊕ B) (4 Marks)

c) Using a 4 to 1 MUX **implement F**

F (A,B,C,D) = A'.B + A .B.D + A.B'. D' (3 Marks)

Question 4

Design a Decoder that receives a BCD number and displays a **P** on a 7-segment display as shown in Fig. 1 below. If a non-BCD number appears at the input an **F** should be displayed. Start with a truth table and derive final output. Give final circuit diagram. (8 marks)

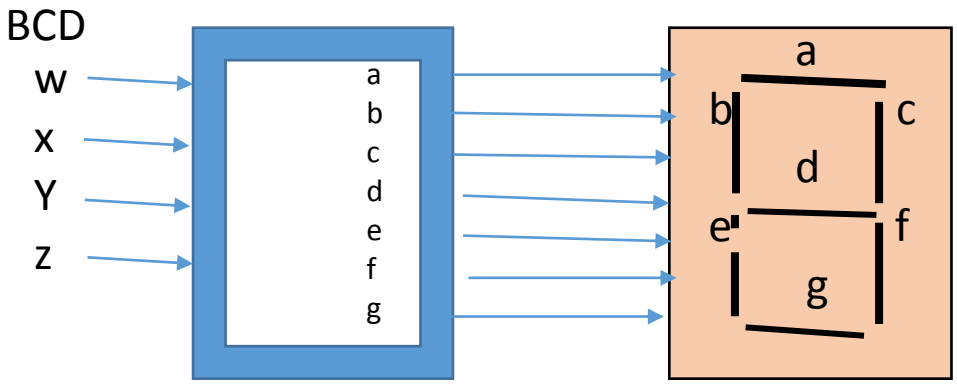

Fig. 1

Question 5

Design an **UP/DOWN BCD** counter, starting with a state diagram. Use T-Flip Flop for your implementation. (7 Marks)

Question 6

a) **Analyze** the circuit given in Fig. 2 below fully (give excitation equations, transition table, state table and state diagram):
b) Initially Do has been set to "1" (for one clock period). Draw the timing diagram for y0, y1, y2 for 5 consecutive clock cycles. Assume each Flip flop has a delay of 10 ns. (10 marks)

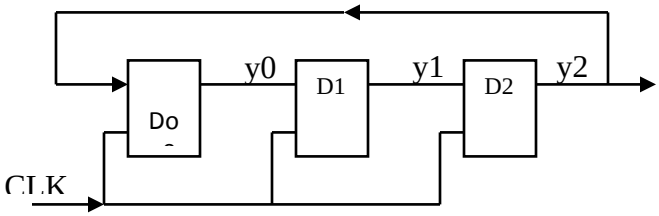

Fig. 2. Circuit to be analyzed in Q.6.