Department of Electrical & Computer Engineering

COEN 212:
DIGITAL SYSTEMS DESIGN I
Lecture 9: Sequential Circuits
Latches and Flip-flops

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Lecture 9:
Objectives of this lecture

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- In this lecture, we talk about:
  - Sequential Circuits.
  - Latches.
  - Flip-flops.

Lecture 9:
Reading for this lecture

- Digital Design by M. Morris R. Mano and Michael D. Ciletti, 6th Edition, Pearson, 2018:
  - Chapter 5 (5.1 to 5.4)

Lecture 9: Sequential Circuits:

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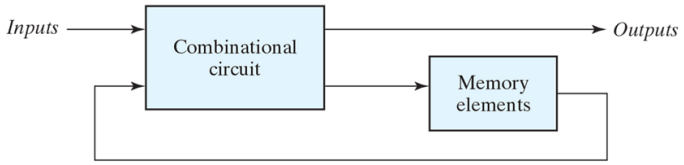
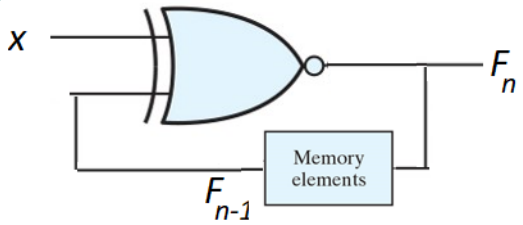
- A typical Sequential Circuit:



- Example:



- State Table:

Present state	Next state		Output (F^n)	
F^{n-1}	$x = 0$	$x = 1$	$x = 0$	$x = 1$
0	0	1	0	1
1	1	0	1	0

Lecture 9:
Sequential Circuits:

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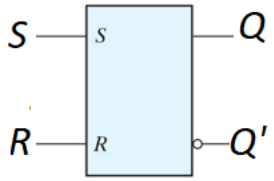
- There are two types of sequential circuits:
  - The synchronous circuits,
  - The asynchronous circuits.

- In the synchronous circuits:
  - state and also outputs change at discrete times dictated by a clock.
- In an asynchronous sequential circuit:
  - the output of each gate is defined based on its input and gates delay. So, the state and outputs can change at any time.
  - The problem with asynchronous circuits is the possibility of encountering instability due to feedback.
- In this course, we mainly consider Synchronous Sequential Circuits.

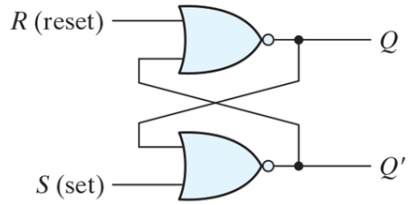
Lecture 9: Latches: SR-Latch

- SR Latch:
  - Has S (Set) and R (Reset) inputs and Q and Q' outputs.
  - Implemented using 2 NORs or 2 NANDs.

Symbol:



Implementation:



- Relationship between S, R, Q and Q'.

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	(forbidden state)

Lecture 9:
Latches: SR-Latch with NAND

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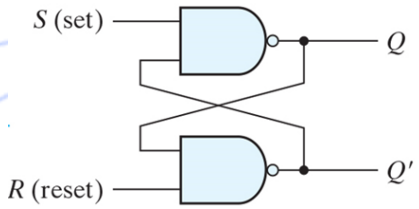
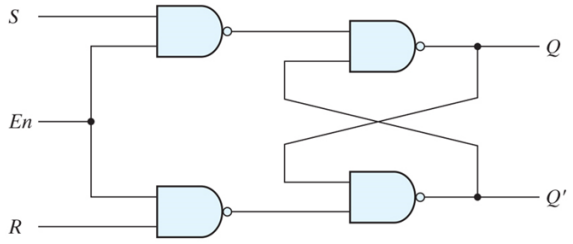
- **SR latch implementation using NAND gates:**
  - Implementation:



Operation:

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	forbidden inputs (00)

- A Control or Enable input can be added.



C	S	R	Next state
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0, \quad Q' = 1$ (reset state)
1	1	0	$Q = 1, \quad Q' = 0$ (set state)
1	1	1	Indeterminate

Lecture 9: Latches: D-Latch

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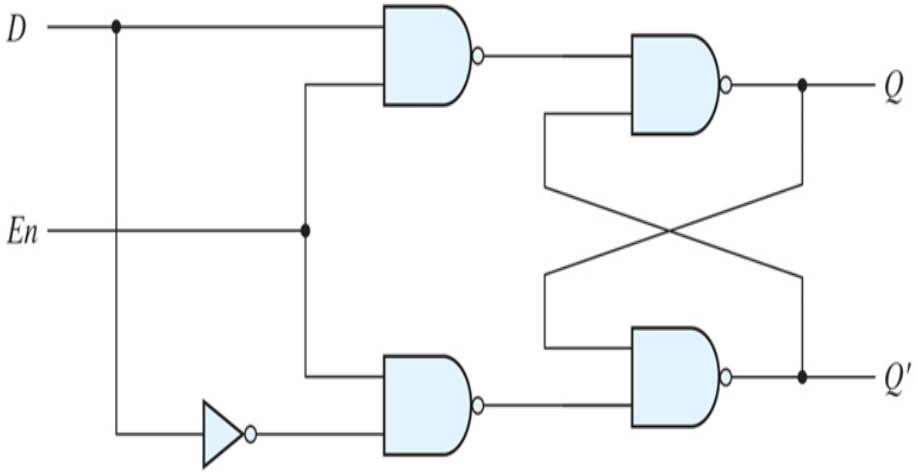
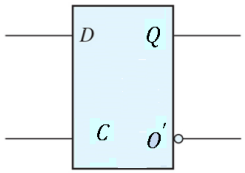
- D-Latch: avoids indeterminate state by making $R = S'$





C	D	Next state
0	X	No change
1	0	$Q = 0, \quad Q' = 1$ (reset)
1	1	$Q = 1, \quad Q' = 0$ (set)

Lecture 9: Flip-flops

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- Output of a Latches depends on the input level.
- Input levels fluctuation may cause erroneous operation.
- Flip-flops are edge triggered. So only change with the clock.
- Some Flip-flops respond to the Rising Edge of clock:

- while others change their state at the Falling Edge:

Lecture 9: Flip-flops

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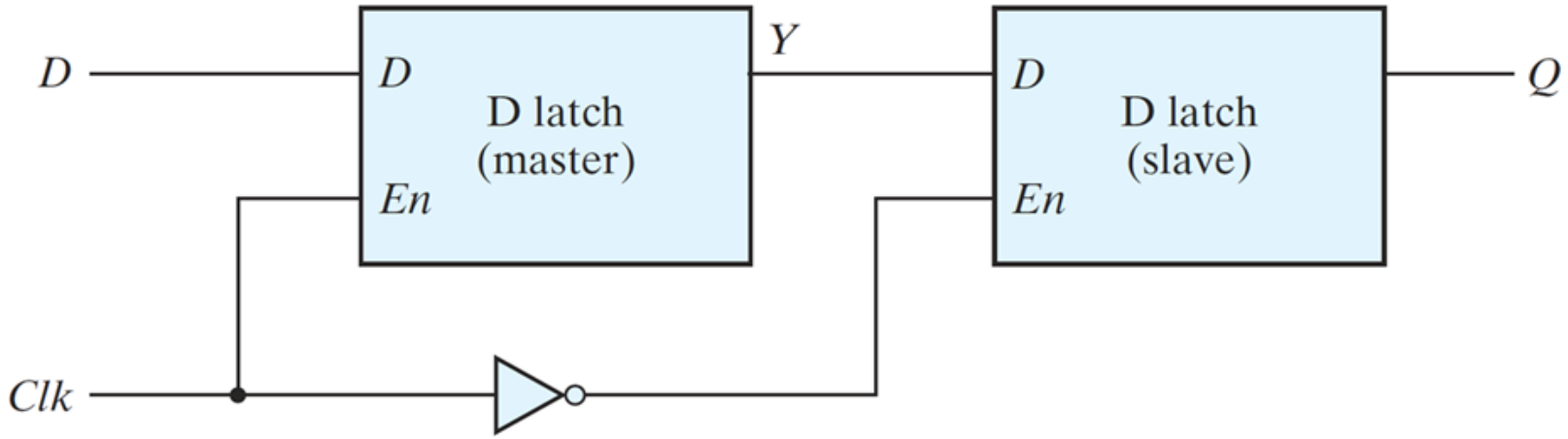
- There are two ways to implement edge-triggered flip-flops:
  - isolate the input from the output. The output change only after control (clock) signal has been removed.
  - make a flip-flop that only changes when level of its clock goes from 0 to 1 or from 1 to 0 and remains unchanged rest of the time.

- **Implementing edge-triggered D flip-flop:**



Lecture 9: D-Flip-flop

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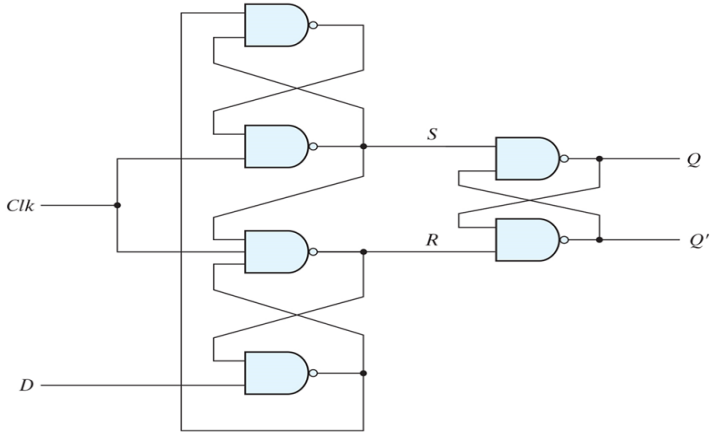
- Implementing D flip-flop using SR-Latch:



- as long as clk=0, $S = 1$ and $R = 1$ and output is unchanged.
- When clk goes to 1:
  - if $D = 0$ makes $R = 0$ and $Q' = 1$ and $Q = 0$,
  - if $D = 1$ the output of the lower most NAND will be 0 and $S = 0$. $Q = 1$, $Q' = 0$.
  - Any further change in D while clk=1 will have no effect on the output.

Lecture 9: D-Flip-flop

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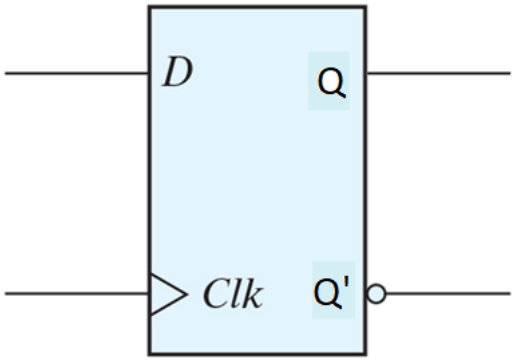
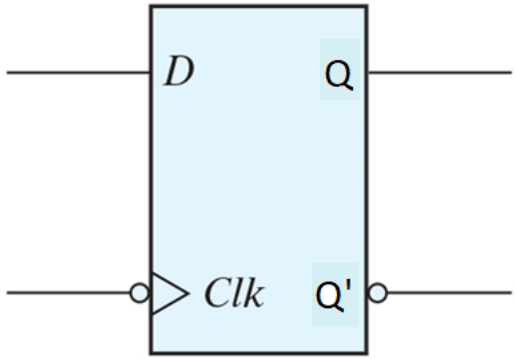
- A rising (positive) edge triggered D-flip-flop is represented by the symbol:



- A falling (negative) edge triggered D-flip-flop is represented by the symbol:



Lecture 9: JK-Flip-flop

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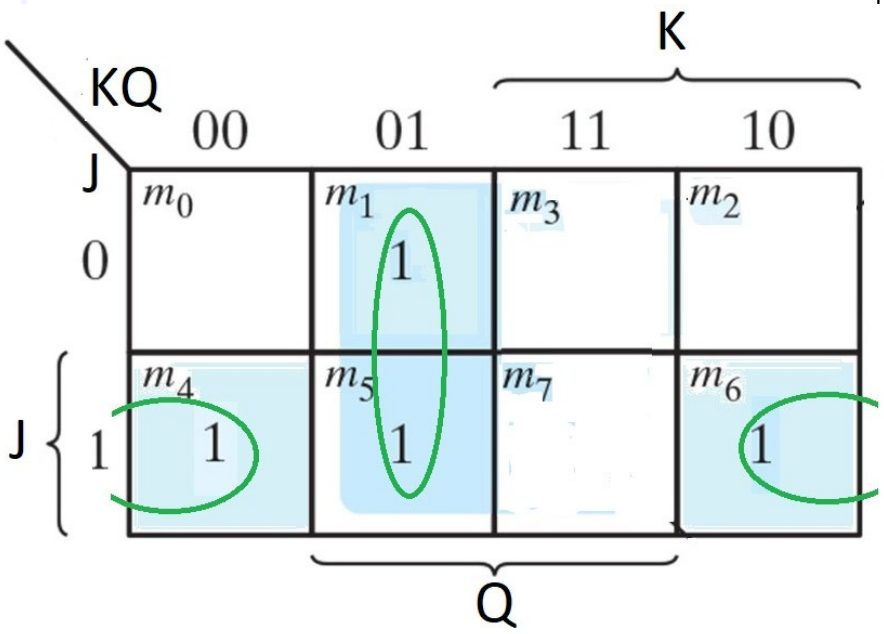
- Truth Table for D
- as a function of J, K and Q:

J	K	Q	D
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

- The K-map for D



$$D = JQ' + K'Q$$

Lecture 9: JK-Flip-flop

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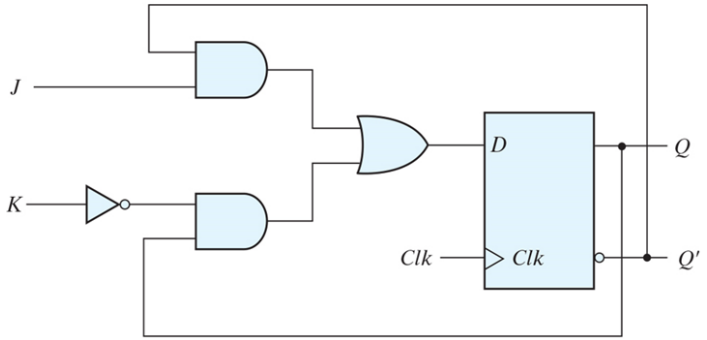
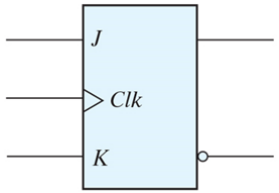
- The Circuit Diagram for the J-K FF is:



- and the symbol is:



Lecture 9: T-Flip-flop

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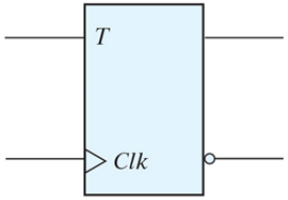
- The Symbol for the T Flip-flop is:



- The T-FF changes its state (toggles) when $T = 1$:

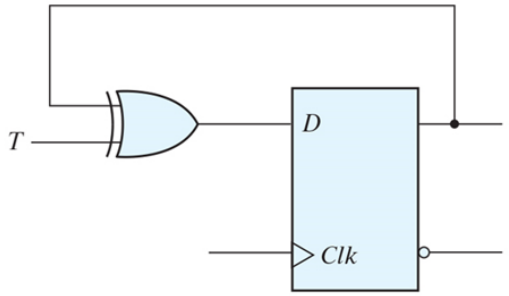
T Q	D	
0 0	0	no change
0 1	1	no change
1 0	1	toggle
1 1	0	toggle

Lecture 9: T-Flip-flop

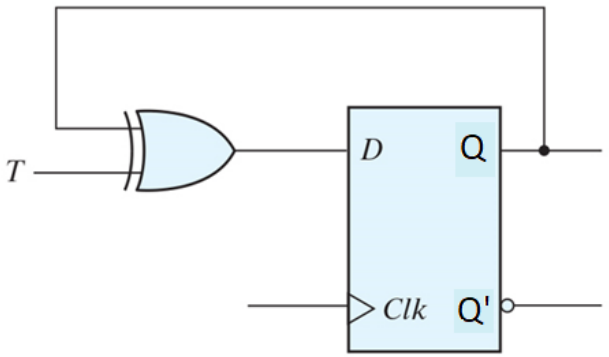
- For implementation using D-FF, we have:

$$D = T \oplus Q.$$

- and the circuit diagram is:



- T-FF could also be implemented using JK-FF



Lecture 9: Characteristic tables and equations:

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- Characteristic tables (or equations) describe the operation of sequential circuits:
- For a JK flip-flop the characteristic table is:

J	K	$Q(t+1)$	
0	0	$Q(t)$	no change
0	1	0	reset
1	0	1	set
1	1	$Q'(t)$	invert

- And the Characteristic Function is:

$$Q(t+1) = JQ'(t) + K'Q(t)$$

where Q(t) and Q(t+1) are the state of the flip-flop, before and after the application of the clock signal.

Lecture 9:
Characteristic tables and equations:

- For D Flip-flop, we have:

D	$Q(t+1)$
0	0
1	1

- So, the characteristic equation is:

$$Q(t+1) = D$$

- For a T flip-flop the characteristic table is:

T	$Q(t+1)$	
0	$Q(t)$	no change
1	$Q'(t)$	toggle (invert)

- And the Characteristic Function is:

$$Q(t+1) = T \oplus Q(t) = T'Q(t) + TQ'(t)$$

Lecture 9:
Flip-Flop with Direct Inputs:

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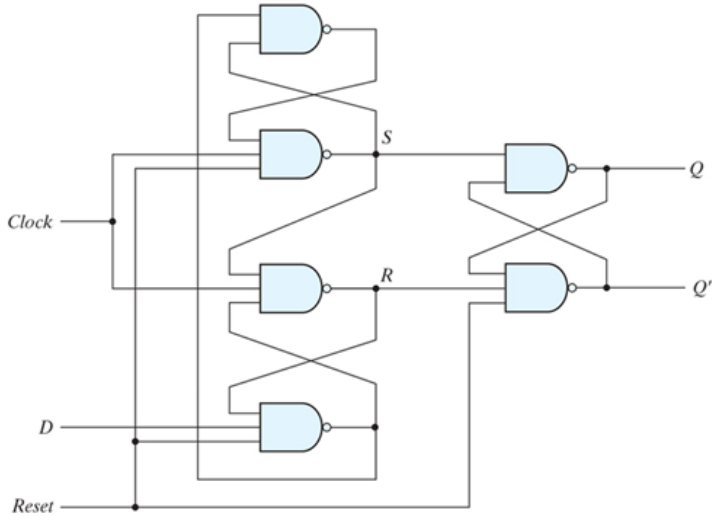
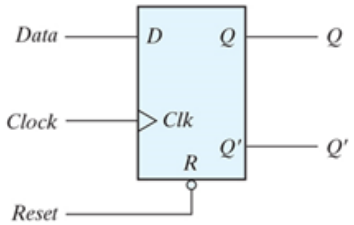
- A flip-flop with a reset state:



- The symbol for D-FF with reset:



Lecture 9: Knowledge Check

- **Question 1:** In a JK FF Q=1, the input J=1, K=1 results in:

a) Q=1, b) Q=0, c) Q'=0, d) undefined state

- **Question 1:** In a T FF Q=1, applying a four bit stream 1010 results in:

a) Q=1, b) Q=0, c) Q'=0, d) Q=10