OLD EXAMS

COEN 312 DIGITAL DESIGN

COEN 312 DIGITAL DESIGN
Final April 19, 2001
Answer all questions
No calculators, notes or books are allowed

Lecturers: A.J. Al-Khalili, M. Nekili, C. Taillefer
Time allowed 3:00 hours

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Question 1 (10 Marks)

(a) Given the function F', determine the complement function F and minimize the total number of literals using **Boolean algebra**. (3 Marks)

$$F' = \left[(z+0)\cdot(x'+y)+zxy'+z'(y+y'x)+z'x'\right]'$$

(b) Minimize the function Y using **Karnaugh Maps**. Present your answer as a product of sums (POS). List all the **prime implicants**. (4 Marks)

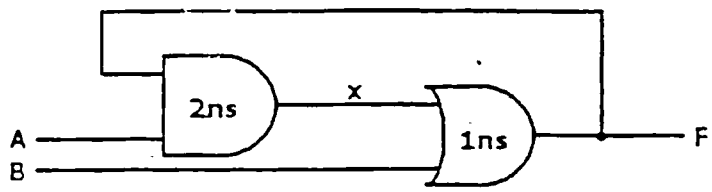
$$Y = \prod(3,5,7,8,12,13)+d(0,2,4)$$

(c) Determine the minimized Boolean function Q defined in the following Truth Table. Use the **Quine-McCluskey Tabular Method**. (3 Marks)

A	B	C	Q
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	1
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	1

Question 2 (10 Marks)

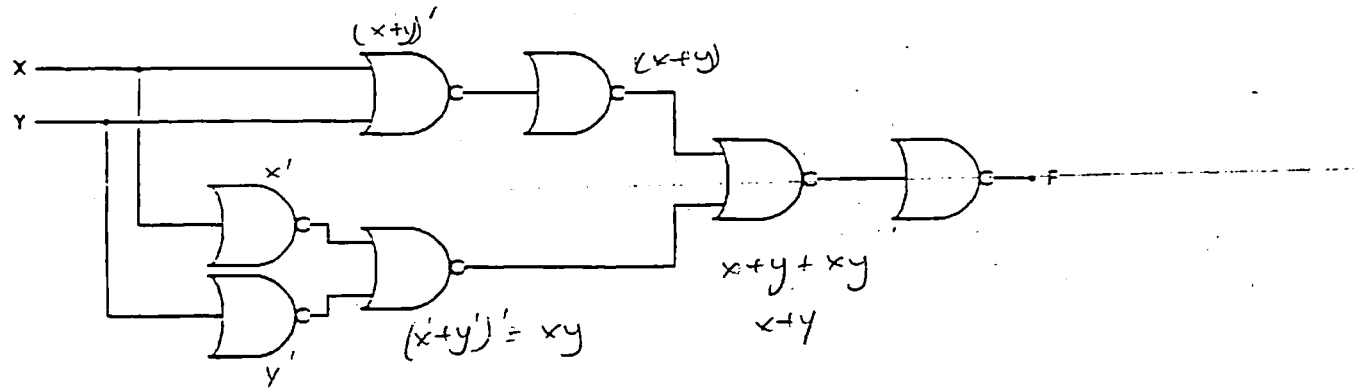
(d) Determine the timing diagram for the circuit below, where the inputs change simultaneously every 10ns from AB = 00 to AB = 11, then to AB = 00. Assume the AND gate has a propagation delay of 2ns and that the OR gate has a propagation delay of 1ns. Clearly label all the delays on the timing diagram. (5 Marks)

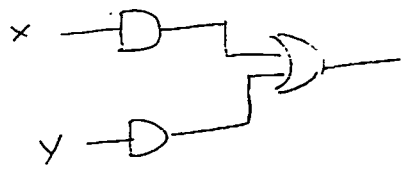


Question 2 (10 marks)

(a) Convert the all-NOR multi-level combinational logic circuit to

(i) a two-level AND-OR-Inverter circuit (2 Marks)
(ii) a two-level all-NAND circuit (3 Marks)





Question 3 (10 Marks)

(a) Design a 3-to-8 decoder using NOR gates only. Mark the minterms obtained. (3 Marks)

(b) Use a 3-to-8 decoder plus minimal logic gates to implement the following functions: (3 Marks)

$$F(A,B,C) = \sum(0,1,2)$$
$$F(A,B,C) = \sum(4,6,7)$$
$$F(A,B,C) = \sum(2,3,5)$$

(c) Use a 4-to-1 MUX plus minimal extra logic (if necessary) to implement the following function: (4 Marks)

$$F(A,B,C,D) = AB' + A'B'C' + A'BD$$

Question 4 (10 Marks)

(a) Design a binary multiplier to multiply 2-bit binary numbers $A=a_1a_0$ and $B=b_1b_0$. (4 Marks)

(b) Implement using a ROM by showing the patterns of "0"s and "1"s stored in the ROM as words and bits. (2 Marks)

(c) Minimize and then implement using a PLA. (4 Marks)

Question 5 (10 Marks)

Design a synchronous sequential circuit, having one input x and one output z. Data is arriving serially on line x. The output z=1 if the total number of 0's received is an even number greater than zero, provided that two consecutive 1's have never occurred.

Question 6 (10 Marks)

Starting with all flip-flops outputs at the Low level, plot the timing diagram for the outputs q_0, q_1 and Z over six clock periods for the circuit in the figure below. Assume that the JK flip-flops have a propagation delay of 10ns, the clock frequency is 10MHz, and the XOR gate has no delay.