Microwave Oscillator Design

Application Note A008

Introduction

This application note describes a method of designing oscillators using small signal S-parameters. The background theory is first developed to produce the design equations. These equations are then applied to develop three different oscillators: a 4 GHz bipolar lumped resonator oscillator, a 4 GHz bipolar dielectric resonator oscillator, and a 12 GHz GaAs FET dielectric resonator oscillator.

Theory

Microwave transistors can be used for both amplifier and oscillator applications. From the small signal s parameters of the transistor, the stability factor k can be calculated from:

$$k = \frac{1 + |D|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{21}||s_{12}|} \quad (1)$$

where

$$k = s_{11}\, s_{22} - s_{21}\, s_{12} \bullet \quad (2)$$

Note that since the transistor S-parameters change with frequency, k also varies with frequency.

A transistor is unconditionally stable at any frequency where k > 1. This condition guarantees that at the specified frequency the transistor will not oscillate into any termination at either port that has a positive resistance (i.e. into any impedance that is inside the Smith chart). To be mathematically rigorous, we should add that the condition |D| < 1 must also be met to insure stability. Since in practice with real circuits this seems always to be the case, we ignore this requirement in this design procedure.

For amplifiers it is desirable to have k > 1. At any frequency where this condition holds, a simultaneous match can be achieved at both ports, resulting in:

$$s_{11}' = s_{11} + \frac{s_{12}\, s_{21}\, \Gamma_L}{1 - s_{22}\, \Gamma_L} = 0 \quad (3)$$

$$s_{22}' = s_{22} + \frac{s_{12}\, s_{21}\, \Gamma_G}{1 - s_{11}\, \Gamma_G} = 0 \quad (4)$$

In these equations Γ_G is the reflection coefficient seen looking into the generator, and Γ_L is the reflection coefficient seen looking into the load. The unprimed S-parameters refer to the transistor as measured with 50 Ω terminations, and the primed S-parameters show the effects of loading the transistor with Γ_G and Γ_L. When equations (3) and (4) are satisfied, there is no reflected power at either the input port or at the output port. The power gain of the transistor under these conditions is called the maximum available gain (Gma), and is given by:

$$G_{ma} = |s_{21}'|^2 = \frac{|s_{21}|}{|s_{12}|}\left(k - \sqrt{k^2 - 1}\right) \quad (5)$$

The S-parameters are a function of the common (ground) lead. Usually amplifiers are built in the common emitter or common source configuration since k is often greater than one with this grounding. If k < 1 it is still possible to design an amplifier for finite gain. To do so, the condition that both Γ_G and Γ_L are in the stable region must be satisfied. With k < 1 a simultaneous match is not possible, as selecting Γ_G = s11'* = 0 and Γ_L = s22'* = 0 would result in terminations in the unstable region. With k < 1 the amplifier must be less than perfectly matched. Many practical amplifiers are built in this manner.

This discussion of amplifier design gives us some insight into how to design an oscillator from small signal S-parameters. If we can design an "amplifier" for which k < 1 and either Γ_G or Γ_L is in the unstable region, we will in reality have designed an oscillator (see Figure 1).

The necessary conditions for oscillation can be restated as:

$$k < 1 \tag{6}$$

$$S_{11}' \Gamma_G = 1 \text{ and } S_{22}' \Gamma_L = 1 \tag{7}$$

If the active device selected has a stability factor greater than one at the desired frequency of oscillation, condition (6) can be achieved either by changing the two-port configuration (changing from common emitter to common base or common collector, for example) or by adding feedback.

Condition (7) simply confirms that the oscillator produces power at both ports. If either condition in (7) is satisfied, the other condition is automatically satisfied. Once we have achieved k < 1, condition (7) gives the necessary relationship to complete the oscillator design. We will adopt the technique of resonating the input port and designing a match that satisfies condition (7) at the output.

The upper frequency for oscillation is limited to fmax, which is the frequency where unilateral gain equals unity. The unilateral gain is generated by reducing the S-parameters to a single gain parameter given by:

$$s_{11}' = 0$$
$$s_{22}' = 0$$
$$s_{12}' = 0$$

$$U = \left|s_{12}'\right|^2 \frac{1/2\left|s_{21}/s_{12} - 1\right|}{k\left|s_{21}/s_{12}\right| - \mathrm{Re}\left\{s_{21}/s_{12}\right\}} \tag{8}$$

This parameter U is the highest gain the transistor can ever achieve, and it is invariant to the common lead. In practice, it is difficult to build a useful oscillator at frequencies above fmax/2.

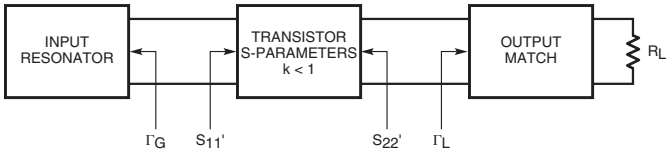

Figure 1. Oscillator design.

Design Procedure

Oscillator design from s parameters therefore proceeds as follows. First an active device is selected, and its stability factor k is calculated at the desired frequency of oscillation. If k < 1 the design can proceed. If k > 1, a configuration change must be made or feedback must be added until k < 1 is achieved.

With k < 1 we know that an input matching circuit having Γ_G which produces |s22'| > 1 can be found. The design condition is therefore

$$\left|s_{22}'\right| > 1 \tag{9}$$

This condition can be viewed as stating that there is a negative resistance at the output port of the terminated transistor. There are many techniques for realizing such an input circuit, or resonator. One method is to use a computer simulation and optimize for the condition that s11 of the one port consisting of the resonator cascaded with the transistor (this is equal to s22' of the transistor) is greater than unity. A resonator satisfying the property that $|\Gamma_G| = 1$ is lossless; this is a desirable feature in most oscillator designs. Oscillators are often named by the type of resonator they employ, as shown in Table 1.

Table 1. Oscillator Types

Resonator	Oscillator Name
Cavity	High Q or Stable
YIG	YTO (YIG Tuned Oscillator)
Varactor	VTO (Voltage Tuned Oscillator)
Lossless Transmission Lines	Distributed or Microstrip Oscillator
Lossless Lumped Element	Lumped Oscillator
Dielectric Resonator	DRO (Dielectric Resonator Oscillator)

With the input circuit established, the load circuit is designed to satisfy:

$$\Gamma_L = 1/S_{22}' \tag{10}$$

which follows directly from condition (7). Note that since |s22'| > 1, this equation guarantees $|\Gamma_L| < 1$, i.e. the load resistor will be positive.

For the special case where the oscillator is intended to oscillate directly into a 50 Ω load, no load circuit needs to be designed, and the condition for oscillation can be re-expressed. If the load is 50 Ω, $\Gamma_L = 0$. Therefore, since $|s22'|\,\Gamma_L = 1$, we have $|s22'| = \infty$. In practice, it has proven sufficient to design for

$$\left|s_{22}'\right| > 100 \tag{11}$$

Satisfying condition (9) requires $|\Gamma_L| < .01$, which corresponds to a load that is essentially 50 Ω.

The above method will only predict the frequency of oscillation. It provides no information about output power, harmonics, phase noise, or other parameters of possible interest. In general, the output power of the oscillator will approach the 1 dB compression power (P1 dB) of the transistor used as an amplifier if the DC bias is designed for maximum P1 dB. Other performance parameters would typically have to be measured from the finished oscillator.

Design Examples

Example 1: A 4 GHz Lumped Resonator Oscillator

The first example is a computer study of a 4 GHz lumped resonator oscillator based on the Avago AT-41400 bipolar transistor chip. The program used in this design is TOUCHSTONE™ from EEsof; any other linear analysis and optimization could equally well be used. To achieve an "active device" with k < 1, the transistor chip is used in the common base configuration. The catalog common emitter S-parameters are used to describe the transistor chip. The S-parameters for a bias of 8 V and 25 mA are selected to give the best output power. Since this data includes 0.5 nH of base bonding inductance and 0.2 nH of emitter bonding inductance (see reference 1), these parasitics have to be removed (by cascading negative valued inductors) to get to the chip level S-parameters. The 0.21 nH base bond wire used in the oscillator is included as part of the "active device" description. Note that the nodal connections establish the emitter as the input and the collector as the output. Analysis shows that this two port has a stability factor k = -0.423 at 4 GHz. Since this value is less than one, we know that an oscillator design is possible.

A topology of series inductor (emitter bond wire) – shunt capacitor is chosen for the resonator. Note that other resonator topologies are possible; this choice represents one possible solution that is easily realized physically. Initial values are guessed (4 pF for the capacitor, 0.2 nH for the inductor) and the circuit is optimized for s11 of the oscillator greater than 100. Optimization finds a solution of C = 3.9891 pF; LE = 0.16044 nH, and LB = 0.21362 nH. The circuit file is shown in Figure 2, along with the output file. Note MAG[S11] of OSC = 140.756 > 100, i.e. the circuit will oscillate into an essentially 50 Ω load. A schematic for the finished design is shown in Figure 3.

```
! <OSCEX1_T.CKT>
! A 4 GHZ LUMPED RESONATOR OSCILLATOR USING THE AT-41400 CHIP

CKT

         IND_LBX  1        2                  L=-.5
         S2PA     2        3         4        A:\S_DATA\AT41400G.S2P
         IND_LEX  4        5                  L=-.2
         DEF3P    5        3         1        CHIP
! CHIP IS THE AT-41400 CHIP WITH BOND WIRES REMOVED AND CONFIGURED COMMON BASE

         CHIP     1        2         3
         IND_LB   3        0                  L#.15 0.21362 1
         DEF2P    1        2                  XR
! XR IS THE ACTIVE DEVICE FOR THE OSCILLATOR

         CAP_CR   1        0                  C# .01 3.98910 25
         IND_LE   1        2                  L# .15 0.16044 1
         XR       2        3
         DEF1P    3                           OSC
!OCS IS THE RESONATED OSCILLATOR


FREQ

         STEP     4

OUT

         XR       K
         OSC      S11

OPT

         XR       K<1
         OSC      MAG[S11]>100
```

Figure 2a. Circuit file for 4 GHz lumped resonator oscillator.

```
FREQ-GHZ          K MAG[S11] ANG[S11]
                 XR       OSC       OSC

4.00000      -0.423  140.756   52.435
```

Figure 2b. Output file for OSCEX1_T.

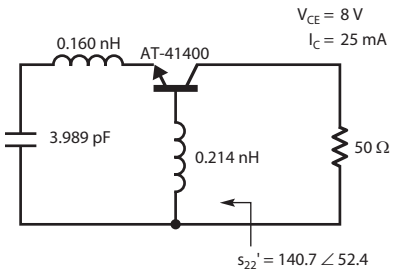

Figure 3. Lumped resonator oscillator at 4 GHz.

Example 2: A 4 GHz Dielectric Resonator Oscillator

A more interesting circuit to build is an equivalent 4 GHz oscillator that uses a dielectric resonator (DR) in series configuration to create the input resonator. In this application the DR is tightly coupled in the TE01δ mode (reference 2) to an input 50 Ω microstrip line. This effectively creates a very large resistance (i.e. open circuit) at the correct electrical distance from the transistor, causing oscillation. One advantage to using a DR as the input resonator is that the very high unloaded Qs of these devices (often on the order of 10000) yields an oscillator with little tendency to drift in frequency. The fact that the resonator consists effectively of an open circuit that is only coupled to the line at the frequency of oscillation indicates that at other frequencies the transistor can be terminated in 50 Ω, greatly reducing the possibility of secondary oscillations at undesired frequencies.

Once again the circuit can be simulated and optimized for s11 OSC > 100. The dielectric resonator is modeled by a large valued series resistor. The initial estimate of 1000 Ω comes from an estimate of 10 for the coupling coefficient β of the DR to the microstrip line (typical for this kind of application), and the relationship that β = R/(2 Zo). This value and the distance from the transistor at which the DR is coupled are the variables for optimization. A printout of the circuit file and the resultant output are given in Figure 4. The schematic for the resulting oscillator is shown in Figure 5. Measurements on this oscillator (reference 3) show that as predicted the frequency of oscillation is 4 GHz. The observed output power of + 14 dBm is in fair agreement with the +19 dBm level that would be predicted from the P1 dB of the transistor. This oscillator also exhibited excellent phase noise performance, –117 dBc/Hz at 10 kHz from the carrier.

(Phase noise is a way of measuring the "noise skirts" of the oscillator. This noise level is expressed as being a certain level below the oscillation signal, at a certain distance out from the center frequency of oscillation. High levels of suppression at a narrow spacing indicates a very quiet oscillator.)

Example 3: A 12 GHz Dielectric Resonator Oscillator

Most high performance microwave bipolar transistors have an fmax on the order of 20 GHz. Thus it is difficult to build oscillators with these devices at 12 GHz (above fmax/2). Gallium arsenide field effect transistors, with typical fmax values approaching 100 GHz, provide a reasonable solution to this problem. Where possible silicon bipolar transistors are used for oscillator design because of their superior phase noise performance.

The third example uses a dielectric series resonator to input tune a common-source GaAs FET, the packaged ATF-26836. The S-parameter data is taken from the model (reference 4) of the ATF-26836 at a bias condition of 5 V, 30 mA. As before, a circuit simulation is done, with the variable for optimization being the position of the DR relative to the transistor. The resulting circuit is given in Figure 6. This circuit uses a dielectric substrate of ε = 2.2 and h = 20 mils.

This oscillator has been built and tested over temperature. These measurements show another significant advantage of DROs. By choosing a DR with the appropriate temperature coefficient, an oscillator that is very stable in output frequency over temperature can be built. Using a dielectric puck with a temperature coefficient of 3 ppm/°C the frequency remains constant to ±3 MHz over a -40° C to 60° C temperature range. The typical output power is 11 dBm, and the efficiency is about 10%. Typical test data for this oscillator is plotted in Figure 7. The oscillator phase noise at 100 kHz from the carrier is about –110 dBc/Hz.

```
! <OSCEX2_T.CKT>
! A 4 GHZ DIELECTRIC RESONATOR OSCILLATOR USING THE AT-41400 CHIP

CKT

         IND_LBX   1         2                   L=-.5
         S2PA      2         3         4         A:\S_DATA\AT41400G.S2P
         IND_LEX   4         5                   L=-.2
         DEF3P     5         3         1         CHIP
! CHIP IS THE AT-41400 CHIP WITH BOND WIRES REMOVED AND CONFIGURED COMMON BASE

         CHIP      1         2         3
         IND_LB    3         0                   L=.33
         DEF2P     1         2                   XR
! XR IS THE ACTIVE DEVICE FOR THE OSCILLATOR

         RES_DR    1         0                   R/1.421e+03
         TLINP     1         2                   Z=50 L/218.81238 K=6.6 A=0 F=1
         IND_LE    2         3                   L=0.5
         XR        3         4
         DEF1P     4                             OSC
!OCS IS THE RESONATED OSCILLATOR


FREQ

         STEP      4

OUT

         XR        K
         OSC       S11

OPT

         XR        K<1
         OSC       MAG[S11]>100
```

Figure 4a. Circuit file for 4 GHz dielectric resonator oscillator.

```
FREQ-GHZ          K MAG[S11] ANG[S11]
                 XR       OSC       OSC

4.00000      -0.675  195.417  -38.919
```

Figure 4b. Output file for OSCEX2_T.

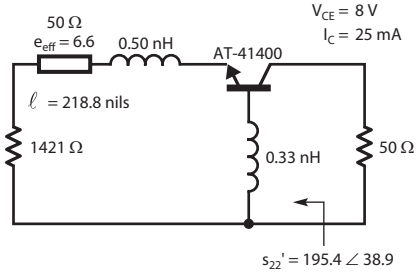

Figure 5. Dielectric resonator oscillator (DRO) at 4 GHz.

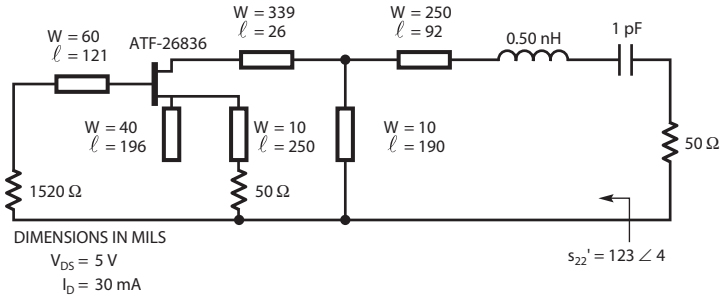

Figure 6. Dielectric resonator oscillator (DRO) at 11.5 GHz.

Conclusion

By applying the design procedure given in this note, many oscillator circuits can be designed using both silicon bipolar transistors and gallium arsenide field effect transistors up to frequencies approaching fmax/2 of the transistor. The final design will depend upon practical considerations, including realizability, size, component layout, harmonic response, phase noise, and repeatability in production.

References

1. Avago 1987 Semiconductor Data Book – Silicon Products, p. 161.
2. D. Kajfez and P. Guillon, Dielectric Resonators, Artech, 1986.
3. G.D. Vendelin, W.C. Mueller, A.P.S. Khanna, and R. Soohoo, "A 4 GHz DRO", Microwave Journal, June 1986, pp. 151-152.
4. Avago 1987 Semiconductor Data Book – Gallium Arsenide Products.

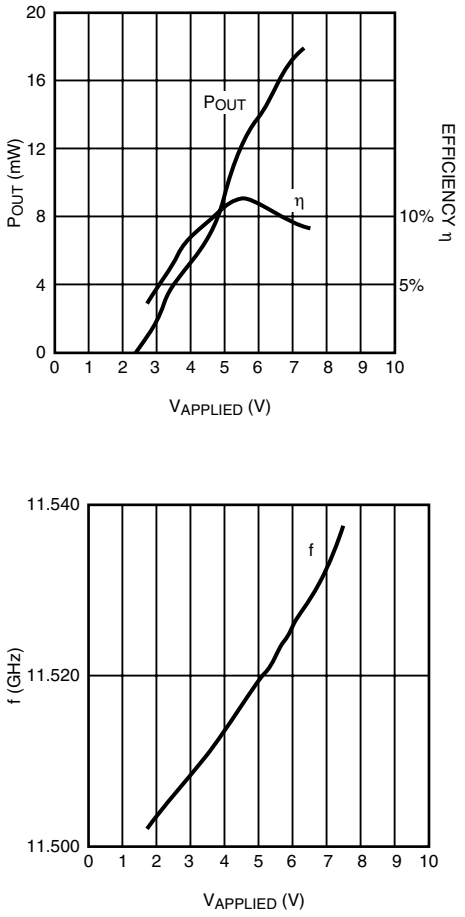

Figure 7. Test data for 11.5 GHz DRO.

5968-3628EN - September 2, 2010