ELEC 312: ELECTRONICS – II (ASSIGNMENT Set#1)
Department of Electrical and Computer Engineering
Winter 2011-2012

7.46_Solution:

$I_0 = I_D = \frac{1}{2} k'_n (\frac{W}{L}) V^2_{ov}$ form this equation we can get the value of $V_{ov} = 0.25$ V. Now

$V_{DS} = V_{GS} = V_t + V_{ov} = 0.75$ V and hence $R = \frac{V_{DD} - V_{GS}}{I_{ref}} = 10.5\ k\Omega$

The lowest V_0 will be when $V_{DS2} = V_{OV} = 0.25$ V

$R_0 = \frac{V_A.L}{I_D} = 50k\Omega$ and $\Delta I_D = \frac{V_0}{R_0} = 10\ \mu A$

7.51_Solution:

From the figure p7.51 we can write V_{OS2} & $V_{GS2} - V_{pt}$ => $V_{DS\,max} = V_{GS2} - V_t$ therefore we get $V_{GS1} = -0.8$ V

Now for Q_1:

$I_{D1} = 20\ \mu A = \frac{1}{2} \times 80 \times \frac{W_L}{0.8} \times (-0.8 + 0.6)^2$ and hence $W_1 = 10\ \mu m$

$I_2 = 5\ I_{REF}$ so $W_2 = 5W_1 = 50\ \mu m$

$I_3 = I_{REF}$ so $W_3 = W_1 = 10\ \mu m$ and $W_4 = W_3 \frac{\mu_p}{\mu_n} = 4\ \mu m$

For Q_5 :

$V_{DS5} = V_{GS5} - V_{tn}$ for lowest V_0

$I_5 = 50\ \mu A = \frac{1}{2} \times 200 \times \frac{W_5}{0.8} \times (0.8 - 0.6)^2$ therefore $W_5 = 10\ \mu m$

Now we calculate R:

$V_{G2} = 1.5-0.8 = 0.7V$; $R = \frac{V_{G2}}{I_{REF}} = 35\ k\Omega$ and $R_{02} = \frac{V_{A2}.L}{I_2} = 96k\Omega$ and $R_{05} = \frac{V_{A5}.L}{I_5} = 160\ k\Omega$.

7.55_Solution:

Let $I_{C1} = I_C$ and $I_{C2} = I_0$

$I_{REF} = I_C + \frac{I_C}{\beta} + \frac{I_0}{\beta}$ -----(1) and since $I_{S2} = m\, I_{S1}$ therefore $I_C = \frac{I_0}{m}$ ------(2)

Substituting (2) into (1) we will get $\frac{I_0}{I_{REF}} = \frac{m}{1+\frac{1+m}{\beta}}$

Now if $\beta_{min} = 50$ and we want to limit the transfer error to 10%, consider that if $\beta >> 1$

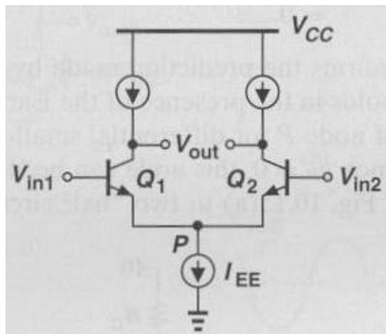
$\frac{I_0}{I_{REF}} \approx m$ Doping 10%, would mean that $(0.90)\, m = \frac{m}{1+\frac{1+m}{\beta}}$ and therefore we will get m = 4.56.

ELEC 312: ELECTRONICS – II ASSIGNMENT-Set#2

Department of Electrical and Computer Engineering

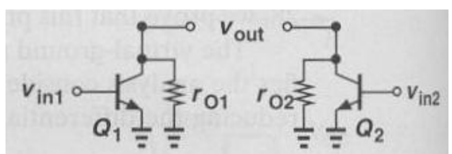
Winter – 2012

1. Find an expression for the differential gain of the following circuit, where ideal current sources are used as loads to maximize the gain. $V_{in1,}$ V_{in2} may be assumed to be balanced differential signals.



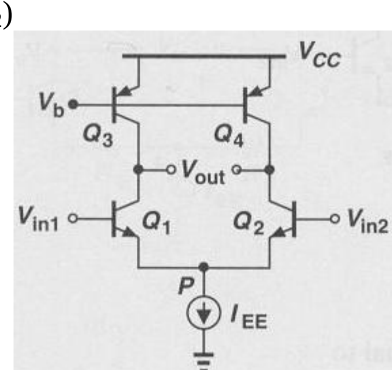
Hints:

With ideal current sources, the Early effect in Q_1 and Q_2 cannot be neglected, and the half circuits must be visualized as depicted in the following figure:



$v_{out1} = -g_m r_o v_{in1}$, $v_{out2} = -g_m r_o v_{in2}$, and hence $(v_{out1} - v_{out2}) / (v_{in1} - v_{in2}) = - g_m r_o$

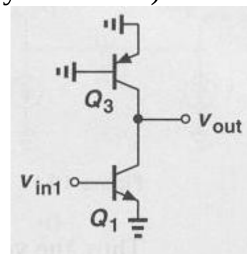
2. The following figure illustrates an implementation of a differential amplifier with active load using complementary BJT devices. Calculate the differential voltage gain $V_{out}/(V_{in1} - V_{in2})$



Hints:

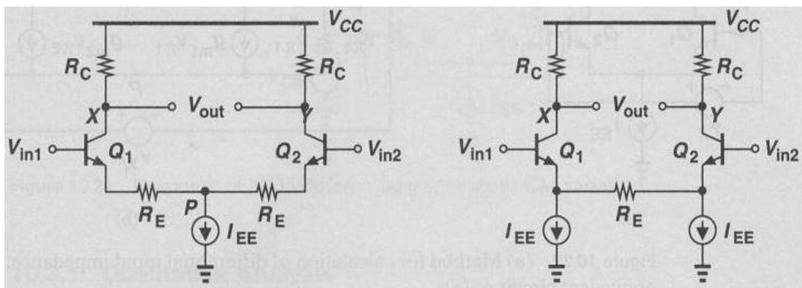
We will assume (since it is not stated otherwise) that the input signals are balanced-differential. Sp node P is at virtual ground.

Noting that each pnp device introduces a resistances a resistance of r_{OP} at the output nodes and drawing the half circuit as the bellow figure, we have (considering each half-circuit and combining differentially at the end)



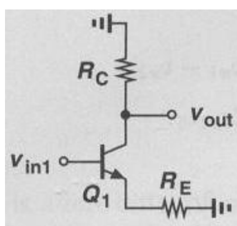
$(v_{out1} - v_{out2}) / (v_{in1} - v_{in2}) = - g_m (r_{ON} // r_{OP})$. Where r_{ON} denotes the output impedance of the npn transistors.

3. Determine the gain of the emitter degenerated differential pairs shown in the following figure. Assume $V_A = \infty$.



<u>Hints:</u>

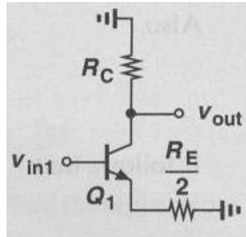
In the 1st figure, node P is a virtual ground, yielding the half circuit depicted in the following figure,



we have (like a CE amplifier with emitter load)

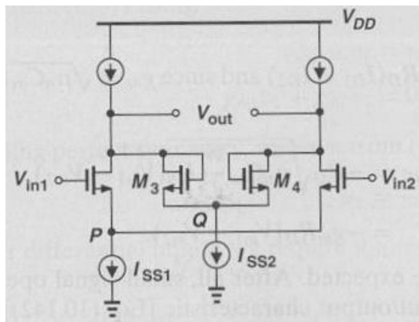
$A_v = - R_C / (R_C + 1/g_m)$.

In the 2nd figure, the line of symmetry passes through the "midpoint" of R_E. In other words, if R_E is regarded as two $R_E/2$ units in series, then the node between the units acts as a virtual ground as the following figure,



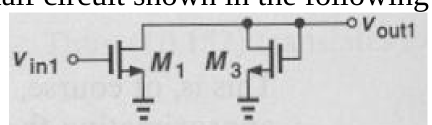
We have, $A_v = - R_C / (R_E/2 + 1/g_m)$.

4. Assuming $\lambda = 0$, compute the voltage gain of the following circuit. I_{SS2} is used to bias the transistors M_3 and M_4. Consider all I-sources are identical.



Hints:

Assume balanced differential operation. Identifying both nodes P and Q as virtual grounds, we construct the half circuit shown in the following figure,



And we have, $A_v = - g_{m1} / g_{m3}$