2.3.3.1: A two-stage MOS operational amplifier (OP-AMP)

Figure 31 depicts the schematic of a two-stage CMOS operational amplifier[1]. Let us calculate the voltage gain that can be afforded by this circuit.

Toward this, we need to know about the bias currents and the characteristics of the devices, such as width (W), length (L), transconductance factor ($\mu_n C_{ox}$, $\mu_p C_{ox}$), threshold voltages (V_{THN}, V_{THP}), and the *Early* voltages (V_{AN}, V_{AP}). Consider the following given information.

W/L values (Table)

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L (in μm)	20/0.5	20/0.5	5/0.5	5/0.5	40/0.5	10/0.5	40/0.5	40/0.5

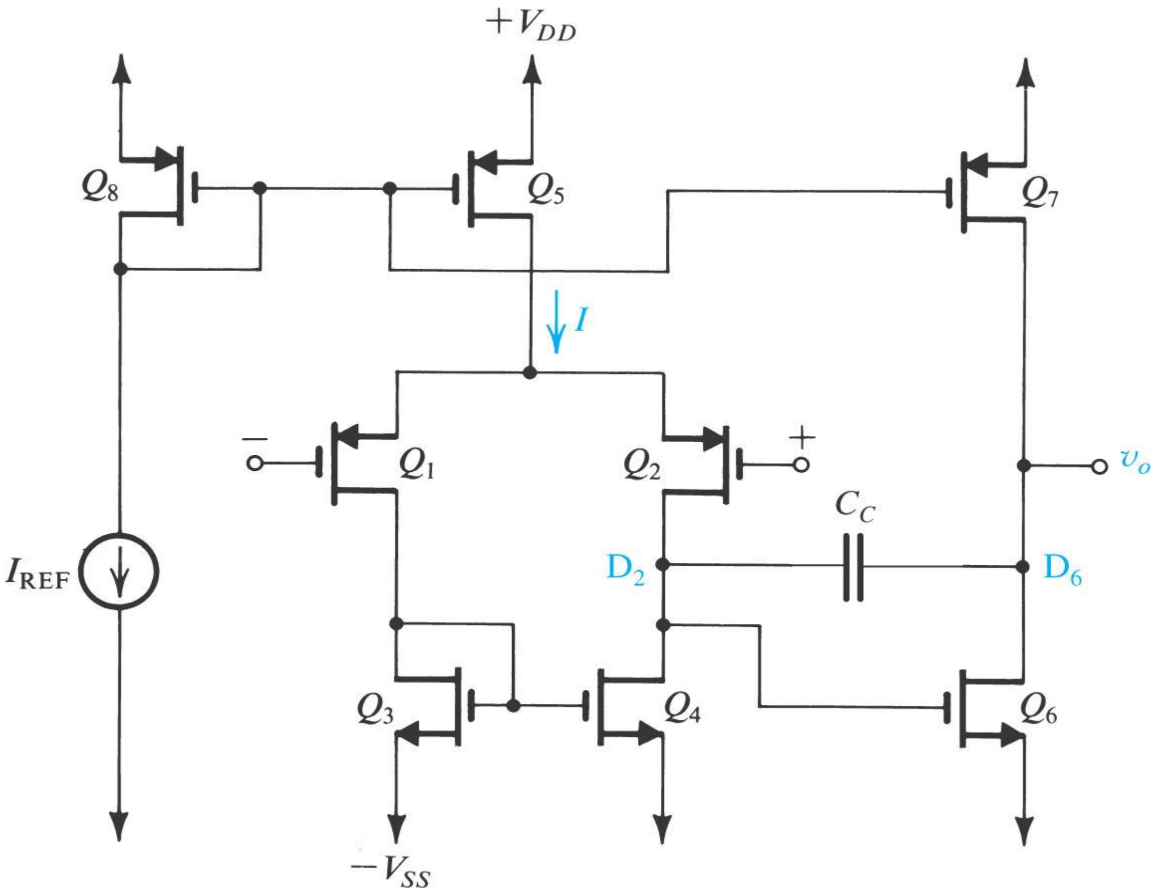


Figure 31: Schematic of a two-stage CMOS operational amplifier

Further, $\mu_n C_{ox}$=200 $\mu A/V^2$, $\mu_p C_{ox}$ =60 $\mu A/V^2$, V_{THN}=0.7 V, V_{THP}=-0.8 V, V_{AN} =10 V, V_{AP} =12 V, V_{DD} =V_{SS} =1.8 V, and I_{REF} = 120 μA.

[1] Figure 8.41, *Microelectronic Circuits* by Sedra and Smith, 6th edn., ©2010 , Oxford University Press Inc, ch.8.

Inspection of Fig.31 reveals that the OP-AMP has a DA as the signal input stage (Q_1, Q_2). The devices are PMOS transistors. A PMOS current mirror system (Q_5, Q_7, Q_8) *supplies the DC bias* current to the amplifying stages.

The DA has an NMOS current mirror as active load. The stage that follows the DA is an NMOS-CS amplifier (Q_6) with a PMOS (Q_7) current mirror as *active load.*

The capacitor C_C provides *frequency compensation* to ensure stable operation of the OP-AMP when connected in a negative-feedback for signal processing. The concept of frequency compensation will be discussed in chapter 3 of this note-pack.

Since the voltage gain depends upon g_m of the signal-driven transistor(s) and the output resistances of the signal-driven transistor and of the transistor forming the active load (i.e., r_{op}, r_{on}), we need to find the pertinent g_m values (i.e., of Q_1,Q_2,Q_6 –these are driven by the signal),and the output resistances of Q_2, Q_4, Q_6, and Q_7. The g_m and output resistance values depend upon the DC bias current. So we need to find the bias currents through the different stages (a stage is a column of transistors in the schematic).

Thus, considering that Q_8, Q_5 and Q_7 form current mirrors and that the *W/L* values for these are identical (see the Table) we conclude that I_5=I_7 =I_{REF} =120 μA.

Since I_5 divides equally between Q_1 and Q_2, we can determine I_1=I_2 =I_{REF}/2=60 μA. Since Q_3 is in series with Q_1, and likewise Q_4 is with Q_2, we know I_3 =I_4=I_1=I_2= 60 μA. Similarly, I_6 =I_7 =120 μA.

Using the square-law equation for the drain current in the MOST, i.e., $I_D = (1/2)\mu C_{ox}(W/L)V_{ov}^2$, where V_{ov} =|V_{GS}|-|V_{TH}|, we can determine the following quantities

<u>For Q_1, Q_2</u> :

I_D=120/2 μA, $\mu_n C_{ox}$=200 $\mu A/V^2$ (for NMOS), *W/*L = 20/0.5, V_{OV} =0.122 V.

Further, since the transconductance $g_m = \partial I_D / \partial V_{OV} = 2I_D / V_{OV}$, we get g_{mQ1}=g_{mQ2}=9.836×10^{-4} mho.

<u>For Q_2,Q_4 :</u>

The output resistances are dependent upon the *Early* voltage and DC bias current. Thus, $r_{o2} = V_{AN} / I_{DQ2}$ =166.67 $k\Omega$. Similarly, $r_{o4} = V_{AP} / I_{DQ4}$ =200 $k\Omega$.

Then signal voltage gain of stage#1 (i.e., Q_2, Q_4 pair) is $-g_{mQ2} \times r_{o2} \parallel r_{o4}$ = -89.42 V/V

For Q_6, Q_7 :

I_{DQ7}= 120 μA (by current mirroring principle, and since $(W/L)_{Q7} = (W/L)_{Q8}$).

Also, I_{DQ6} = 120 μA (since Q_6, Q_7 are in series).

For Q_6 , V_{OV} =0.245 V, $g_{mQ6} = 9.796 \times 10^{-4}$, r_{o6} =83.33 $k\Omega$.

For Q_7 , r_{07} =100 $k\Omega$.

The signal voltage gain of stage#2 (i.e., Q_6 , Q_7 pair) is $-g_{mQ6} \times r_{o6} \parallel r_{o7}$ = -44.53 V/V

Overall voltage gain of the two stage OP-AMP= -89.42 $\times$ (-44.53)=3989.92 V/V.

The above serves as an example to calculate the voltage gains in a cascade of multi-stage MOS amplifiers. The above gain is the gain of the two- stage OP-AMP as depicted in Figure 31.

The voltage gain is not the only parameter of interest for an OP-AMP. Several other performance characteristics, such as: (i) offset voltage, offset current, -3dB bandwidth, unity-gain bandwidth, CMRR, slew rate, settling time, power supply rejection ratio (PSRR), input common mode range (CMR), total DC power consumption, harmonic distortion, noise figure etc., are important. Interested students are encouraged to read more advanced books[2] and or take a course on, for example, *introduction to analog VLSI*.

2.3.3.2: MOS based Operational Amplifier (a second example)[3]

[2] See the list at the end of this chapter

[3] *Analog IC design: the current-mode approach,* Edited by C. Toumazou, F.J. Lidgey & D.G. Haigh © April 1990: Peter Peregrinus Ltd., London, United Kingdom, ISBN 0 86341 215 7

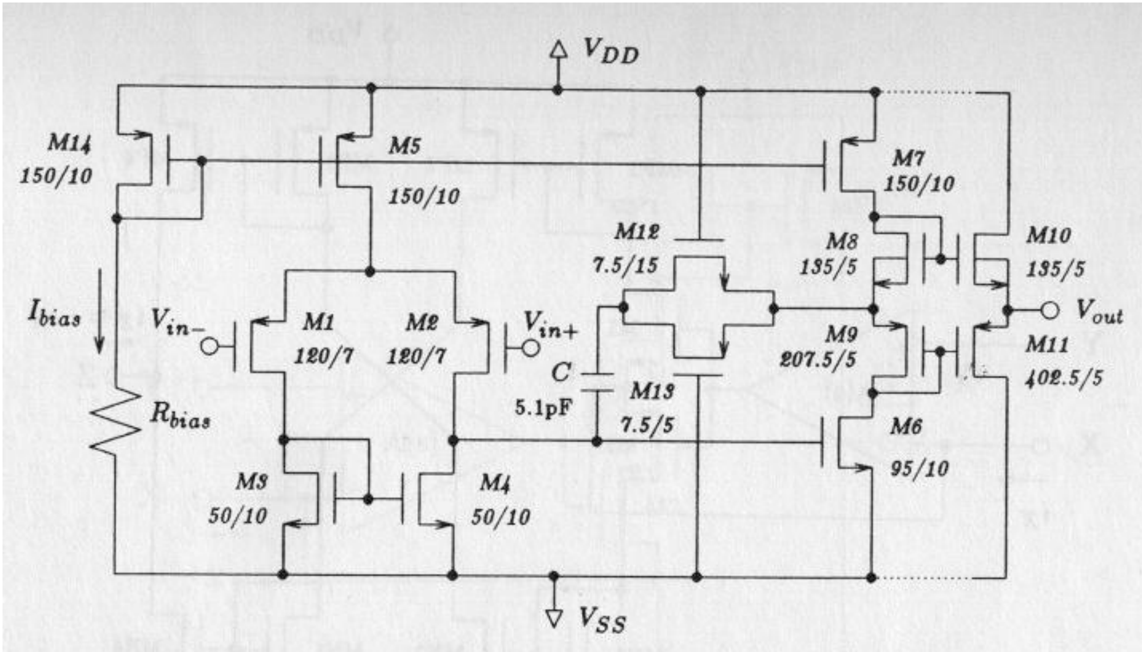


Figure 32: A CMOS OP-AMP with a class AB output stage.

Discussion: Figure 32 presents a three-stage OP-AMP including a class AB output stage. The output stage offers a low output impedance – an important criterion for a voltage amplifier (i.e., VCVS).

The input DA is comprised of two PMOS transistors (M1,M2), with PMOS current mirror (M14,M5) bias source and NMOS (M3,M4) current mirror (active) load.

The capacitor C together with transistors M12, M13 form a series C,R frequency compensation circuit.

The second stage of amplification comes from the NMOS transistor M6 which has an active load comprised of the diode connected transistors (M8,M9) in series with the current mirror load (M7).

Transistors M10 (NMOS), M11 (PMOS) together with the diode connected transistors (M8,M9) from a class AB output stage. Since the output is taken from the source terminals of M10, M11, the output resistance will be small.

The *W*/*L* data shown are in microns.

2.3.3.3: <u>BJT based OP-AMP</u>

Please refer to *Microelectronic Circuits* by Sedra and Smith, 6^{th} edn., ©2010 , Oxford University Press Inc, ch.8, p.657-663.

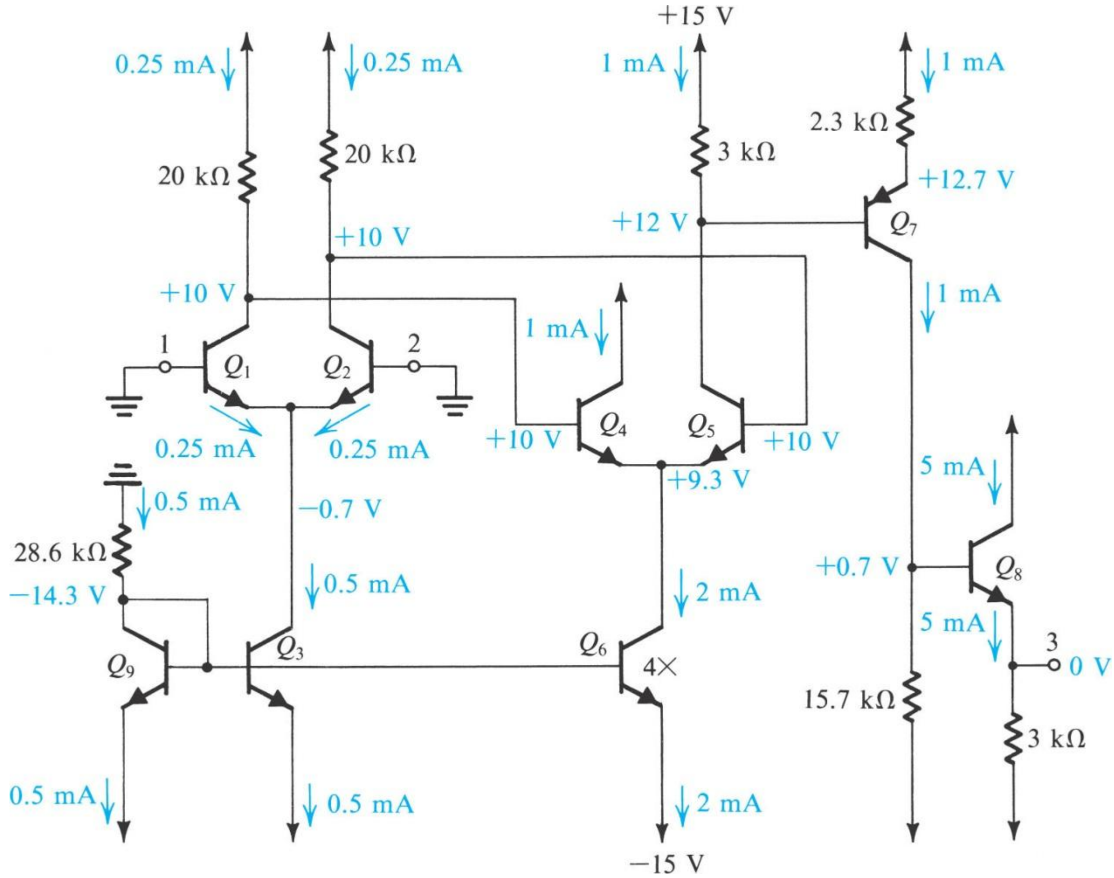
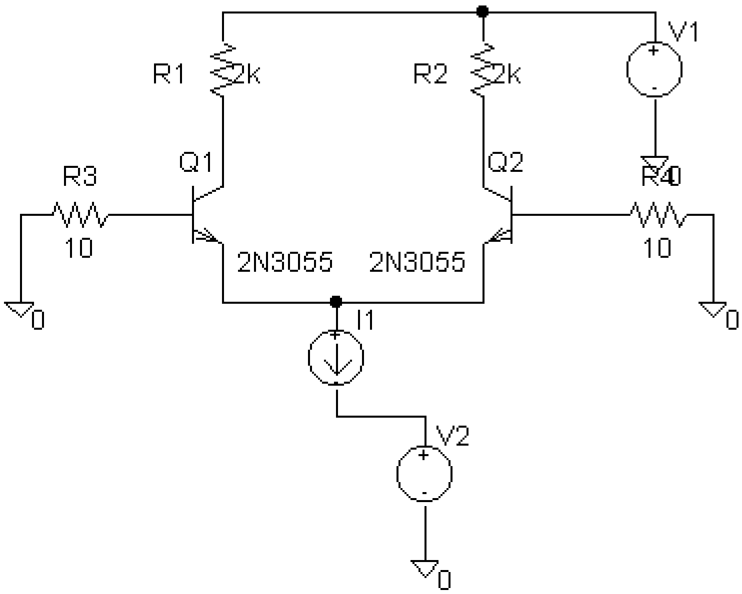


Figure 33: A four-stage BJT OP-AMP

For analyzing the circuit operation, and calculating the voltage gain and input/output resistances, please read ref#1, p.657-663.

2.4 : Practice Exercises

Q.1: Consider the schematic of a differential amplifier below. The output listing for the network in pSPICE format is appended. Using this listing do the following:



❖ Draw an ac equivalent circuit model for the amplifier.

❖ Using necessary theoretical formula and the relevant component values from the output listing, find the (a) voltage gain, and (b) input resistance for small signal operation.

* Schematics Netlist *

R_R1 $N_0002 $N_0001 2k

R_R2 $N_0003 $N_0001 2k

V_V1 $N_0001 0 DC 5

V_V2 $N_0004 0 DC -5

Q_Q1 $N_0002 $N_0005 $N_0006 Q2N3055

R_R4 $N_0007 0 10

R_R3 0 $N_0005 10

Q_Q2 $N_0003 $N_0007 $N_0006 Q2N3055

I_I1 $N_0006 $N_0004 DC 5m

SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
($N_0001)	5.0000	($N_0002)	.1730				
($N_0003)	.1730	($N_0004)	-5.0000				
($N_0005)	-864.9E-06	($N_0006)	-.5602				
($N_0007)	-864.9E-06						

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
V_V1	-4.827E-03
V_V2	5.000E-03

TOTAL POWER DISSIPATION 4.91E-02 WATTS

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**** 12/31/103 11:09:01 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\pe_el312lect_ch2.sch

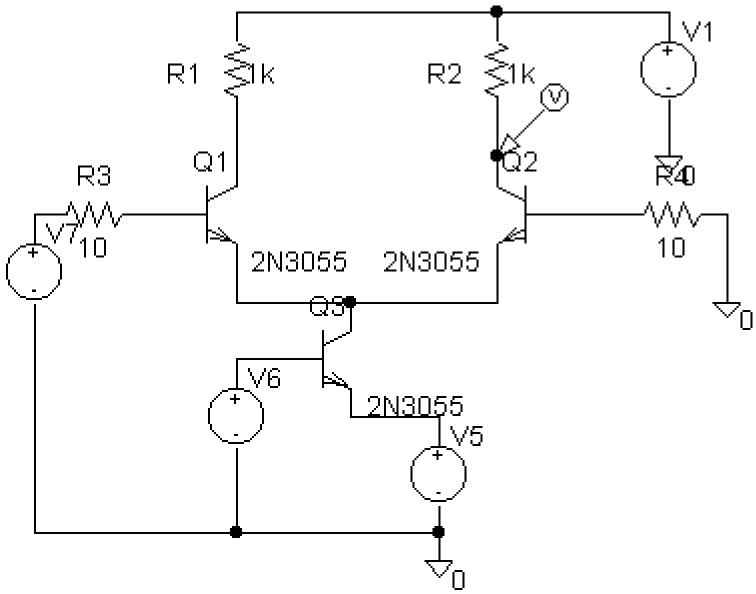
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2
MODEL	Q2N3055	Q2N3055
IB	8.65E-05	8.65E-05
IC	2.41E-03	2.41E-03
VBE	5.59E-01	5.59E-01
VBC	-1.74E-01	-1.74E-01
VCE	7.33E-01	7.33E-01
BETADC	2.79E+01	2.79E+01
GM	9.32E-02	9.32E-02
RPI	4.59E+02	4.59E+02
RX	1.00E-01	1.00E-01
RO	2.08E+04	2.08E+04
CBE	4.48E-09	4.48E-09
CBC	2.58E-10	2.58E-10
CJS	0.00E+00	0.00E+00
BETAAC	4.28E+01	4.28E+01
CBX	0.00E+00	0.00E+00
FT	3.13E+06	3.13E+06

Q.2: For the network below, the output listing is appended. Repeat the work done in Q.1 above.



* Schematics Netlist *

Q_Q1 $N_0002 $N_0001 $N_0003 Q2N3055

R_R4 $N_0004 0 10

Q_Q3 $N_0003 $N_0005 $N_0006 Q2N3055

R_R1 $N_0002 $N_0007 1k

V_V1 $N_0007 0 DC 5

R_R3 $N_0008 $N_0001 10

R_R2 $N_0009 $N_0007 1k

V_V5 $N_0006 0 DC -5

V_V6 $N_0005 0 DC -4.4295

V_V7 $N_0008 0 DC 0 AC 1

Q_Q2 $N_0009 $N_0004 $N_0003 Q2N3055

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
($N_0001)	-719.5E-06	($N_0002)	3.0812				
($N_0003)	-.5527	($N_0004)	-719.5E-06				
($N_0005)	-4.4295	($N_0006)	-5.0000				
($N_0007)	5.0000	($N_0008)	0.0000				
($N_0009)	3.0812						

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
V_V1	-3.838E-03
V_V5	4.096E-03

V_V6 -1.149E-04
V_V7 -7.195E-05

TOTAL POWER DISSIPATION 3.92E-02 WATTS

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**** 12/31/103 11:42:49 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\pe_el312lect_ch2_2.sch

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

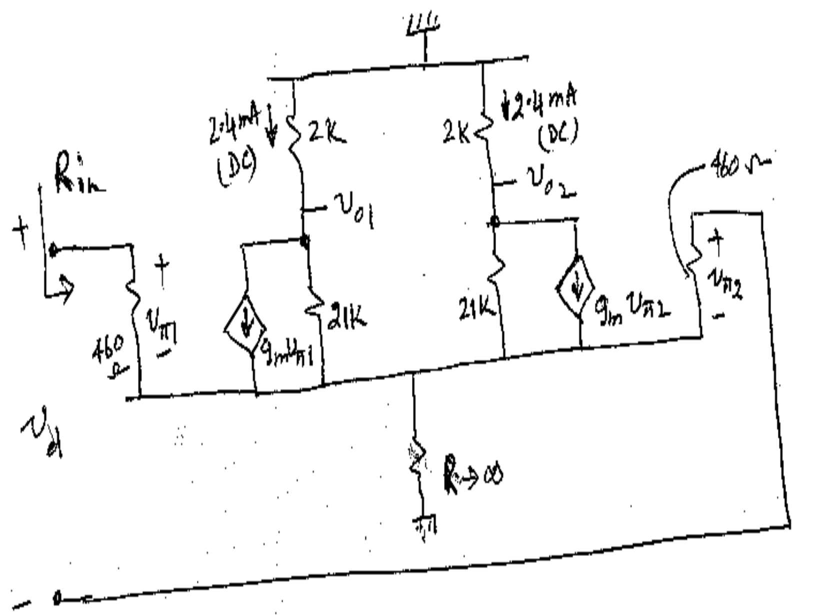
****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q3	Q_Q2
MODEL	Q2N3055	Q2N3055	Q2N3055
IB	7.19E-05	1.15E-04	7.19E-05
IC	1.92E-03	3.98E-03	1.92E-03
VBE	5.52E-01	5.71E-01	5.52E-01
VBC	-3.08E+00	-3.88E+00	-3.08E+00
VCE	3.63E+00	4.45E+00	3.63E+00

BETADC	2.67E+01	3.46E+01	2.67E+01
GM	7.41E-02	1.54E-01	7.41E-02
RPI	5.64E+02	3.35E+02	5.64E+02
RX	1.00E-01	1.00E-01	1.00E-01
RO	2.77E+04	1.35E+04	2.77E+04
CBE	3.73E-09	6.86E-09	3.73E-09
CBC	1.60E-10	1.51E-10	1.60E-10
CJS	0.00E+00	0.00E+00	0.00E+00
BETAAC	4.18E+01	5.15E+01	4.18E+01
CBX	0.00E+00	0.00E+00	0.00E+00
FT	3.03E+06	3.49E+06	3.03E+06

* Q3: The ac equivalent circuit of a BJT differential amplifier is shown below. Determine the input impedance and differential voltage gain $(v_{01}-v_{02})/v_d$



Given

$h_{fe} = 43$

$g_m = \frac{I_{DC}}{V_T}$

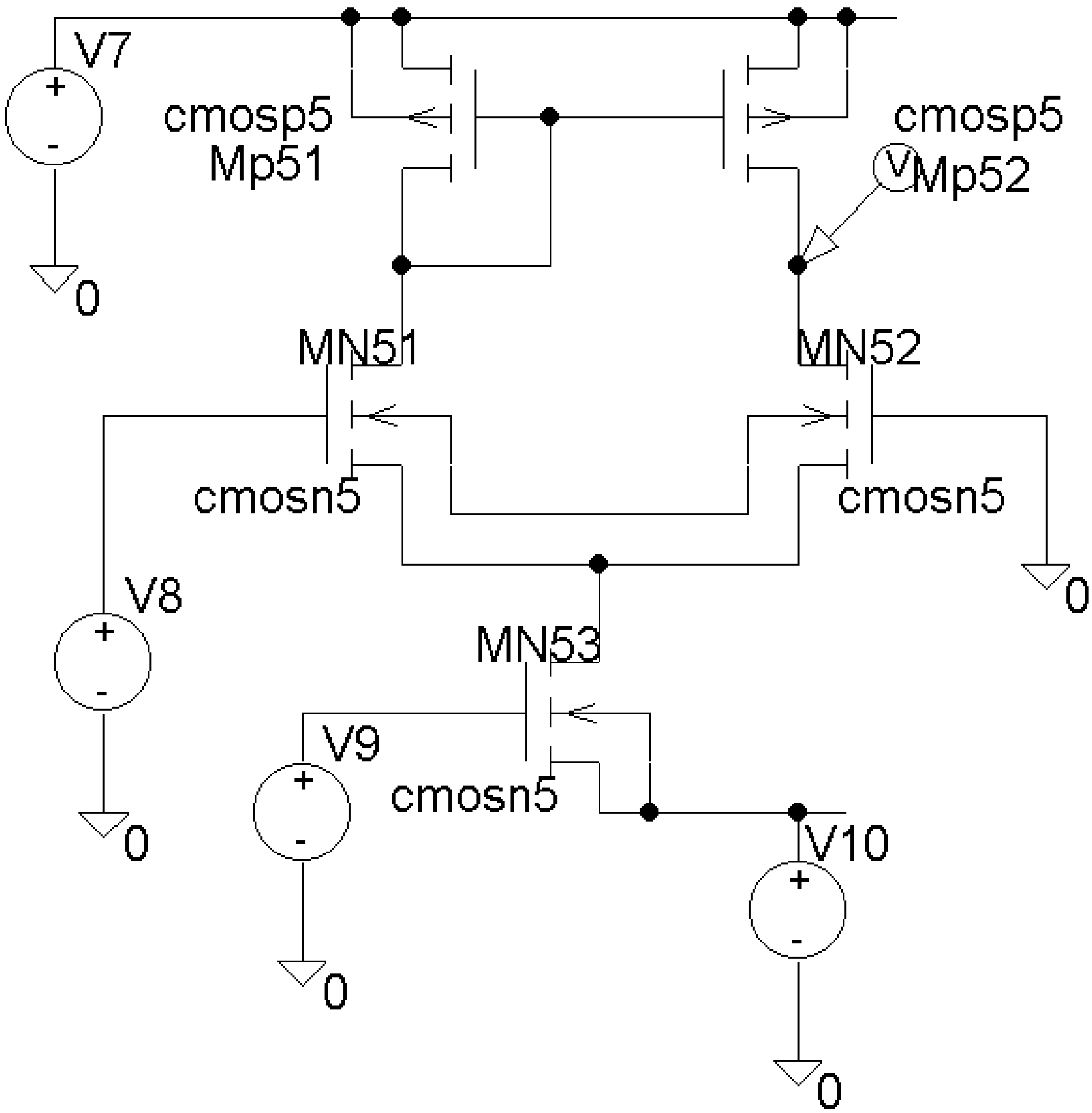
$V_T = \frac{kT}{q} \approx 25mV$ at room temperature.

Q4 Repeat Q3 when $R = 14 K\Omega$

Q.5: Deleted

Q.6: Consider the schematic and the output file listing for the differential amplifier shown below.

- ❖ Draw the ac equivalent circuit for the amplifier using standard symbols (i.e., g_m, r_{ds} ..)
- ❖ Estimate the voltage gain of the amplifier using the data form the output listing and relevant formula learned in your lecture class. The output node is where the voltage probe is attached.



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* Schematics Netlist *

M_Mp51 $N_0001 $N_0001 $N_0002 $N_0002 cmosp5

+ L=2u

+ W=18u

M_Mp52 $N_0003 $N_0001 $N_0002 $N_0002 cmosp5

+ L=2u

+ W=18u

```
M_MN51        $N_0001 $N_0005 $N_0004 $N_0006 cmosn5
+ L=2u
+ W=5u
M_MN52        $N_0003 0 $N_0004 $N_0006 cmosn5
+ L=2u
+ W=5u
M_MN53        $N_0004 $N_0008 $N_0007 $N_0007 cmosn5
+ L=2u
+ W=10u
V_V10        $N_0007 0 DC -1.5
V_V9        $N_0008 0 DC -.5
V_V7        $N_0002 0 DC 1.5
V_V8        $N_0005 0 DC 0 AC 1


****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE
($N_0001)     .2325                ($N_0002)    1.5000

($N_0003)     .2325                ($N_0004)    -.9651

($N_0005)    0.0000                ($N_0006)    -.8457

($N_0007)   -1.5000                ($N_0008)    -.5000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V10        4.951E-05
    V_V9         0.000E+00
```

V_V7 -4.951E-05
V_V8 0.000E+00

TOTAL POWER DISSIPATION 1.49E-04 WATTS

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**** 01/02/104 09:58:50 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\CMR_study.sch

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

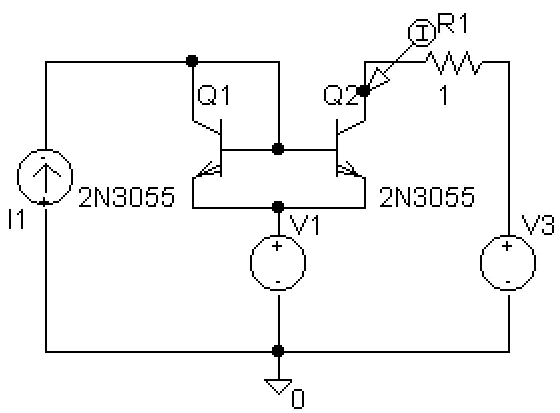
****

**** MOSFETS

NAME	M_Mp51	M_Mp52	M_MN51	M_MN52	M_MN53
MODEL	cmosp5	cmosp5	cmosn5	cmosn5	cmosn5
ID	-2.48E-05	-2.48E-05	2.48E-05	2.48E-05	4.95E-05
VGS	-1.27E+00	-1.27E+00	9.65E-01	9.65E-01	1.00E+00
VDS	-1.27E+00	-1.27E+00	1.20E+00	1.20E+00	5.35E-01
VBS	0.00E+00	0.00E+00	1.19E-01	1.19E-01	0.00E+00
VTH	-9.43E-01	-9.43E-01	6.46E-01	6.46E-01	6.82E-01
VDSAT	-3.20E-01	-3.20E-01	2.96E-01	2.96E-01	2.99E-01
GM	1.31E-04	1.31E-04	1.29E-04	1.29E-04	2.59E-04
GDS	1.10E-07	1.10E-07	2.46E-07	2.46E-07	5.42E-07
GMB	3.28E-05	3.28E-05	3.68E-05	3.68E-05	8.62E-05
CBD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGSOV	4.31E-15	4.31E-15	1.53E-15	1.53E-15	3.05E-15

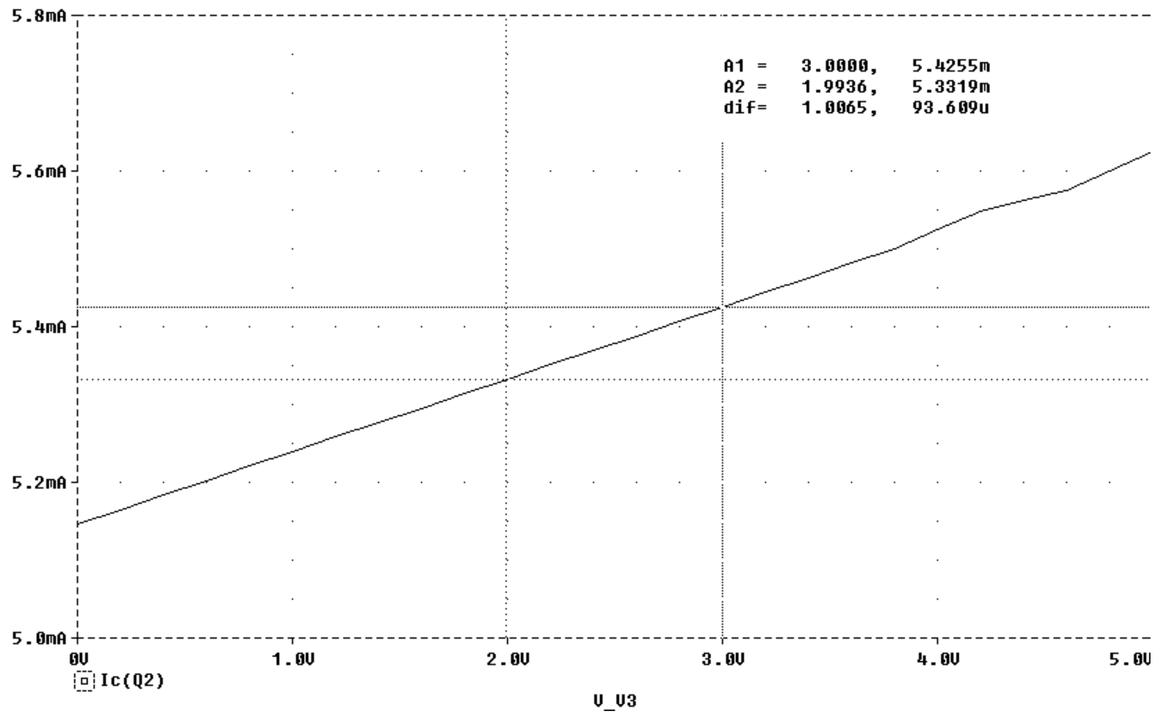
CGDOV	4.31E-15	4.31E-15	1.53E-15	1.53E-15	3.05E-15
CGBOV	7.25E-16	7.25E-16	7.67E-16	7.67E-16	7.67E-16
CGS	8.33E-14	8.33E-14	2.28E-14	2.28E-14	4.57E-14
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

Q.7: The figure below shows a BJT-based simple current mirror. The DC bias current in Q1 is 5 mA. The schematic represents a test set up to measure the output impedance of



Basic current mirror

the current mirror. The relevant graphical behavior is shown below. The Y-axis is the current into the collector pin of Q2 (the output transistor). What is the output resistance of this mirror?



Q.8: The simulation result for the above current mirror is appended below. What is the expected output resistance for the mirror? Use the pertinent data for the transistors to determine the output resistance. Compare this with the value you get from the above graph.

* Schematics Netlist *

I_I1 0 $N_0001 DC 5m
Q_Q1 $N_0001 $N_0001 $N_0002 Q2N3055
V_V1 $N_0002 0 DC -5
Q_Q2 $N_0003 $N_0001 $N_0002 Q2N3055
V_V3 $N_0004 0 DC 5
R_R1 $N_0003 $N_0004 1

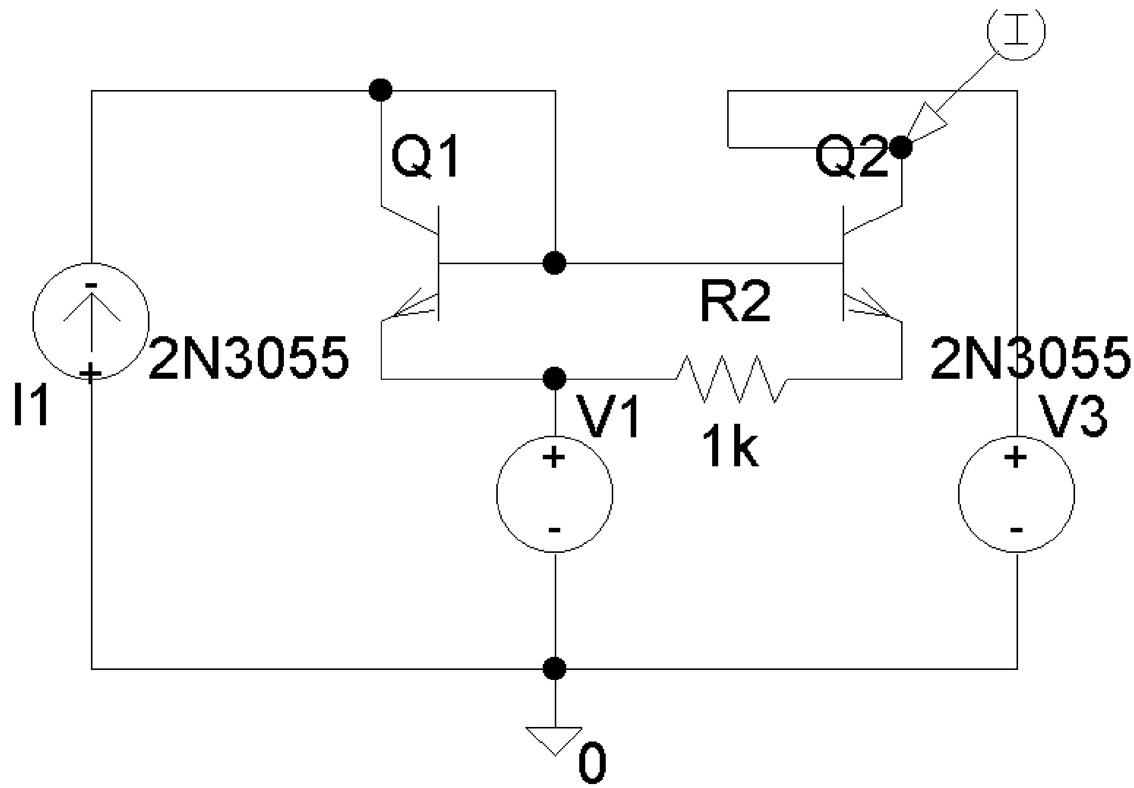
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

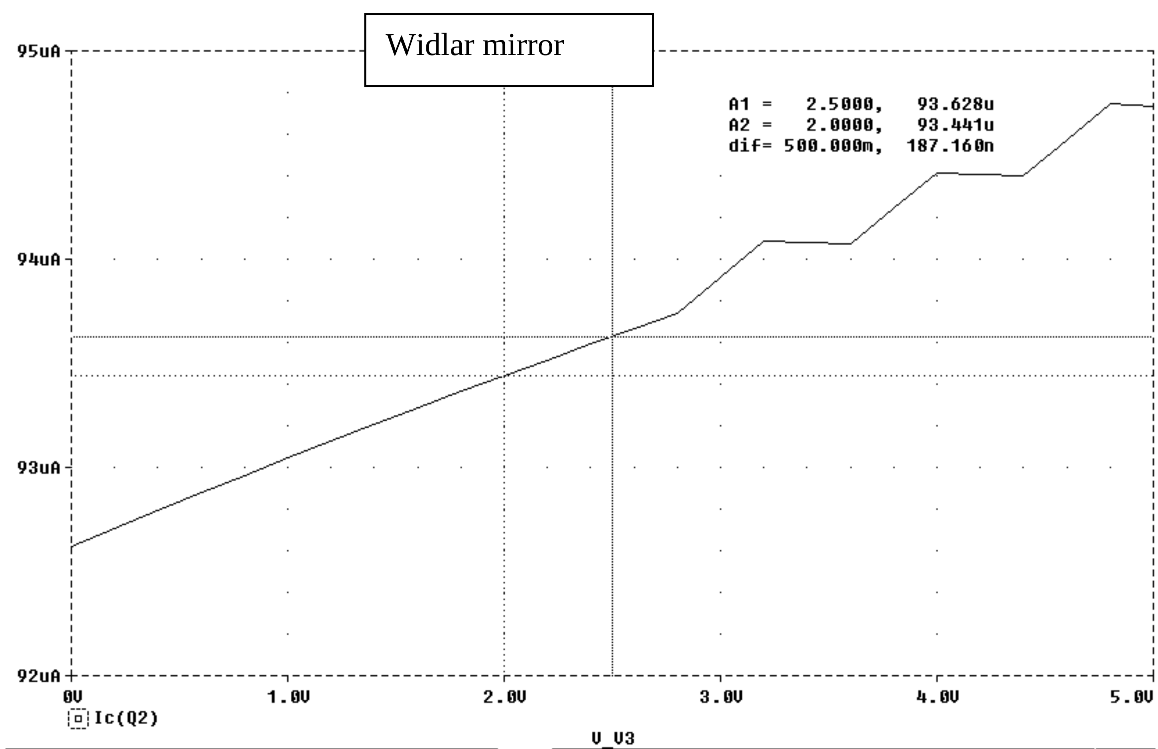
****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2
MODEL	Q2N3055	Q2N3055
IB	1.36E-04	1.36E-04
IC	4.73E-03	5.62E-03
VBE	5.77E-01	5.77E-01
VBC	0.00E+00	-9.42E+00
VCE	5.77E-01	9.99E+00
BETADC	3.48E+01	4.14E+01
GM	1.83E-01	2.17E-01
RPI	2.78E+02	2.78E+02
RX	1.00E-01	1.00E-01
RO	1.06E+04	1.06E+04
CBE	7.99E-09	9.33E-09
CBC	2.76E-10	1.16E-10
CJS	0.00E+00	0.00E+00
BETAAC	5.07E+01	6.03E+01
CBX	0.00E+00	0.00E+00
FT	3.52E+06	3.65E+06

Q.9: For the Widlar mirror below, the output current voltage characteristic is shown in the accompanying graph. Determine the output resistance.


Q1
Q2
R2
2N3055
2N3055
I1
V1
1k
V3
0


Widlar mirror
A1 = 2.5000, 93.628u
A2 = 2.0000, 93.441u
dif= 500.000m, 187.160n
95uA
94uA
93uA
92uA
0V
1.0V
2.0V
3.0V
4.0V
5.0V
Ic(Q2)
V_V3

Q.10: The simulated output listing for the above mirror is attached below. Use necessary formula and the relevant data to calculate the R_{out}. Compare with the value obtained from the graph.

Schematics Netlist *

```
Q_Q1        $N_0001 $N_0001 $N_0002 Q2N3055
V_V3        $N_0003 0 DC 5
V_V1        $N_0002 0 DC -5
R_R2        $N_0002 $N_0004  1k
Q_Q2        $N_0003 $N_0001 $N_0004 Q2N3055
I_I1        0 $N_0001 DC 5m

****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

*****************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE


($N_0001)   -4.4225                ($N_0002)   -5.0000

($N_0003)    5.0000                ($N_0004)   -4.8937

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V3       -9.473E-05
    V_V1        5.095E-03

    TOTAL POWER DISSIPATION   2.59E-02  WATTS

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**** 01/03/104 10:06:09 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****
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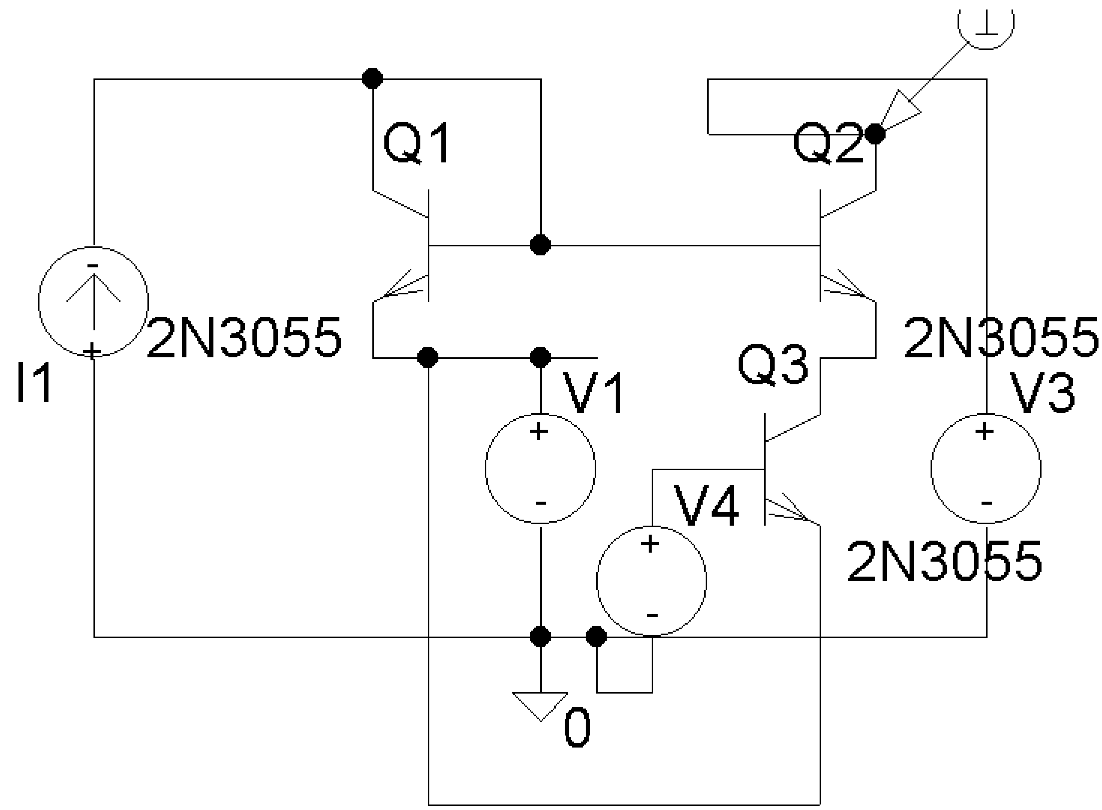
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

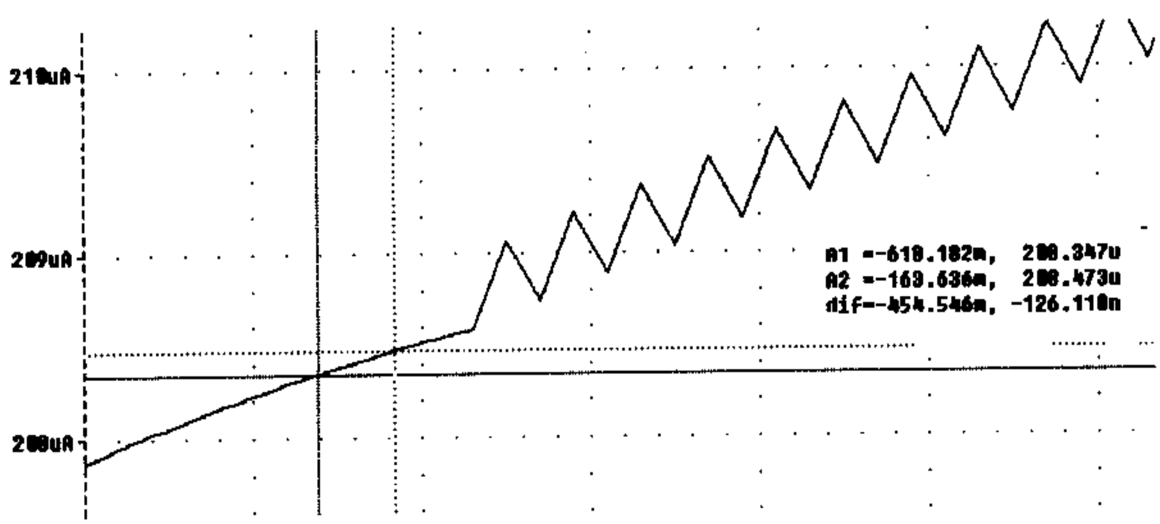
NAME	Q_Q1	Q_Q2
MODEL	Q2N3055	Q2N3055
IB	1.38E-04	1.16E-05
IC	4.85E-03	9.47E-05
VBE	5.78E-01	4.71E-01
VBC	0.00E+00	-9.42E+00
VCE	5.78E-01	9.89E+00
BETADC	3.51E+01	8.19E+00
GM	1.87E-01	3.66E-03
RPI	2.73E+02	4.07E+03
RX	1.00E-01	1.00E-01
RO	1.03E+04	6.27E+05
CBE	8.17E-09	9.22E-10
CBC	2.76E-10	1.16E-10
CJS	0.00E+00	0.00E+00
BETAAC	5.10E+01	1.49E+01
CBX	0.00E+00	0.00E+00
FT	3.53E+06	5.62E+05

Q.11 In order to enhance the output resistance of the Widlar mirror, the resistance R2 is replaced by a BJT device as shown below. Draw the ac equivalent circuit for the modifier current mirror. Label the circuit components clearly.



The output I-V characteristic is shown below. Determine the output resistance and compare with the value predicted by the theoretical formula.

You have to use the component values given in the output listing.



* Schematics Netlist *

```
Q_Q1        $N_0001 $N_0001 $N_0002 Q2N3055
V_V3        $N_0003 0 DC 5
V_V1        $N_0002 0 DC -5
I_I1      0 $N_0001 DC 5m
Q_Q2        $N_0003 $N_0001 $N_0004 Q2N3055
Q_Q3        $N_0004 $N_0005 $N_0002 Q2N3055
V_V4        $N_0005 0 DC -4.5
```

```
SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
******************************************************************************
 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE


($N_0001)   -4.4225                  ($N_0002)   -5.0000

($N_0003)    5.0000                  ($N_0004)   -4.9144

($N_0005)   -4.5000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_V3        -2.105E-04
    V_V1         5.235E-03
    V_V4        -2.453E-05

    TOTAL POWER DISSIPATION   2.71E-02  WATTS

_**** 01/03/104 10:33:30 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****
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**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C
****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2	Q_Q3
MODEL	Q2N3055	Q2N3055	Q2N3055
IB	1.38E-04	1.80E-05	2.45E-05
IC	4.84E-03	2.10E-04	2.29E-04
VBE	5.78E-01	4.92E-01	5.00E-01
VBC	0.00E+00	-9.42E+00	4.14E-01
VCE	5.78E-01	9.91E+00	8.56E-02
BETADC	3.51E+01	1.17E+01	9.32E+00
GM	1.87E-01	8.13E-03	8.95E-03
RPI	2.73E+02	2.55E+03	2.11E+03
RX	1.00E-01	1.00E-01	1.00E-01
RO	1.03E+04	2.82E+05	2.91E+03
CBE	8.16E-09	1.11E-09	1.16E-09
CBC	2.76E-10	1.16E-10	6.93E-10
CJS	0.00E+00	0.00E+00	0.00E+00
BETAAC	5.10E+01	2.07E+01	1.89E+01
CBX	0.00E+00	0.00E+00	0.00E+00
FT	3.53E+06	1.06E+06	7.69E+05

Q.12: By a mistake the bias voltage at the base of Q3 was altered from –4.5 V to –4.4 V. What effect will this have in the output resistance of the current mirror? The simulation output listing is attached below. Calculate the output resistance and compare it with the value found in Q.11 above. Discuss your results.

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) -4.4229 ($N_0002) -5.0000

($N_0003) 5.0000 ($N_0004) -4.9837

($N_0005) -4.4000

VOLTAGE SOURCE CURRENTS
NAME CURRENT

V_V3 -3.024E-03
V_V1 1.038E-02
V_V4 -2.352E-03

TOTAL POWER DISSIPATION 5.67E-02 WATTS

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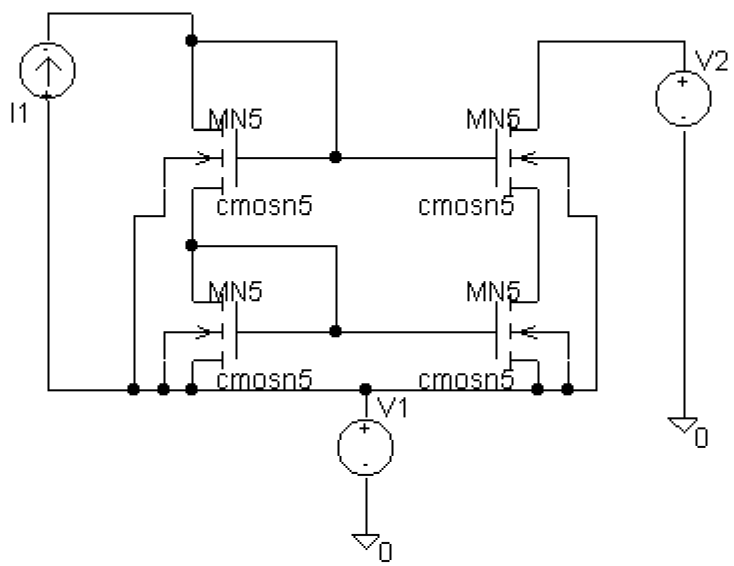
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

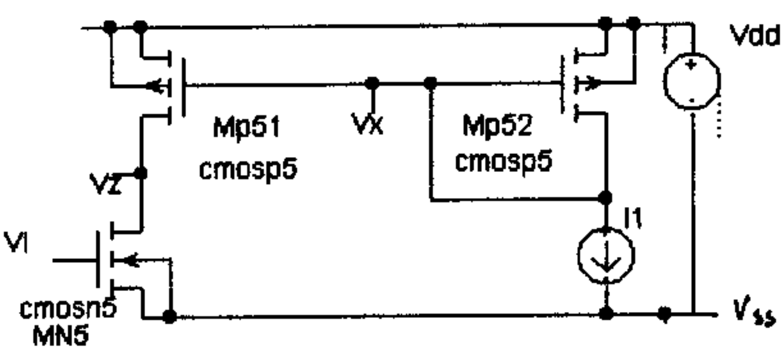
NAME	Q_Q1	Q_Q2	Q_Q3
MODEL	Q2N3055	Q2N3055	Q2N3055
IB	1.37E-04	8.97E-05	2.35E-03
IC	4.77E-03	3.02E-03	3.11E-03
VBE	5.77E-01	5.61E-01	6.00E-01
VBC	0.00E+00	-9.42E+00	5.84E-01
VCE	5.77E-01	9.98E+00	1.63E-02
BETADC	3.49E+01	3.37E+01	1.32E+00
GM	1.84E-01	1.17E-01	2.01E-01
RPI	2.76E+02	4.41E+02	1.38E+02
RX	1.00E-01	1.00E-01	1.00E-01
RO	1.05E+04	1.97E+04	4.24E+00
CBE	8.06E-09	5.41E-09	1.79E-08
CBC	2.76E-10	1.16E-10	2.33E-07
CJS	0.00E+00	0.00E+00	0.00E+00
BETAAC	5.08E+01	5.15E+01	2.78E+01
CBX	0.00E+00	0.00E+00	0.00E+00
FT	3.52E+06	3.37E+06	1.28E+05

Q.13: The schematic below presents a cascode current mirror using NMOS transistors.



Draw the ac equivalent circuit for the system and indicate in the circuit how you could determine the output resistance of the current mirror.

Q.14: Consider the NMOS amplifier with PMOS active load as shown below. Assume that the I-V equation is of the form I(NMOS)= $K_n(V_{GS}-V_{TN})^2(1+\lambda_n V_{DS})$ and I(PMOS)=$K_p(V_{SG}-|V_{TP}|)^2(1+\lambda_p V_{SD})$. Given K_n=90 μA/V^2, K_p=30 μA/V^2, V_{TN}=1 V, VTP= -1 V, λ_n=0.01 V^{-1}, λ_p=0.02 V^{-1}, V_{dd}=10 V, V_{SS}=-3V, and I1=200 μA, find the DC voltages at various nodes (i.e., V_x, V_z) of the system. Assume V_i =0 V. The PMS transistors are identical.



Q.15,16 : deleted

Q.17. In a MOS differential amplifier using current mirror load, the voltage gain is given by $g_m / (g_{dp} + g_{dn})$ where $g_m = \sqrt{2 \mu C_{ox} \frac{W}{L} I_{DC}}$ for the amplifying device and $g_{dp} = \frac{1}{r_{op}}$, $g_{dn} = \frac{1}{r_{on}}$. The suffixes 'p', 'n' standing for PMOS and NMOS transistors.

Given $\mu C_{ox} = 100\ \mu A/V^2$, $I_{DC} = 100\ \mu A$, $V_{TN} = 1V$, $V_{AP} = 20V$, $V_{An} = 30V$.

Design the aspect ratio W/L of the amplifying transistors for a gain of 40.

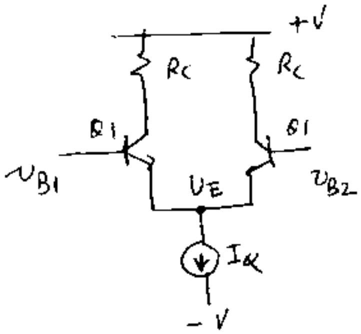
Soln:

$$40 = \frac{g_m}{g_{dp} + g_{dn}} \qquad g = \frac{1}{r}\ ;\ r = \frac{V_A}{I_{DC}}$$

$$40 = \frac{\sqrt{2 \times 100 \times 10^{-6}\ \frac{W}{L} \times 100 \times 10^{-6}}}{100 \times 10^{-6} \left(\frac{1}{20} + \frac{1}{30}\right)}$$

Solving $\sqrt{\frac{2W}{L}} = \frac{10}{3}$; $\frac{W}{L} = \frac{50}{9}$

Q.18: For the BJT DA, find an expression for the common emitters node voltage v_E when the DA has two large signal (, input voltages v_{B1}, v_{B2}.



Ans. For large signal operation you use the exponential equation for the BE junctions at each transistor.

For Q_1, $i_{E1} = I_s e^{(v_{B1}-v_E)/nV_T} \simeq I_s e^{(v_{B1}-v_E)/V_T}$ assuming $n=1$

For Q_2, $i_{E2} = I_s e^{(v_{B2}-v_E)/V_T}$,

$V_T \rightarrow$ thermal voltage $\frac{kT}{q}$

But by KCL at v_E node, $i_{E1} + i_{E2} = I_Q$

$$\text{So} \quad I_Q = I_s \cdot e^{\frac{v_{B1}-v_E}{V_T}} + I_s e^{\frac{v_{B2}-v_E}{V_T}}$$, assuming identical transistors.

$$= I_s e^{-\frac{v_E}{V_T}} \cdot \left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)$$

$$\text{So} \quad e^{-v_E/V_T} = \frac{I_Q}{I_s} \cdot \frac{1}{\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)}$$

Taking natural log on both sides

$$-\frac{v_E}{V_T} = \ln\left(\frac{I_Q}{I_s}\right) - \ln\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)$$

$$\text{or} \quad v_E = V_T \left[\ln\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right) - \ln\left(\frac{I_Q}{I_s}\right)\right].$$

Q: What if $v_{B1} = \frac{v_d}{2}$; $v_{B2} = -\frac{v_d}{2}$? and v_d is very small } TRY YOURSELF!

Additional references:

2. *CMOS Circuit Design, Layout and Simulation*, by R. Jacob Baker, IEEE Press, © 2005 by the Institute of Electrical and Electronics Engineers, ISBN 0-471-70055-X

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4. *Analysis and Design of Analog Integrated Circuits*, by P.R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, John Wiley & Sons, Inc., ©2001, ISBN 0-471-32168-0.

5. *Fundamentals of Microelectronics*, by Behzad Razavi, John Wiley & Sons, Inc., © 2008, ISBN 978-0-471-47846-1.