

If the transistors are identical, we can put $I_{s1} = I_{s2}$. Then $I_o = I_{REF}$.

In case of the MOS: $I_o = \frac{\mu C_{ox}}{2} \left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2$; $I_{REF} = \frac{\mu C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$. So $I_o = I_{REF} \frac{(W/L)_2}{(W/L)_1}$.

If $(W/L)_2 = (W/L)_1$; $I_o = I_{REF}$.

Obviously, the key factor that makes the mirroring operation possible is maintenance of same V_{BE} (for BJT) and same V_{GS} (for MOS) for the pair (reference generator, and the mirror) of devices concerned. DC currents of different levels can be easily generated by adopting the following arrangements (Figures 3(a)-(b)).

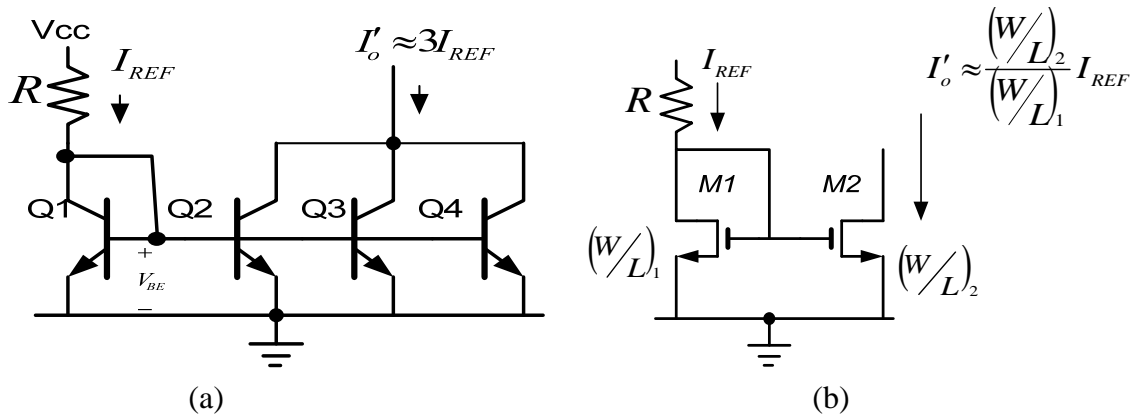


Figure 3: (a) BJT based current mirror with a gain of three (all BJTs identical), (b) MOS based current mirror with a gain equal to the aspect ratios (i.e., W/L values) of M1 and M2, the two NMOS are assumed to belong to same technology.

2.1.3: DC bias design in case of current source/mirror

To set up the reference current one has to employ a fixed DC power supply and a fixed resistance. Once this is done, the operation follows the equations already mentioned above. Let us consider two examples.

Example 2.1.3.1 : (BJT device):

$$I_{ref} = \frac{V_{CC} - V_B}{R}; I_C = I_S e^{(V_B - V_{EE})/V_T}, \text{ assuming } n=1$$

$$\text{KCL } I_{ref} - \frac{I_C}{\beta_1} - \frac{I_o}{\beta_2} = I_C; I_x = \frac{I_C}{\beta_1} + \frac{I_o}{\beta_2}, \text{ Further,}$$

$I_o = I_S e^{(V_B - V_{EE})/V_T}$. If I_o is given, I_S is known, and V_{EE} is given, we can find V_B . Using the KCL equations above and assuming $\beta_1 = \beta_2 = \beta$, we can write

$$\frac{V_{CC} - V_B}{R} - I_C \left(1 + \frac{1}{\beta}\right) - \frac{I_o}{\beta} = 0. \text{ Now, if } V_{CC} \text{ and } \beta \text{ are known,}$$

We can solve the above equation for R .
Finding R completes the DC design.

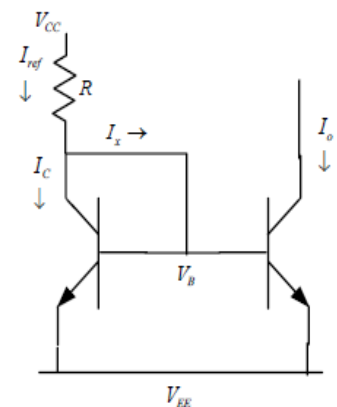


Figure 4 : Related to Ex 2.1.3.1

Note the following work, which includes the effect of V_{DS} in both the reference generator transistor and the mirroring transistor. Consider figure 8.

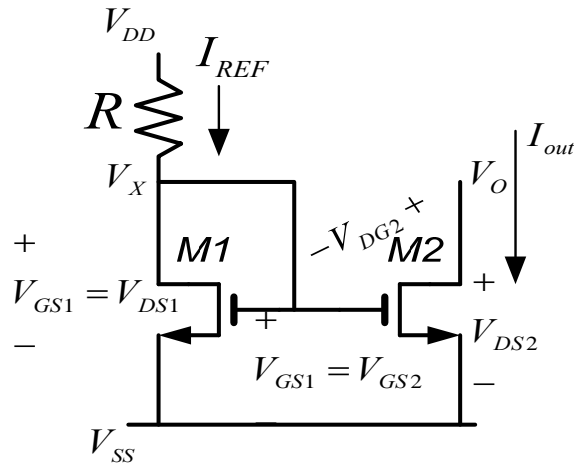


Figure 8: Illustrating the effect of unequal V_{DS} in the reference and the mirroring MOS transistors

$$I_{REF} = I_o(1 + \lambda V_{DS1}) = I_o(1 + \lambda V_{GS1}), \text{ since } V_{DS1} = V_{GS1} \text{ because of gate-drain connection.}$$

$$I_{MIRROR} = I_{out} = I_o(1 + \lambda V_{DS2}), \text{ where } V_{DS2} = V_{DG2} + V_{GS2} = V_{DG2} + V_{GS1}. \text{ Then } I_{REF} - I_{MIRROR} = -I_o \lambda V_{DG2}.$$

$$\text{Thus, } I_{MIRROR} = I_{REF} + I_o \frac{1}{V_A} V_{DG2} \approx I_{REF} \left(1 + \frac{V_{DG2}}{V_A}\right), \text{ assuming that } I_o \approx I_{REF}.$$

Now, since $V_{DG2} = V_{DS2} - V_{GS2}$, and $V_{DS2} = V_o - V_{SS}$ (see the schematic), one can finally write

$$I_{MIRROR} = I_{out} = I_{REF} \left(1 + \frac{V_o - V_{SS} - V_{GS2}}{V_A}\right). \text{ The current tracking error is } I_{REF} - I_{out}. \text{ Ideally this should}$$

be zero. (*quiz*: What will be the tracking error if $I_{REF} = I_o$ is not assumed?)

2.1.5 C: Effect of finite β in case of a BJT mirror

Because each BJT has a finite current gain β , a part of I_{REF} is diverted to the base of the reference generator transistor, making $I_C = I_{REF} - I_X$ (see Fig.9). The mirror transistor having same V_{BE} as the reference transistor will follow I_C of the reference transistor. Thus I_{OUT} of the mirror transistor differs from I_{REF} , introducing an error in tracking I_{REF} .

Tracking error: This is the difference between the ideal output bias current (i.e., assuming infinite β) and the actual output bias current (using finite β). Consider the following hints for the necessary derivations (see figure 9).

- Widlar current mirror

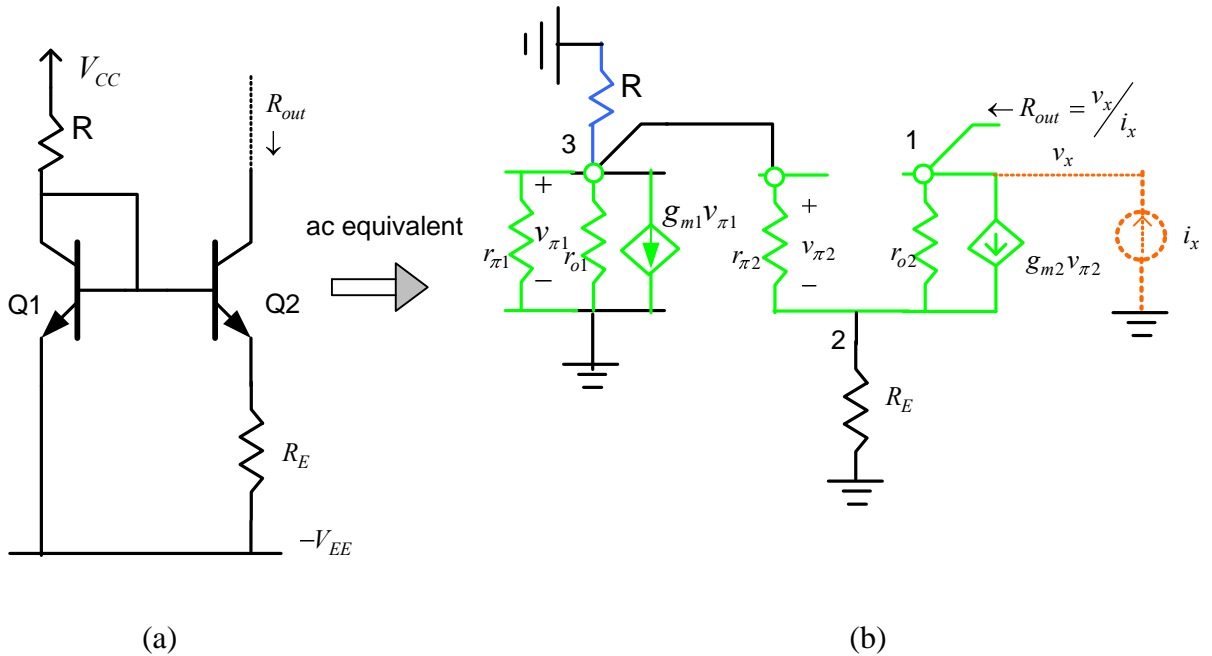


Figure 10: (a) schematic of the Widlar current mirror circuit, (b) ac equivalent circuit for R_{out} calculation.

Consider the ac equivalent circuit in Fig.10(b). By inspection we can derive the following

- (i) The passive admittance matrix PAM (using g_x for $1/r_x$, x being a general element) is:

$$\begin{array}{l}
 \text{Node\#1} \\
 \text{Node\#2} \\
 \text{Node\#3}
 \end{array}
 \begin{bmatrix}
 \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \\
 g_{o2} & -g_{o2} & 0 \\
 -g_{o2} & g_{o2} + g_E + g_{\pi 2} & -g_{\pi 2} \\
 0 & -g_{\pi 2} & g_R + g_{\pi 1} + g_{o1} + g_{\pi 2}
 \end{bmatrix}$$

- (ii) The node voltage vector is : $[V_1 \quad V_2 \quad V_3]^T$

- (iii) The current source vector is:

$$\begin{array}{l}
 \text{Node\#1} \\
 \text{Node\#2} \\
 \text{Node\#3}
 \end{array}
 \begin{bmatrix}
 i_x - g_{m2}v_{\pi 2} \\
 g_{m2}v_{\pi 2} \\
 -g_{m1}v_{\pi 1}
 \end{bmatrix}$$

- (iv) The dependant current source $g_{m2}v_{\pi 2}$ can be expanded as $g_{m2}(V_3 - V_2)$. Similarly, $g_{m1}v_{\pi 1} = g_{m1}V_3$. Substituting in the current source vector expression, we can re-write step (iii) as:

$$\begin{array}{l} \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \left[\begin{array}{c} i_x - g_{m2}V_3 + g_{m2}V_2 \\ g_{m2}V_3 - g_{m2}V_2 \\ -g_{m1}V_3 \end{array} \right]$$

(v) Combining (i), (ii) and (iv) in the general nodal admittance matrix (NAM) equation form $\mathbf{Y} \mathbf{V} = \mathbf{I}$, we can derive:

$$\begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \\ \left[\begin{array}{ccc} g_{o2} & -g_{o2} & 0 \\ -g_{o2} & g_{o2} + g_E + g_{\pi 2} & -g_{\pi 2} \\ 0 & -g_{\pi 2} & g_R + g_{\pi 1} + g_{o1} + g_{\pi 2} \end{array} \right] & \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} & = \begin{bmatrix} i_x - g_{m2}V_3 + g_{m2}V_2 \\ g_{m2}V_3 - g_{m2}V_2 \\ -g_{m1}V_3 \end{bmatrix} \end{array}$$

(vi) Transferring the voltages V_2, V_3 on the right hand side (RHS) to the left side, respectively in the columns of *Node#2* and *Node#3*, with a consequent change in sign we derive

$$\begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \\ \left[\begin{array}{ccc} g_{o2} & -g_{o2} & g_{m2} \\ -g_{o2} & g_{o2} + g_E + g_{\pi 2} + g_{m2} & -g_{\pi 2} - g_{m2} \\ 0 & -g_{\pi 2} & g_R + g_{\pi 1} + g_{o1} + g_{\pi 2} + g_{m1} \end{array} \right] & \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} & = \begin{bmatrix} i_x \\ 0 \\ 0 \end{bmatrix} \end{array}$$

(vii) The solution $v_x = V_1 = f(g_x) i_x$, produces the expression of $R_{out} = f(g_x)$. Specifically, using Krammer's rule we can evaluate (*use of MAPLE can be helpful*)

$$R_{out} = \frac{g_{o2}(g_R + g_{\pi 1} + g_{o1} + g_{\pi 2} + g_{m1}) + g_E(g_R + g_{\pi 1} + g_{o1} + g_{\pi 2} + g_{m1}) + g_{\pi 2}(g_R + g_{\pi 1} + g_{o1} + g_{m1}) + g_{m2}(g_R + g_{\pi 1} + g_{o1} + g_{m1})}{g_{o2}(g_E g_{\pi 1} + g_E g_{\pi 2} + g_{\pi 2} g_{o1} + g_{\pi 2} g_R + g_E g_R + g_E g_{m1} + g_{\pi 2} g_{m1} + g_{\pi 2} g_{\pi 1} + g_E g_{o1})}$$

- *Numerical evaluation:*

If we assume that the two BJTs are identical with $V_A = 50$ volts, $I_C = I_{REF} = 1$ mA, $\beta = 99$, $R_E = 1$ k Ω , $R = 3$ k Ω , we can determine all the parameters¹ in the expression for R_{out} , and finally get $R_{out} = \mathbf{1.465$ M Ω (approximately). This is a large value. This is the result of inserting R_E at the emitter of Q2.

To gather an idea of R_{out} without the emitter resistance R_E , we can set $R_E = 0$, i.e., $g_E = \infty$. We can evaluate

¹ The assumption made here is that the *ac* parameters of the two transistors are identical. In practice it is not true. With R_E at the emitter of Q₂, the DC current in Q₂ will be different from that of Q₁, and hence the *ac* parameters will be different.

is not effective. In this case the resistance is approximately $1/g_m$ (the student is suggested to prove it). The collector/drain terminal in this case has to be grounded for ac signals. This situation does not arise for a *diode connected* transistor (i.e., case 2.2.1A).

2.2.2: Use of active loads in single stage amplifiers

2.2.2 A: CE/CS amplifier

The schematics for a CE/CS amplifier with an active loads are shown in Figures 17(a), (b) with current mirror active loads and in Figures 17(c), (d) with current source active loads.

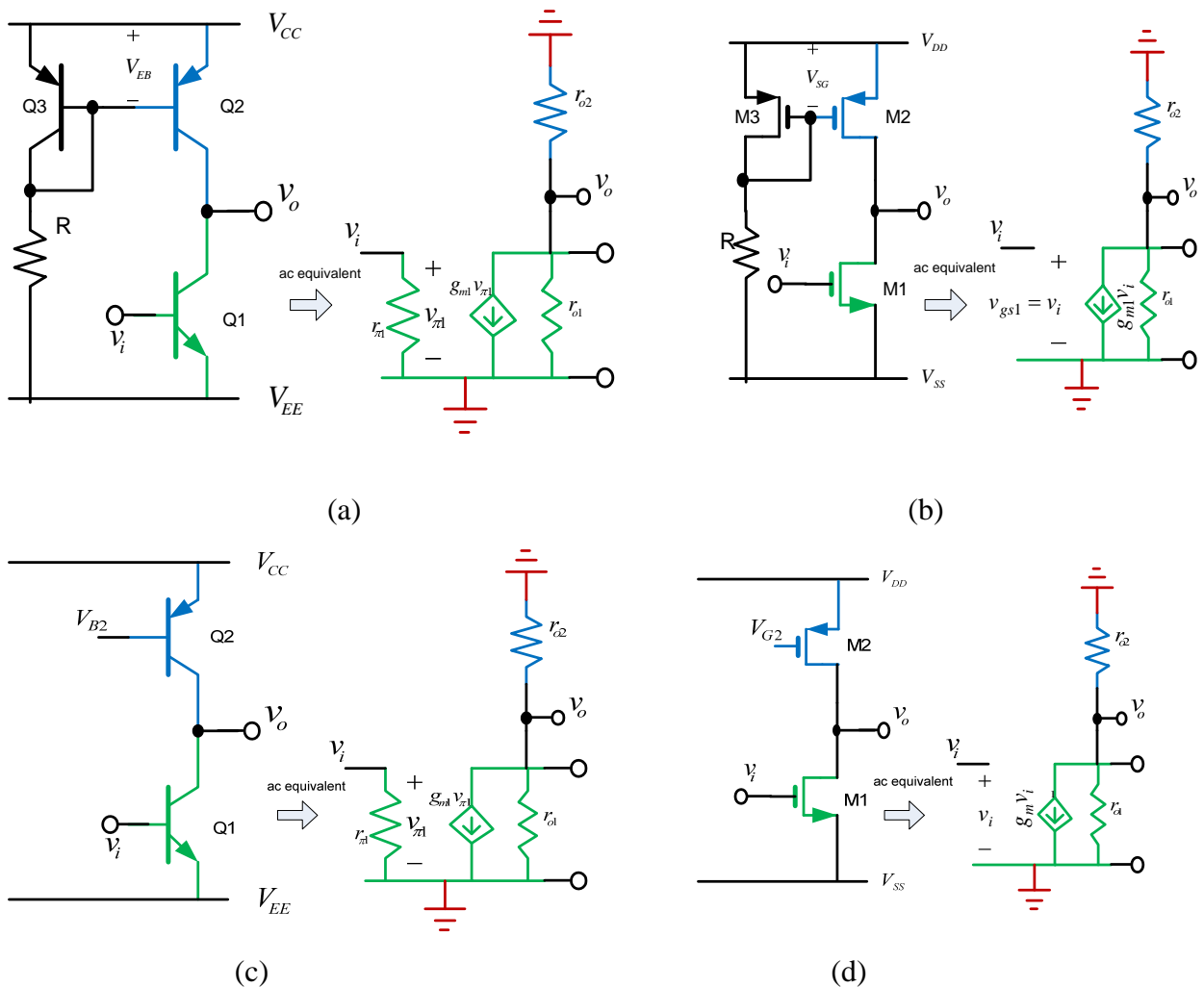


Figure 17: (a) CE BJT amplifier, and (b) CS MOS amplifier, with *current mirror* active load; (c) CE BJT amplifier, and (d) CS MOS amplifier, with *current source* active load

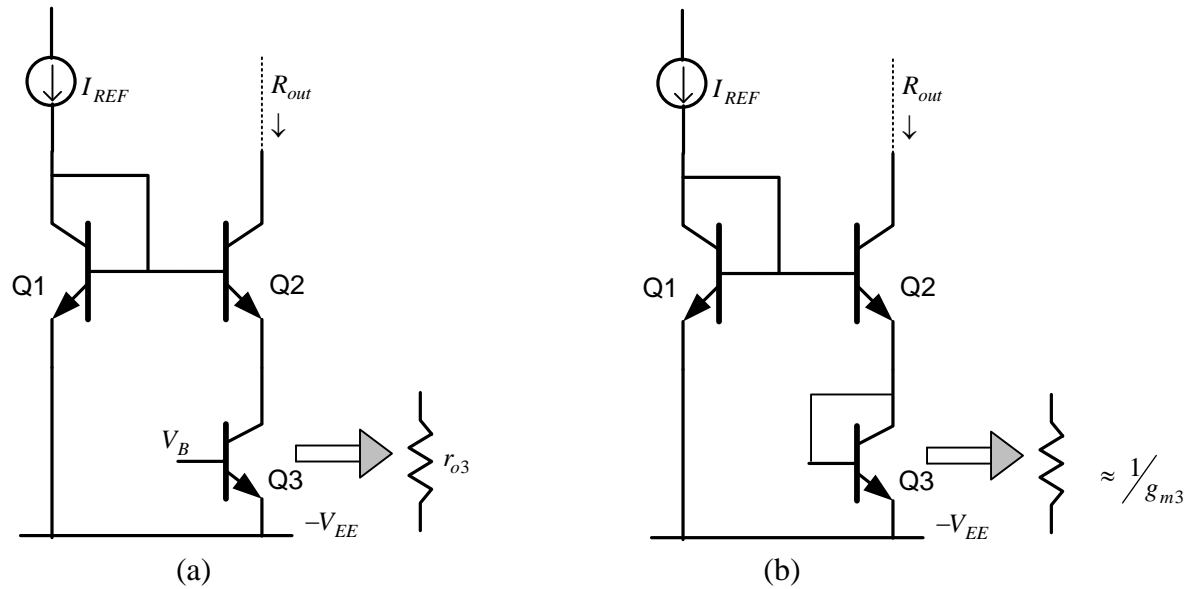


Figure 19: (a) Mirror of Fig.10(a) with R_E replaced by fixed V_{BE} across Q_3 , (b) R_E replaced by diode connected Q_3

In practical integrated circuit implementation of the current mirror, we need to replace the I_{REF} by actual circuit elements providing a bias current. This has already been shown in Fig.9, for example.

Finally, use of too many (more than two) independent DC voltage sources is not practical in an actual integrated circuit substrate floor. Hence the arrangement around Q_3 in Fig.19(a) needs a change to reflect Q_3 as providing an *ac* output resistance of r_o . This can be achieved by including Q_3 as part of a current mirror as shown in Fig. 20(a), for example.

2.2.3 B: Cascode current mirror

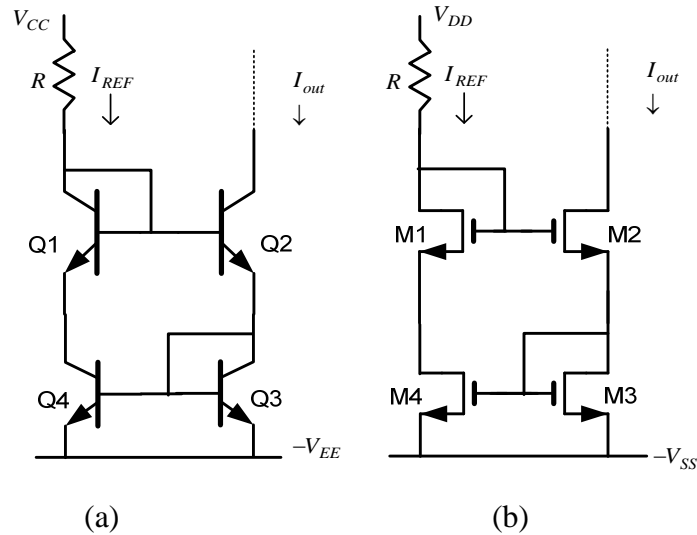


Figure 21: (a) Wilson current mirror with BJT devices, (b) Wilson current mirror with MOS devices.

2.3: Differential amplifiers:

- Differential amplifiers with discrete resistance circuits.
- Differential amplifiers with active loads.

A differential amplifier amplifies difference of two signals. So this amplifier shall have two input nodes. The output can have one or two nodes. In the first case (one output node), the system is simply referred to as a differential-in single-out amplifier. In the second case (output having two nodes), the system will be called as differential-in, differential- out amplifier. Typical schematics of a differential amplifier using BJT and MOS devices are shown in figure 22, and figure 23. It can be seen that the emitter terminals of the input devices in a BJT differential amplifier are connected together and a DC current source provides the bias current through this tail-end. For a MOS amplifier, the source terminals of the input devices are connected together. In a discrete component version of the system, the loads are resistances. In an integrated circuit version, the loads will be replaced by active loads.

When the transistors are matched (i.e., identical and of same semiconductor process technology), the output of the differential amplifier will be zero when the two input signal are equal. Thus, a differential amplifier provides good rejection (i.e., produces zero output) for common mode

Clearly, $v_{o1} = -g_m R_C v_I/2$, $v_{o2} = g_m R_C v_I/2$. Then the differential output voltage signal = $v_{o1} - v_{o2} = -g_m R_C v_I$. The voltage gain is then $-g_m R_C$.

2.3.1.3 E: Common mode voltage gain

Now we shall consider $v_I = v_2 = v_{CM}$. Then $v_3 = v_{CM}$ (see eq. 2.3.1.10). In this case, we shall have $v_{o1} = v_{o2} = 0$. Accordingly, the differential output voltage is zero! Since we are considering identical matched transistors calculating a differential voltage gain with *zero* differential input signal voltage becomes meaningless.

We therefore calculate the single-ended voltage gain, i.e., v_{o1}/v_{CM} . We now divide the amplifier into two halves (half circuits) as shown in Fig.26. Each half is like a CE amplifier with un-bypassed resistance in the emitter. The derivation follows. Consider only one half-circuit. KCL at the node of v_x gives

$$-\frac{v_{CM} - v_x}{r_\pi} - g_m(v_{CM} - v_x) + \frac{v_x}{2R_I} = 0 \quad (2.3.1.12)$$

Solving for v_x , we get
$$v_x = \frac{2v_{CM}(g_m r_\pi + 1)R_I}{r_\pi + 2R_I(g_m r_\pi + 1)} \quad (2.3.1.13)$$

The output signal voltage $v_{o1} = -g_m R_C (v_{CM} - v_x) = -\frac{g_m r_\pi R_C v_{CM}}{r_\pi + 2R_I(g_m r_\pi + 1)} \quad (2.3.1.14)$

Remembering that $g_m r_\pi = \beta$, $r_\pi = (\beta + 1)r_e$, $(\beta + 1)/\beta = 1/\alpha$, we can finally get the common mode gain $G_{CM} = v_{o1}/v_{CM} = -\frac{\alpha R_C}{r_e + 2R_I} \approx -\frac{\alpha R_C}{2R_I}$. This is approximately same as the voltage gain of a CE BJT amplifier with an un-bypassed emitter resistance of r_e (internal to the transistor) in series with $2R$ (external to the transistor).

The MOS or CMOS technology is primarily used now- a- days for integrated circuits and systems. So we can work with a MOST-based DA for signal related analysis or calculations.

For a current mirror based DA, consider figures 29(a) and (b) for the schematic and the associated small signal equivalent circuit respectively. The amplifying devices are NMOS while the active loads are comprised of PMOS transistors.

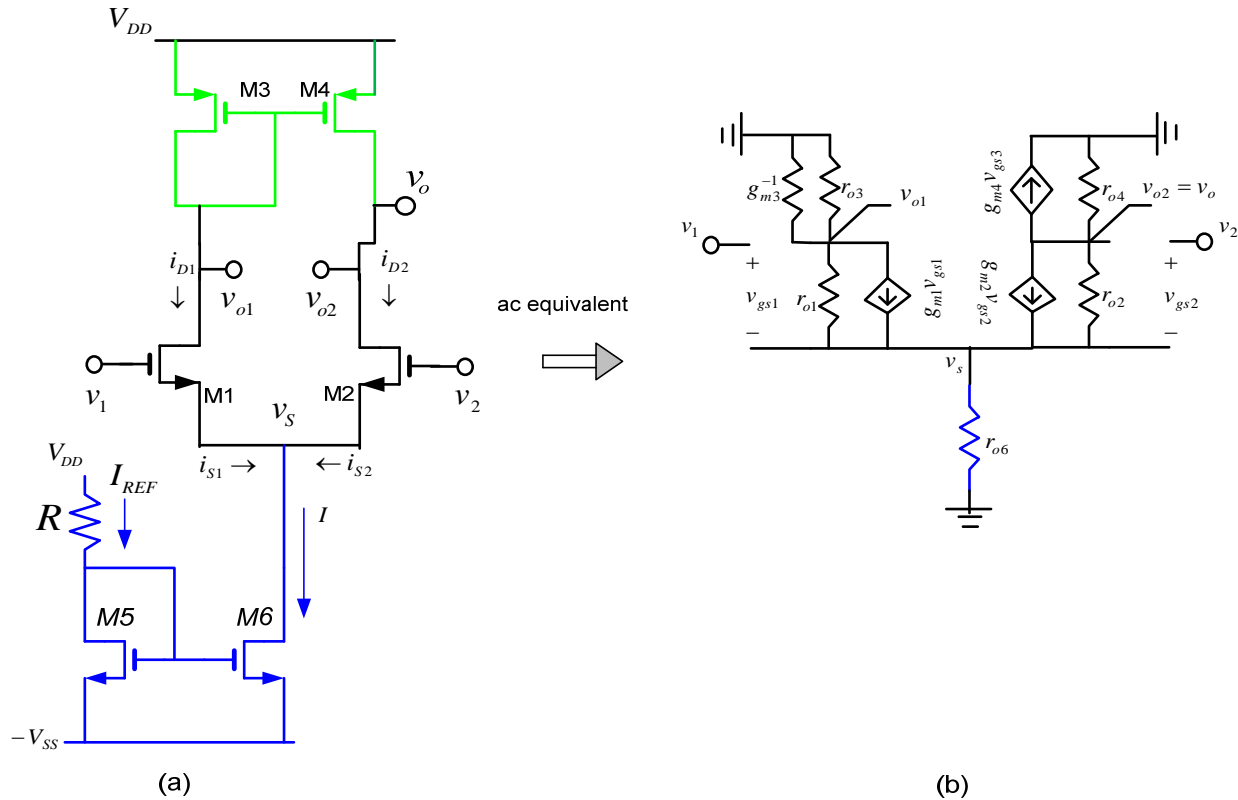


Figure 29: (a) A CMOS DA with current mirror load and current mirror bias current source, (b) ac equivalent circuit at low frequency (i.e., ignoring any parasitic capacitances). Body effect in M1 and M2 has been ignored

Analysis: To begin an approximate analysis, we will introduce several simplifying assumptions. Thus the NMOS transistors M1,M2 are considered matched pair of transistors. So $g_{m1}=g_{m2}=g_{mn}$, $r_{o1}=r_{o2}=r_{dn}$. Similarly, the PMOS pair M3,M4 are considered matched. So $g_{m3}=g_{m4}=g_{mp}$, and $r_{o3}=r_{o4}=r_{dp}$. Let us introduce the conductance parameter $g_{xy}=1/r_{xy}$. We will then carry out the analysis for *balanced* differential input signals, i.e., $v_1=v_d/2$, $v_2=-v_d/2$. Consequently, $v_s=0$, $v_{gs1}=v_d/2$, $v_{gs2}=-v_d/2$. Further the circuit configuration of the current mirror dictates $v_{gs3}=v_{o1}$