CHAPTER 2

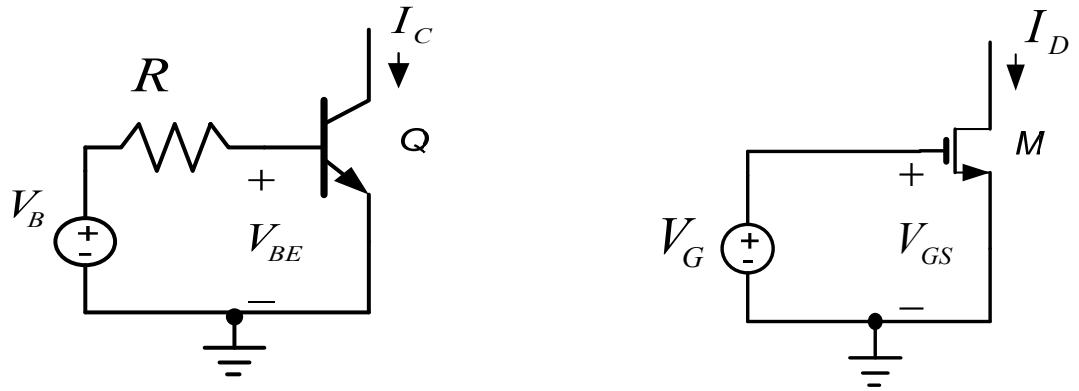
In this chapter we shall present additional (over those in Electronics-I course) electronic circuits that are used as subsystems in a larger electronic system, especially in connection with integrated circuit technology. In particular the following will be covered.

- Current source, current mirror and active loads
- Differential amplifiers (discrete as well as integrated circuit)
- Example of a multi-stage amplifier (such as an Operational Amplifier)

2.1 Current source, current mirror and current steering:

2.1.1: BJT and MOS current sources

Consider figures 1(a)-(b) which depict the basic configuration of a BJT, and an MOS current source, respectively.



(a) (b)

Figure 1: (a) basic BJT current mirror, (b) basic MOS current mirror

The output terminal (collector/drain) of the device delivers a constant DC current to the load (not shown explicitly) as long as the voltage V_{BE} (for BJT) and V_{GS} (for MOS) remains constant and the temperature remains fixed (say, 27 deg. C). The value of this DC current is given by:

(for BJT) $I_C \approx I_S \exp(V_{BE}/V_T)$

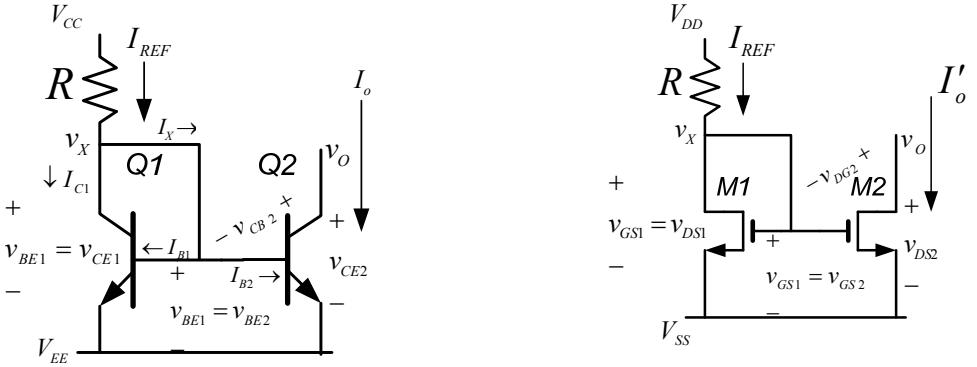
(for MOS) $I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_{TH})^2$

Note that the devices are assumed to operate in the active (for BJT) and saturation (for MOS) regions. In these regions, the I-V characteristics of the devices are almost parallel to the V-axis (i.e., $\Delta I/\Delta V = 0$). The output terminal is supposed to appear like an infinite resistance (internal resistance of an ideal current source) to the load system (not shown). But in reality this is never satisfied.

When the active device (i.e., transistor) is located nearer to the most positive DC supply line, the terms 'current source' is used. When the active device is nearer to the most negative (or ground) DC supply line, the name 'current sink' is used for the current source.

2.1.2: Basic BJT and MOS current mirrors

In an integrated circuit environment we need to provide DC bias currents to various subsystems located on the same wafer. It is not very economic to build an independent current source near the location of each of these subsystems. Instead, one reference current source is built and then current mirrors are used to generate several other DC currents which can feed the different subsystems. The basic configurations of a current mirror using BJT and MOS transistors are shown in figures 2(a)-(b).



(a) (b)

Figure 2: (a) BJT current mirror, (b) MOS current mirror

The operation of a current mirror can be easily understood as follows:

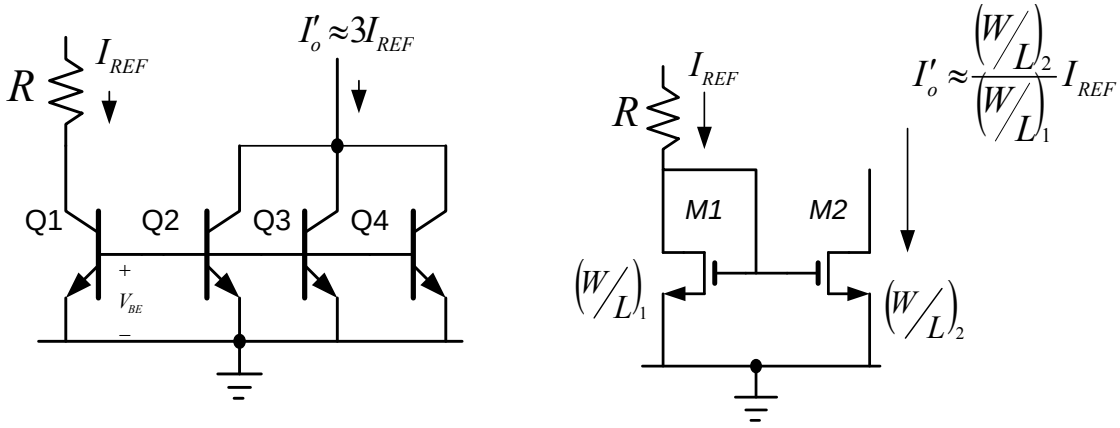
In case of the BJT: $I_o = I_{s2}\exp(V_{BE}/V_T)$; $I_{REF} \approx I_{C1} = I_{s1}\exp(V_{BE}/V_T)$

If the transistors are identical, we can put $I_{s1} = I_{s2}$. Then $I_o = I_{REF}$.

In case of the MOS: $I_o = \frac{\mu C_{ox}}{2}(\frac{W}{L})_2(V_{GS} - V_{TH})^2$; $I_{REF} = \frac{\mu C_{ox}}{2}(\frac{W}{L})_1(V_{GS} - V_{TH})^2$. So $I_o = I_{REF}\frac{(W/L)_2}{(W/L)_1}$.

If $(W/L)_2 = (W/L)_1; I_o = I_{REF}$.

Obviously, the key factor that makes the mirroring operation possible is maintenance of same V_{BE} (for BJT) and same V_{GS} (for MOS) for the pair (reference generator, and the mirror) of devices concerned. DC currents of different levels can be easily generated by adopting the following arrangements (Figures 3(a)-(b)).



(a) (b)

Figure 3: (a) BJT based current mirror with a gain of three (all BJTs identical), (b) MOS based current mirror with a gain equal to the aspect ratios (i.e., W/L values) of M1 and M2, the two NMOS are assumed to belong to same technology.

2.1.3: <u>DC bias design in case of current source/mirror</u>

To set up the reference current one has to employ a fixed DC power supply and a fixed resistance. Once this is done, the operation follows the equations already mentioned above. Let us consider two examples.

Example 2.1.3.1 :(BJT device):

$I_{ref} = \frac{V_{CC} - V_B}{R}$; $I_C = I_S e^{(V_B - V_{EE})/V_T}$, assuming n=1

KCL $I_{ref} - \frac{I_C}{\beta_1} - \frac{I_o}{\beta_2} = I_C$; $I_x = \frac{I_C}{\beta_1} + \frac{I_o}{\beta_2}$. Further,

$I_o = I_S e^{(V_B - V_{EE})/V_T}$. If I_o is given, I_S is known, and V_{EE} is given, we can find V_B. Using the KCL equations above and assuming $\beta_1 = \beta_2 = \beta$, we can write

$\frac{V_{CC} - V_B}{R} - I_C(1 + \frac{1}{\beta}) - \frac{I_o}{\beta} = 0$. Now, if V_{CC} and β are known, We can solve the above equation for R.

Finding R completes the DC design.

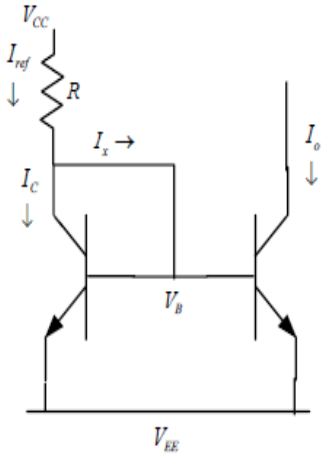


Figure 4 : Related to *Ex 2.1.3.1*

Consider $\beta_1=\beta_2=49$; I_o=3 mA ; I_S =10^{-14} A ; $-V_{EE}=V_{CC}$=5 V. Design the current source, assuming that both the BJT devices are identical.

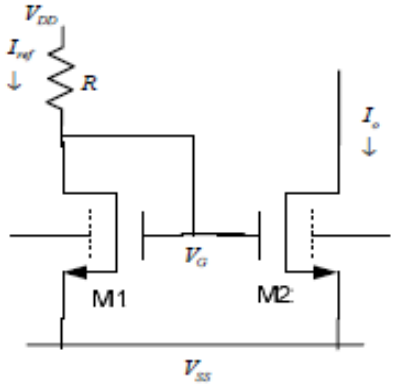
Designing the current source is to design the value of R.

Using $I_o = I_S e^{(V_B - V_{EE})/V_T}$, we can find V_B =-4.34V. Then from $I_C = I_S e^{(V_B - V_{EE})/V_T}$, we can derive I_C =2.92 mA. (The accuracy may be affected by the calculator capability).

Then inserting the known values in $\frac{V_{CC} - V_B}{R} - I_C(1 + \frac{1}{\beta}) - \frac{I_o}{\beta} = 0$, we get

$\frac{5 + 4.34}{R} - 2.92 \times 10^{-3}(1 + 1/49) - 3 \times 10^{-3}/49 = 0$, gives R=3.071 kΩ. (This becomes 2.99 kilo ohms if $I_o=I_C$ = 3 mA is taken).

Example 2.1.3.2 (MOS device):



$I_{ref} = \mu C_{ox}(\frac{W}{2L})_1(V_{GS} - V_{TH})^2$, will give V_{GS} for M1, and with V_{SS} known, we can determine V_G. Thus $V_G = V_{GS} + V_{SS}$. Then $R = \frac{V_{DD} - V_G}{I_{ref}}$. This completes the design of R

Figure 5 : Related to *Ex 2.1.3.2*

If $(W/L)_2$ is A times that of $(W/L)_1$, and the two MOS transistors belong to the same technology, i.e., μ, C_{ox}, V_{TH} are identical for both, we can write $I_o = \mu C_{ox}(W/2L)_2(V_{GS} - V_{TH})^2 = AI_{ref}$. Suppose μC_{ox} =100 μA/volt^2, $(W/L)_1$=5, $(W/L)_2$=10, V_{TH} =0.7 volts, can you design the current source (i.e., find R), for I_o=10 μA. Given V_{DD} =-V_{SS} =5 volts ?

Solution : From the given information, you find $A = \frac{(W/2L)_2}{(W/2L)_1}$ =10/5=2. Then I_{ref} =I_o/A=5 μA.

Substituting in the square law equation for M1, $5\times10^{-6} = 100\times10^{-6}\times5\times(V_{GS}-0.7)^2$, you can calculate V_{GS} =0.6 or 0.8 volts.

For the MOS to conduct, V_{GS} must be > V_{TH} =0.7 volts (given). So you accept V_{GS} =0.8 volts. Since V_{SS} =-5 volts, V_G -V_{SS}= 0.8, leads to V_G= -4.2 volts.

Now using the calculated values of I_{ref}, V_G, and the given value of V_{DD}, you can find R=1.84 Mega Ω.

2.1.4 Current steering : In the above we have cited only one kind of transistors, i.e., NPN (and NMOS) to illustrate the operation of current mirrors. In real systems, currents need be delivered to both kinds of devices. One can then start with a basic mirror made from, say, NMOS stages and steer the path of the current through PMOS stages. Steering implies continuation of the current mirroring operation through both P- and N-type devices in a large electronic system. An example is given in figure 6.

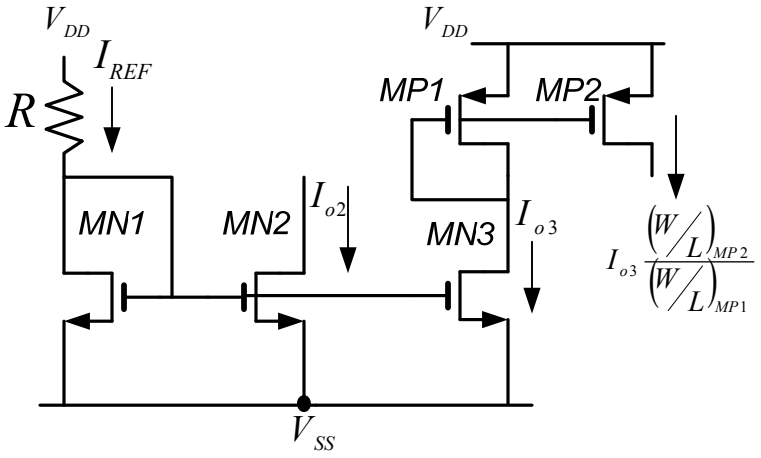


Figure 6: Current steering from a NMOS stage to a PMOS stage.

2.1.5 Non-ideal effects:

2.1.5 A: : *Base-width/Channel modulation effect:* We already have learnt that the current at the output of a BJT/MOS device increases slowly with V_{CE} / V_{DS}, due to the base-width/channel modulation effect. In base-width modulation (for BJT), the increase of current is due to *more number* of charge carriers arriving at the collector. In channel modulation (for MOS), the reason is *faster* collection of the charges by virtue of the electric field at the drain-gate transition. Because of these, the output resistance of a current mirror, for small signal case, is never very large (not to think of infinite value!). For BJT the output resistance is of the order of 20-50 kilo ohms, while in MOS, it could be 100-1000 kilo ohms, in a basic current mirror.

The above effect(s) can be easily taken care of by suitably modifying the equation(s) pertaining to current mirroring operation.

2.1.5 B: *Effect of channel modulation in a MOS current mirror*

Since the variation of I_{DS} with V_{DS} in the saturation region of operation is a consequence of the channel length modulation, we need to consider the I-V equation (for an NMOS):

$I = \mu C_{ox}(W/2L)(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) = I_o(1+\lambda V_{DS})$, where $I_o = \mu C_{ox}(W/2L)(V_{GS}-V_{TH})^2$.

From the geometrical drawing of figure 7, we can deduce the following:

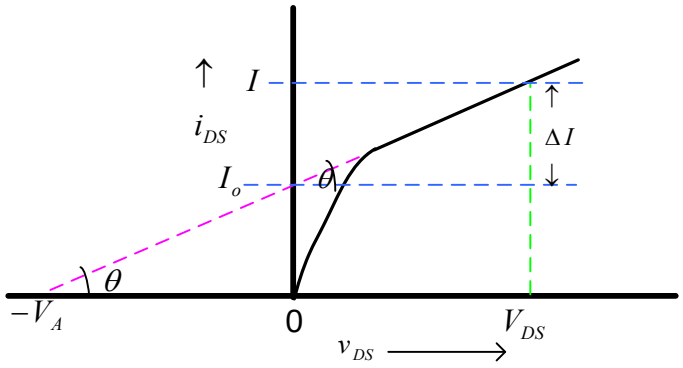


Figure 7: Calculations for the channel modulation effect (*Early* effect) in an NMOS device.

$\frac{\Delta I}{V_{DS}} = \tan\theta = \frac{I_o}{|V_A|}$, so $\Delta I = \frac{I_o}{|V_A|}V_{DS}$. Then $I = I_o + \Delta I = I_o + I_o\lambda V_{DS}$, so $\lambda = \frac{1}{|V_A|}$

The V_{DS} in the reference MOS and the mirroring MOS will be different because of different loading condition, in general $I_{REF} = I_{MIRROR}$ will not hold (for two identical matched MOS transistors). The result of differing V_{DS} bears upon the associated V_{DG} as well. For the reference generator (drain-gate connected) $V_{DG}=0$. For the mirror transistor $V_{DG}=V_{DS} - V_{GS}$ which is $\neq 0$, since the gate is not connected to the drain. When the reference and the mirror transistors have different V_{DS} values the current transfer ratio will be given by

$$\frac{I_{MIRROR}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})}$$

Tracking error: This is the difference between the ideal output bias current (i.e., ignoring the channel modulation efect) and the actual output bias current (including the channel modulation effect).

Note the following work, which includes the effect of V_{DS} in both the reference generator transistor and the mirroring transistor. Consider figure 8.

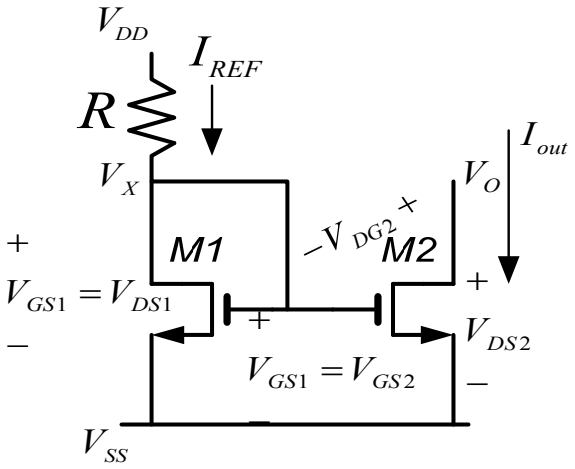


Figure 8: Illustrating the effect of unequal V_{DS} in the reference and the mirroring MOS transistors

$I_{REF} = I_o(1+\lambda V_{DS1}) = I_o(1+\lambda V_{GS1})$, since $V_{DS1} = V_{GS1}$ because of gate-drain connection.

$I_{MIRROR} = I_{out} = I_o(1+\lambda V_{DS2})$, where $V_{DS2} = V_{DG2} + V_{GS2} = V_{DG2} + V_{GS1}$. Then I_{REF} - I_{MIRROR} $= -I_o\lambda V_{DG2}$.

Thus, $I_{MIRROR} = I_{REF} + I_o\frac{1}{V_A}V_{DG2} \approx I_{REF}(1+\frac{V_{DG2}}{V_A})$, **assuming** that $I_o \approx I_{REF}$.

Now, since $V_{DG2} = V_{DS2} - V_{GS2}$, and $V_{DS2} = V_o - V_{SS}$ (see the schematic), one can finally write

$I_{MIRROR} = I_{out} = I_{REF}(1 + \frac{V_O - V_{SS} - V_{GS2}}{V_A})$. The current tracking error is $I_{REF} - I_{out}$. Ideally this should be zero. (*quiz:* What will be the tracking error if $I_{REF} = I_{OUT}$ is not assumed?)

2.1.5 C: *Effect of finite β in case of a BJT mirror*

Because each BJT has a finite current gain β, a part of I_{REF} is diverted to the base of the reference generator transistor, making $I_C = I_{REF} - I_X$ (see Fig.9). The mirror transistor having same V_{BE} as the reference transistor will follow I_C of the reference transistor. Thus I_{OUT} of the mirror transistor differs from I_{REF}, introducing an error in tracking I_{REF}.

Tracking error: This is the difference between the ideal output bias current (i.e., assuming infinite β) and the actual output bias current (using finite β). Consider the following hints for the necessary derivations (see figure 9).

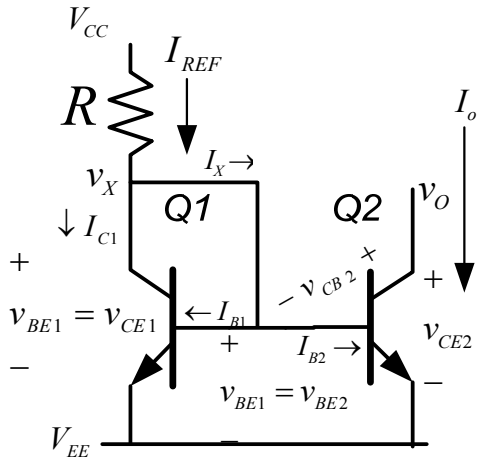


Figure 9: Illustrating the effect of finite β in a BJT current mirror

We need to find $I_{REF} - I_o$. Starting with I_{REF}, we have a KCL at the collector of *Q1*, i.e., at the node of V_X. Thus we get..

Then I_X is……

Writing $I_{B1} = I_{E1}/...$,

Assuming matched transistors, $\beta_1 = \beta_2 = \beta$, so $I_{E1} = I_{E2} = I_E$, you get $I_{REF} = \left(\frac{\beta}{\beta+1} + \frac{2}{\beta+1}\right) I_E$. But $I_o = ... = \frac{\beta}{\beta+1} I_E$. Then, replacing I_E in the expression of I_{REF} by the expression of I_o, you can get…

Now find the expression for $I_{REF} - I_o = \Delta I$….

Relative tracking error $\Delta I/I$…

% tracking error…

2.1.5 D: *Improved current mirrors:*

The principal defect of the basic current mirror is the finite output resistance (R_{out}) for ac signals. This arises out of the finite slope of the I_C vs. V_{CE} (for BJT) or I_D vs. V_{DS} (for MOS) characteristic of a single transistor. Certain circuit techniques have been invented to reduce this slope thereby increasing the value of R_{out} of the current mirror. The technique involves use of transistors stacked one on top of another and use of feedback principles. We shall examine the cases using network analysis principles. Increasing R_{out} makes the current mirror appear more closely like an ideal current source.

- Widlar current mirror

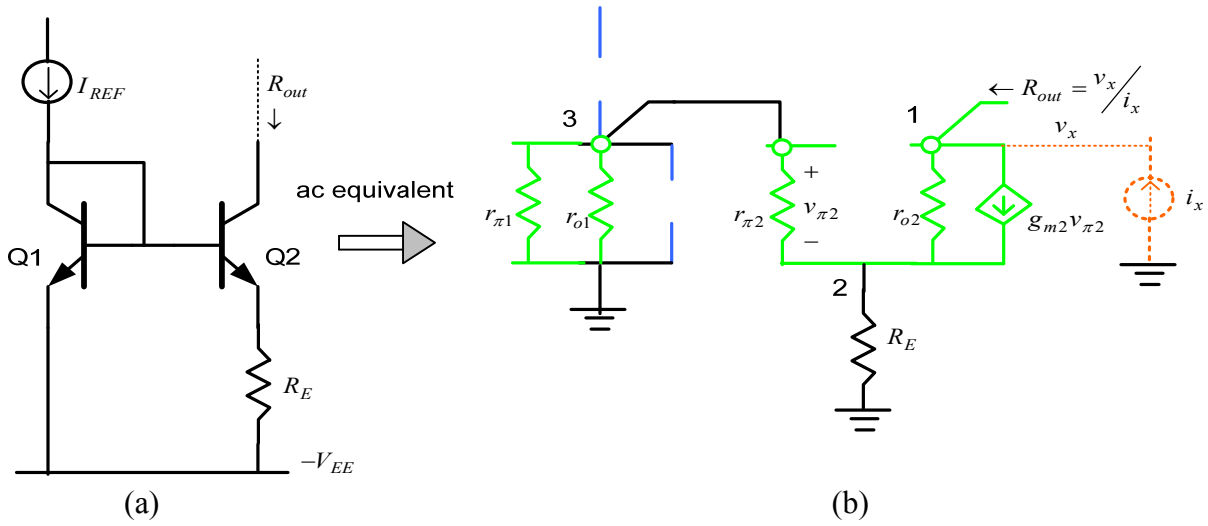


Figure 10: (a) schematic of the Widler current mirror circuit, (b) ac equivalent circuit for R_{out} calculation.

Consider the ac equivalent circuit in Fig.10(b). By inspection we can derive the following

(i) The passive admittance matrix PAM (using g_x for $1/r_x$, x being a general element) is:

$$\begin{array}{c} \\ \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \begin{array}{c} \begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \end{array} \\ \begin{bmatrix} g_{o2} & -g_{o2} & 0 \\ -g_{o2} & g_{o2}+g_E+g_{\pi 2} & -g_{\pi 2} \\ 0 & -g_{\pi 2} & g_{\pi 1}+g_{o1}+g_{\pi 2} \end{bmatrix} \end{array}$$

(ii) The node voltage vector is : $[\ V_1 \quad V_2 \quad V_3\ ]^T$

(iii) The current source vector is:

$$\begin{array}{c} \\ \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \begin{bmatrix} i_x - g_{m2}v_{\pi 2} \\ g_{m2}v_{\pi 2} \\ 0 \end{bmatrix}$$

(iv) The dependant current source $g_{m2}v_{\pi 2}$ can be expanded as $g_{m2}(V_3\text{-}V_2)$. Substituting in the current source vector expression, we can re-write step (iii) as:

$$\begin{array}{c} \\ \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \begin{bmatrix} i_x - g_{m2}V_3 + g_{m2}V_2 \\ g_{m2}V_3 - g_{m2}V_2 \\ 0 \end{bmatrix}$$

(v) Combining (i), (ii) and (iv) in the general nodal admittance matrix (NAM) equation form **Y V =I,** we can derive:

$$\begin{array}{c} \begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \end{array} \\ \begin{bmatrix} g_{o2} & -g_{o2} & 0 \\ -g_{o2} & g_{o2}+g_E+g_{\pi 2} & -g_{\pi 2} \\ 0 & -g_{\pi 2} & g_{\pi 1}+g_{o1}+g_{\pi 2} \end{bmatrix} \end{array} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} i_x - g_{m2}V_3 + g_{m2}V_2 \\ g_{m2}V_3 - g_{m2}V_2 \\ 0 \end{bmatrix}$$

(vi) Transferring the voltages V_2, V_3 on the right hand side (RHS) to the left side, respectively in the columns of *Node#2* and *Node#3*, with a consequent change in sign we derive

$$\begin{array}{c} \begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \end{array} \\ \begin{bmatrix} g_{o2} & -g_{o2}-g_{m2} & g_{m2} \\ -g_{o2} & g_{o2}+g_E+g_{\pi 2}+g_{m2} & -g_{\pi 2}-g_{m2} \\ 0 & -g_{\pi 2} & g_{\pi 1}+g_{o1}+g_{\pi 2} \end{bmatrix} \end{array} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} i_x \\ 0 \\ 0 \end{bmatrix}$$

(vii) The solution $v_x=V_1=\text{f}(g_x)i_x$, produces the expression of $R_{out}=\text{f}(g_x)$. Specifically, using Krammer's rule we can evaluate (*use of MAPLE* can be helpful)

$$R_{out} = \frac{g_{o2}g_{\pi 1} + g_{o2}g_{o1} + g_{o2}g_{\pi 2} + g_E g_{\pi 1} + g_E g_{o1} + g_E g_{\pi 2} + g_{\pi 1}g_{\pi 2} + g_{\pi 2}g_{o1} + g_{m2}g_{\pi 1} + g_{m2}g_{o1}}{g_{o2}g_E g_{\pi 1} + g_{o2}g_E g_{o1} + g_{o2}g_E g_{\pi 2} + g_{o2}g_{\pi 1}g_{\pi 2} + g_{o1}g_{o2}g_{\pi 2}}$$

- *Numerical evaluation*:

If we assume that the two BJTs are identical with V_A=50 volts, I_C=I_{REF} =1 mA, β=99, R_E=1 $k\Omega$, we can determine all the parameters in the expression for R_{out}, and finally get R_{out} =**901 *kΩ*** (approximately). This is a large value. This is the result of inserting R_E at the emitter of Q2.

To gather an idea of R_{out} without the emitter resistance R_E, we can set R_E =0, i.e., g_E =infinity. We can evaluate

$R_{out}\,|_{R_E=0} = \dfrac{g_{\pi 1} + g_{o1} + g_{\pi 2}}{g_{o2}g_{\pi 1} + g_{o1}g_{o2} + g_{o2}g_{\pi 2}}$ (lot simpler!)= 50 $k\Omega$ (i.e., simply r_{o2}). Thus inclusion of R_E at the emitter increases R_{out} by a factor of about 901/50 =18 times!

- *Demonstration by SPICE (Circuit Simulation)*

  Case I: R_E is very small (1 milli ohms), i.e., it is like an ordinary current mirror with emitter of Q2 (almost) shorted to ac ground.

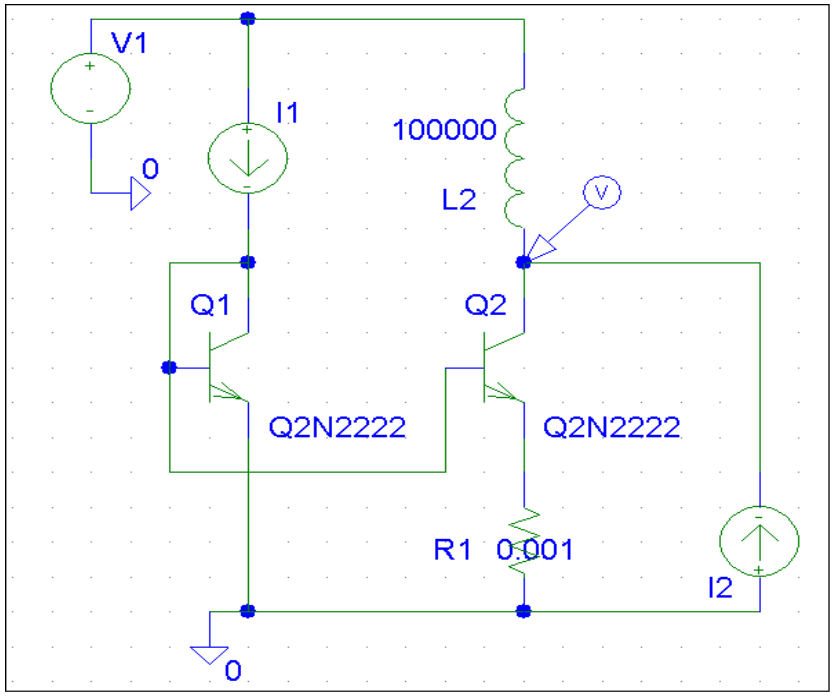


Figure 11:

The ouput list shows DC and ac equivalent circuit parameters for Q1 and Q2

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2
MODEL	Q2N2222	Q2N2222
IB	6.69E-06	6.69E-06
IC	9.87E-04	1.11E-03
VBE	6.46E-01	6.46E-01
VBC	0.00E+00	-9.35E+00
VCE	6.46E-01	1.00E+01
BETADC	1.48E+02	1.66E+02
GM	3.80E-02	4.28E-02
RPI	4.29E+03	4.29E+03
RX	1.00E+01	1.00E+01
RO	7.50E+04	7.50E+04
CBE	5.20E-11	5.40E-11
CBC	7.31E-12	3.01E-12
CJS	0.00E+00	0.00E+00
BETAAC	1.63E+02	1.84E+02
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	1.02E+08	1.20E+08

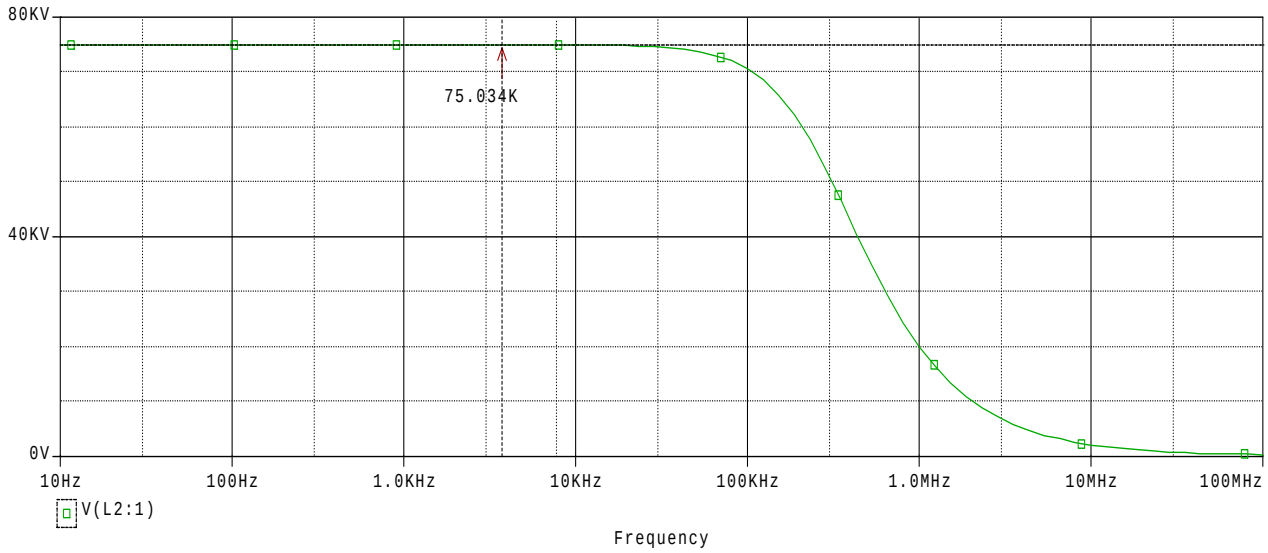


Figure 12:

R_{out} is about 75 kilo ohms which is equal to r_o of Q2 (check from the list, shown in GREEN shade)

Case II: R_E is increased to 1000 ohms (i.e.,it is like the normal Widlar current mirror). The schematic changes.

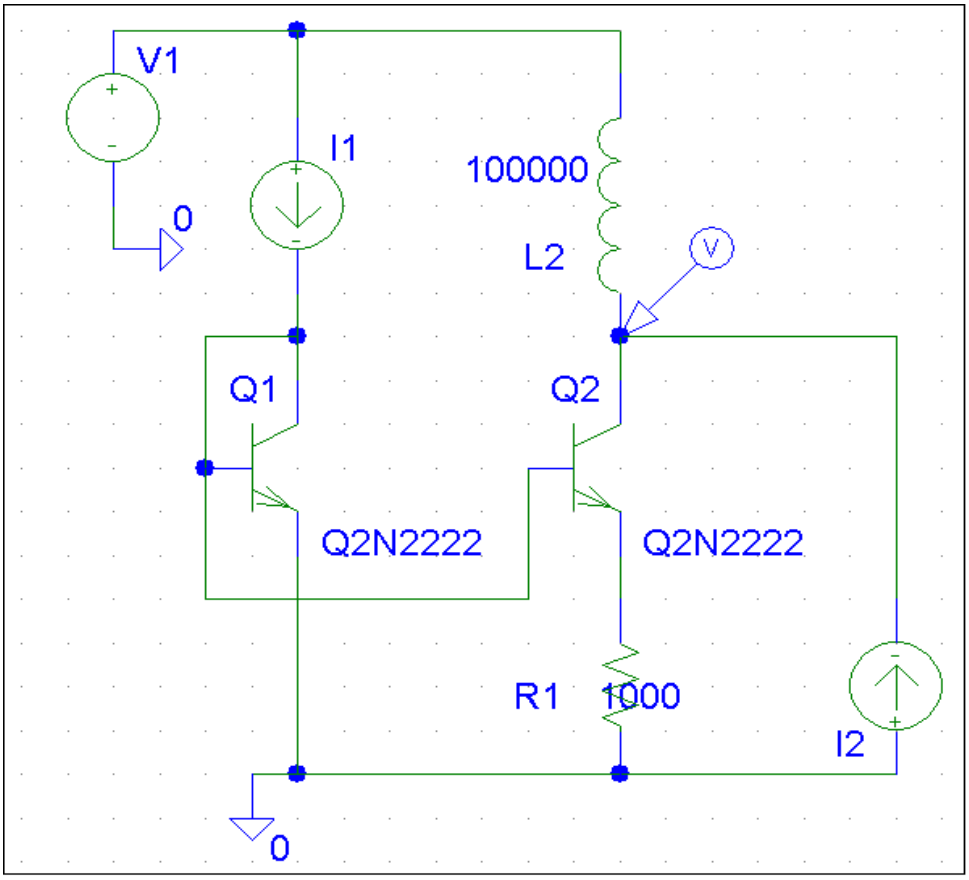


Figure 13:

The DC and ac equivalent circuit parameters now become different in case of Q2. Check the output list below.

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2
MODEL	Q2N2222	Q2N2222
IB	6.72E-06	5.88E-07
IC	9.93E-04	7.09E-05
VBE	6.46E-01	5.74E-01
VBC	0.00E+00	-9.35E+00
VCE	6.46E-01	9.93E+00
BETADC	1.48E+02	1.21E+02
GM	3.82E-02	2.74E-03
RPI	4.27E+03	5.09E+04
RX	1.00E+01	1.00E+01
RO	7.46E+04	1.18E+06

CBE	5.21E-11	3.54E-11
CBC	7.31E-12	3.01E-12
CJS	0.00E+00	0.00E+00
BETAAC	1.63E+02	1.40E+02
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	1.02E+08	1.13E+07

On inserting the relevant values in the expression

$$R_{out} = \frac{g_{o2}g_{\pi1} + g_{o2}g_{o1} + g_{o2}g_{\pi2} + g_E g_{\pi1} + g_E g_{o1} + g_E g_{\pi2} + g_{\pi1}g_{\pi2} + g_{\pi2}g_{o1} + g_{m2}g_{\pi1} + g_{m2}g_{o1}}{g_{o2}g_E g_{\pi1} + g_{o2}g_E g_{o1} + g_{o2}g_E g_{\pi2} + g_{o2}g_{\pi1}g_{\pi2} + g_{o1}g_{o2}g_{\pi2}}$$, we

can find (use MAPLE program if required) R_{out} =4.112 Meg ohms

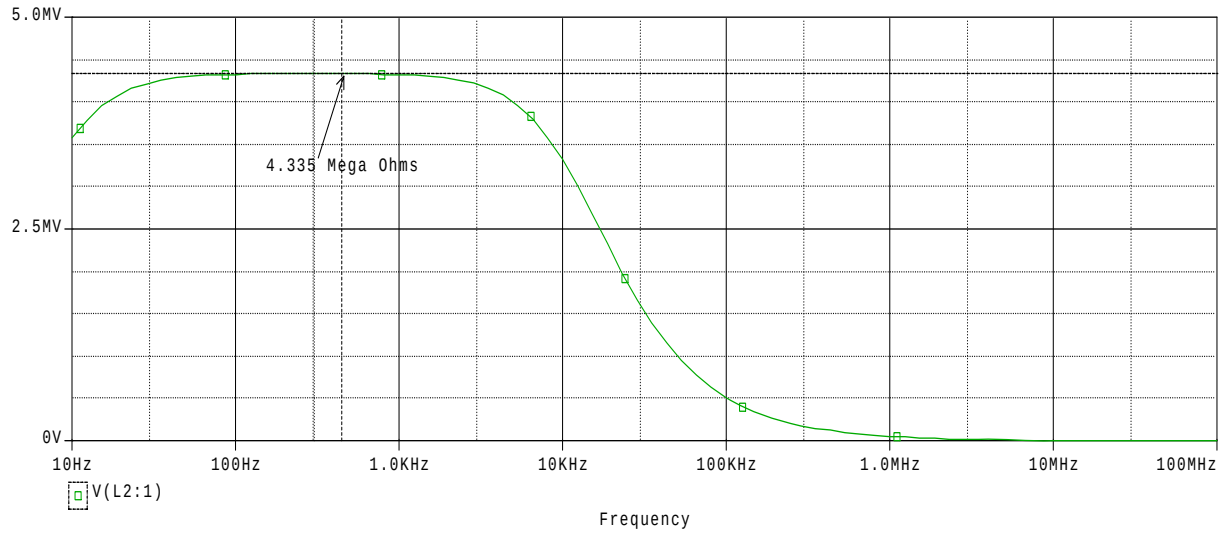


Figure 14:

The simulated value of R_{out} is 4.335 Mega ohms. The increase is by a factor of 4335/75=57.8 times!

Comment : Between the values obtained by the theoretical formula and circuit simulation, we will accept the circuit simulation value as more realistic.

2.2 Active loads and uses:

An active load implies a resistance made from a transistor (active device). The resistance is primarily effective for small signal application. Sometimes transistors are also used like potentiometric resistances to deliver different levels of DC voltages, in an integrated circuits

environment. To understand the operation of a transistor as an active load (resistance), we need to consider the ac equivalent circuit of the transistor.

2.2.1*:* AC equivalent circuits for active loads

2.2.1 A*: Diode connected transistor:* This is easily obtained by connecting the gate and drain of a MOS (base and collector of a BJT). The resulting ac resistance is approximately $1/g_m$, where g_m is the transconductance of the device (obtained by proper DC biasing). Consider the analysis below (see Fig. 15(a)-(c)).

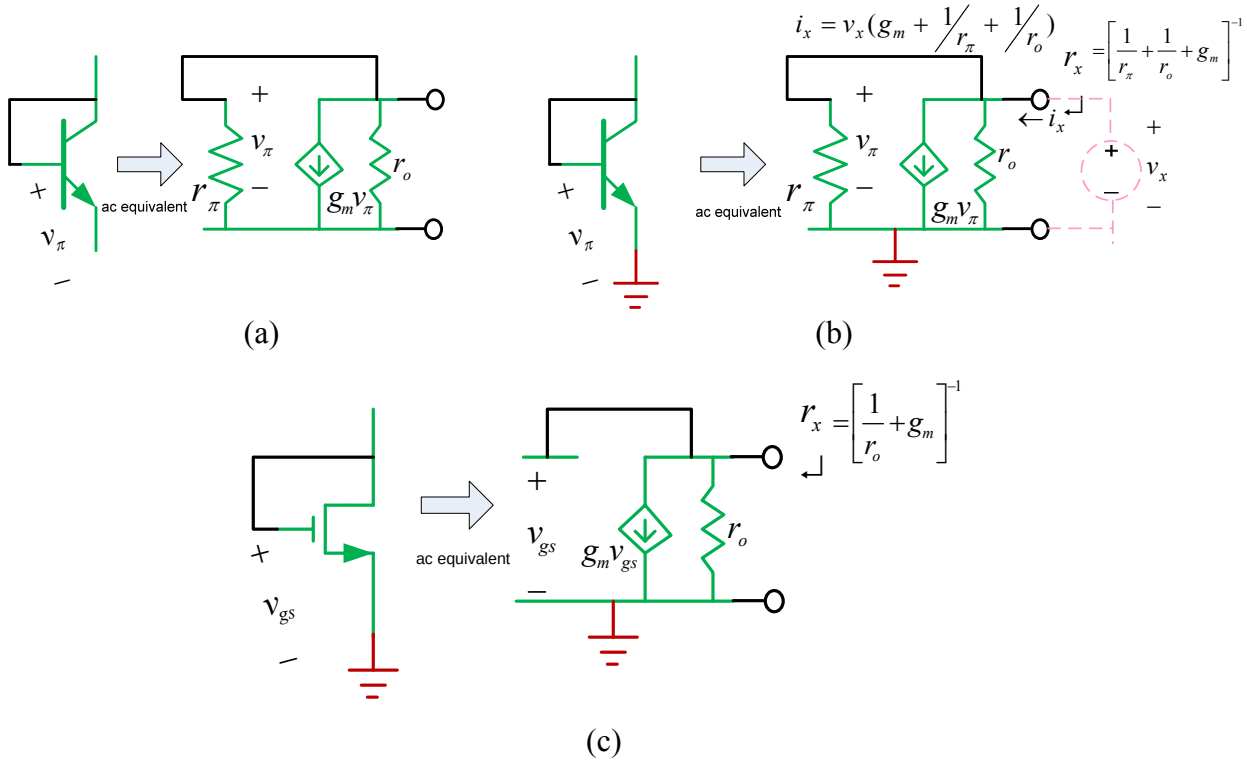
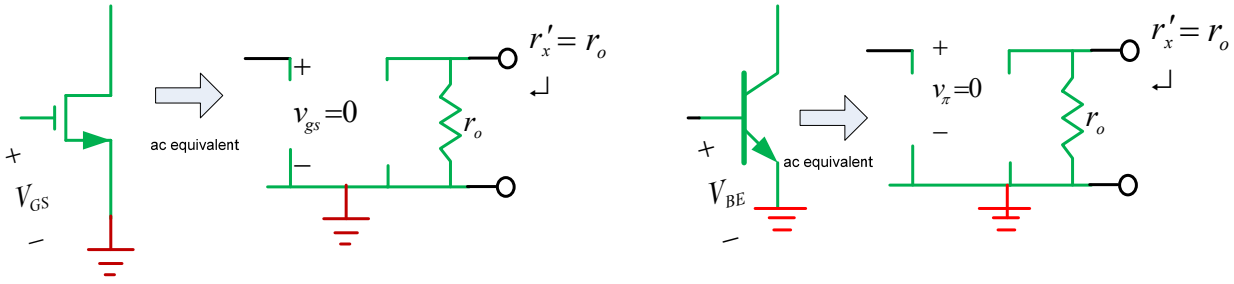


Figure 15: (a) diode connected BJT and ac equivalent circuit, (b) ac output resistance r_x with emitter grounded (i.e., CE configuration) for ac signals, (c) diode connected MOS in CS configuration and the associated ac output resistance.

2.2.1 B: *Current source/sink connected transistor:* In this, the transistor is biased to operate in the active (for BJT) or saturation (for MOS) region in the output characteristics. Thus the collector-emitter (for BJT)/ drain-source (for MOS) nodes pair appear to function like a current source (for DC current) with an attended high value of resistance for small signal

application. A current mirror system can also used for the same purpose. The value of the resistance is approximately the output resistance of the device, i.e., r_o. Since $r_o >> 1/g_m$, when the transistor is operating in the active/saturation region (for BJT/MOS respectively), the current source/sink/mirror configuration is preferred when a high value of small signal resistance is required. Consider the cases below.



(a) (b)

Figure 16: (a) MOS transistor with fixed V_{GS} (or fixed V_{SG} for PMOS), (b) BJT device with fixed V_{BE} (or V_{EB} for NPN BJT).

In figures 16(a)-(b), the control voltages for the VCCS element in the transistors are fixed, i.e., DC. DC implies zero ac. Hence, the controlled current sources do not exist. The output resistance becomes simply r_o of the transistors. This is a high value. Note that the terminal of the device is the *drain* terminal of the MOSFET and the *collector* terminal of the BJT. This is always the case irrespective of whether the device is an NPN/NMOS or PNP/PMOS type.

In summary, if we need a high-valued active resistance, we arrange the device (MOS or BJT) with a DC bias voltage between the controlling node pair (GS for MOS, BE for BJT), and look into the collector/drain of the active device. The ground terminals in Fig.16(a)-(b) could be a DC voltage bus (i.e., zero ac). Thus the transistors are configured to function as a current source/sink.

One must note that the high valued resistance r_o is effective only when the signal follows the direction from collector/drain to emitter/source through the device. The emitter/source end is grounded to ac signals in this case. If, however, the signal follows the path from the emitter/source to collector/drain (i.e., opposite to the first case), the high valued resistance r_o

is not effective. In this case the resistance is approximately $1/g_m$ (the student is suggested to prove it). The collector/drain terminal in this case has to be grounded for ac signals. This situation does not arise for a *diode connected* transistor (i.e., case 2.2.1A).

2.2.2: Use of active loads in single stage amplifiers

2.2.2 A: *CE/CS amplifier*

The schematics for a CE/CS amplifier with an active loads are shown in Figures 17(a), (b) with current mirror active loads and in Figures 17(c), (d) with current source active loads.

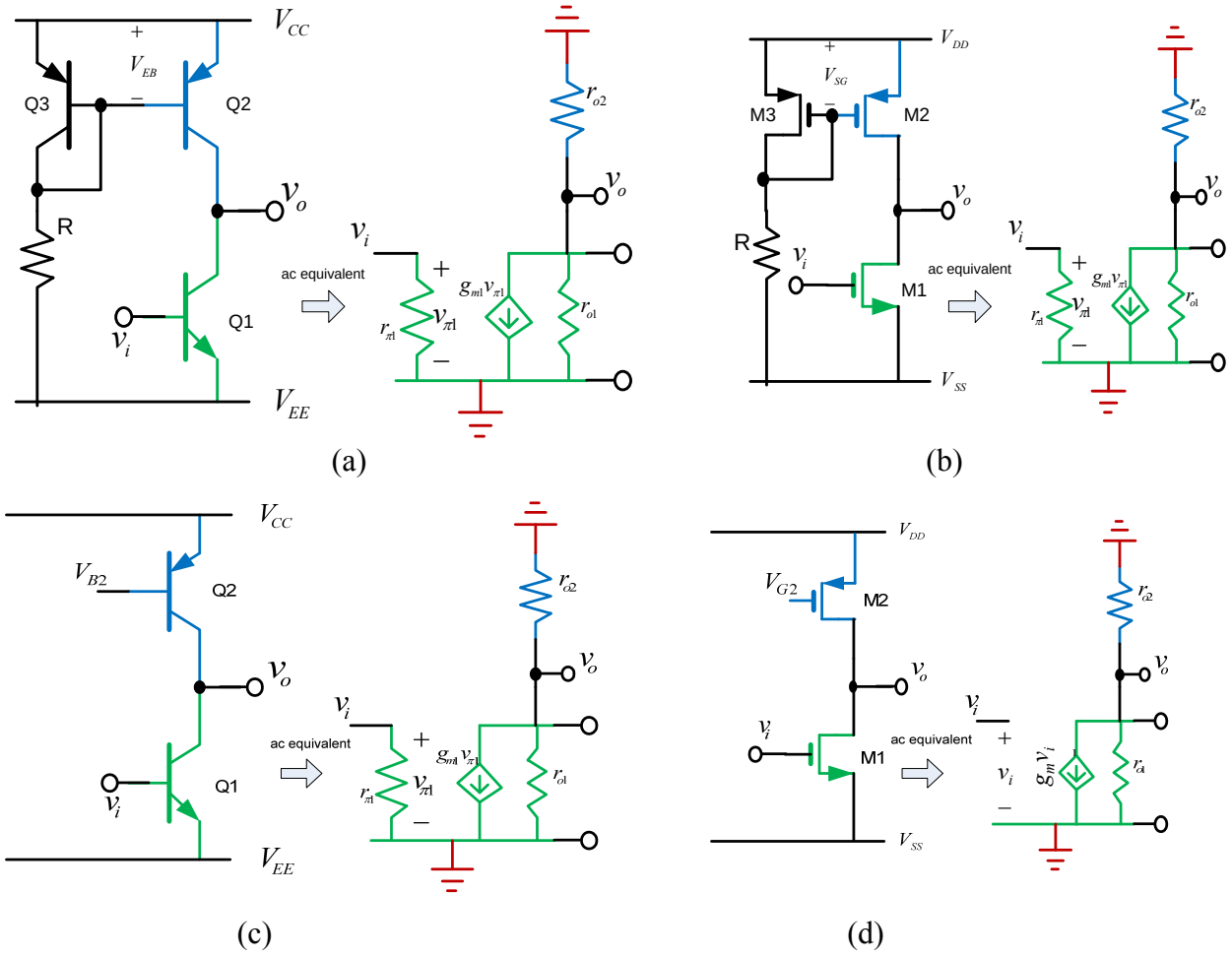


Figure 17: (a) CE BJT amplifier, and (b) CS MOS amplifier, with *current mirror* active load; (c) CE BJT amplifier, and (d) CS MOS amplifier, with *current source* active load

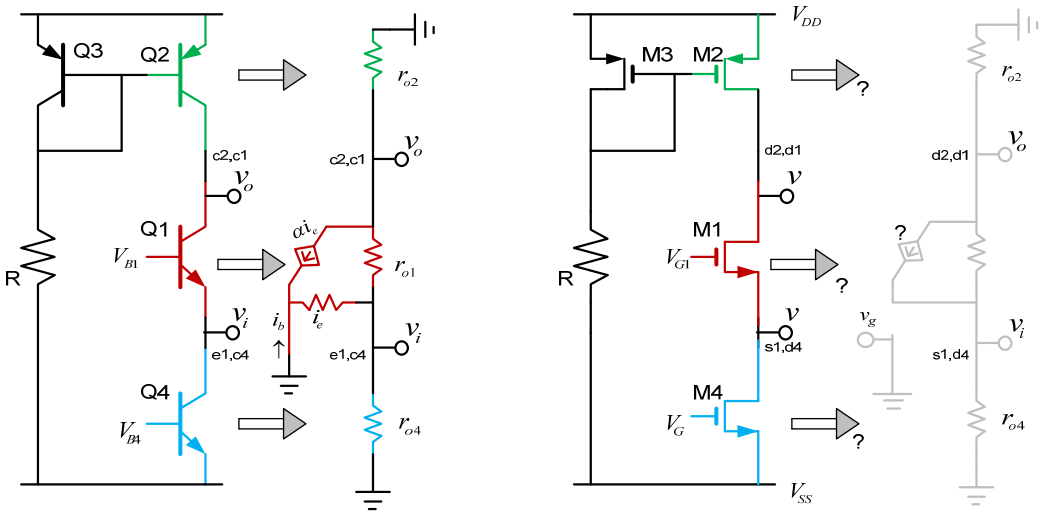
Note that the load transistor is of opposite kind to that of the amplifying device. The amplifying device receives the input ac signal. Since a high voltage gain is required, the current mirror/current source configuration of the active load is employed. This load presents a resistance of r_o for small signal (ac) case. The active load stage has to be biased at the same DC current level as the basic amplifier stage (transistor Q1/M1 in the schematic). This is because the active load is in series connection with the output (collector/drain) terminal of the amplifier stage. If g_m is the transconductance of the amplifier device, the open circuit voltage gain will be given by $-g_m R_L$, where $R_L = r_{o1}||r_{o2}$.

Numerical calculation practice example:

Consider an NMOS amplifier stage with a g_m =200 micro mhos and a bias current of 10 µA. We use a PMOS active load for the amplifier. The Early voltages for the NMOS and PMOS devices are 30 V and 50 V respectively. What voltage gain can be realized from this amplifier?

2.2.2 B: *CB/CG amplifier*

As the name suggests, the base/gate terminal of the amplifying transistor will be held at a constant (DC) voltage. Consider figures 18(a)-(b).

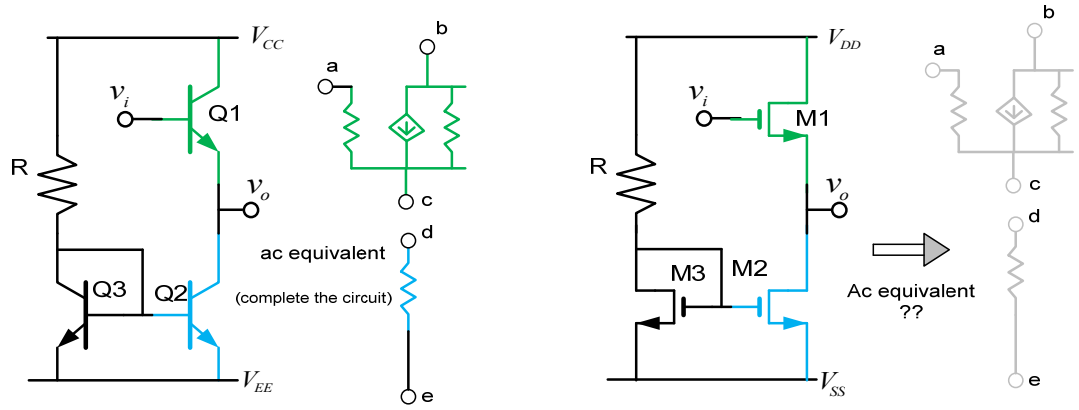


(a) (b)

Figure 18 : (a) CB BJT amplifier with current mirror active load, (b) CG MOS amplifier with current mirror active load.

2.2.2 C: *CC/CD amplifier*

The schematic diagrams are shown below. The collector (of BJT)/drain (of MOS) is connected to a fixed (DC) supply value (i.e., ac ground).



(a) (b)

Figure 18 : (a) CC BJT amplifier with active load (Current mirror), (b) CD MOS amplifier with active load (Current mirror). Which transistors make up the current mirrors ?

2.2.3 Use of active loads in improved current mirrors

2.2.3 A: *Widlar mirror using active load at the emitter*

By using the concept of active loads, we can enhance the output resistance of the Widlar mirror in Fig. 10(a) by replacing R_E with output resistance of a BJT device. The schematic will change to either Fig.19(a) or (b). These are two possible *integrated circuit* implementation of the Widlar mirror. In Fig.19(a), we utilize r_{o3} (why r_{o3} of Q3?) Q3 to replace R_E in Fig.10(a). In Fig.19(b), we utilize $1/g_m$ (why?) of Q3 to replace R_E of Fig.10(a).

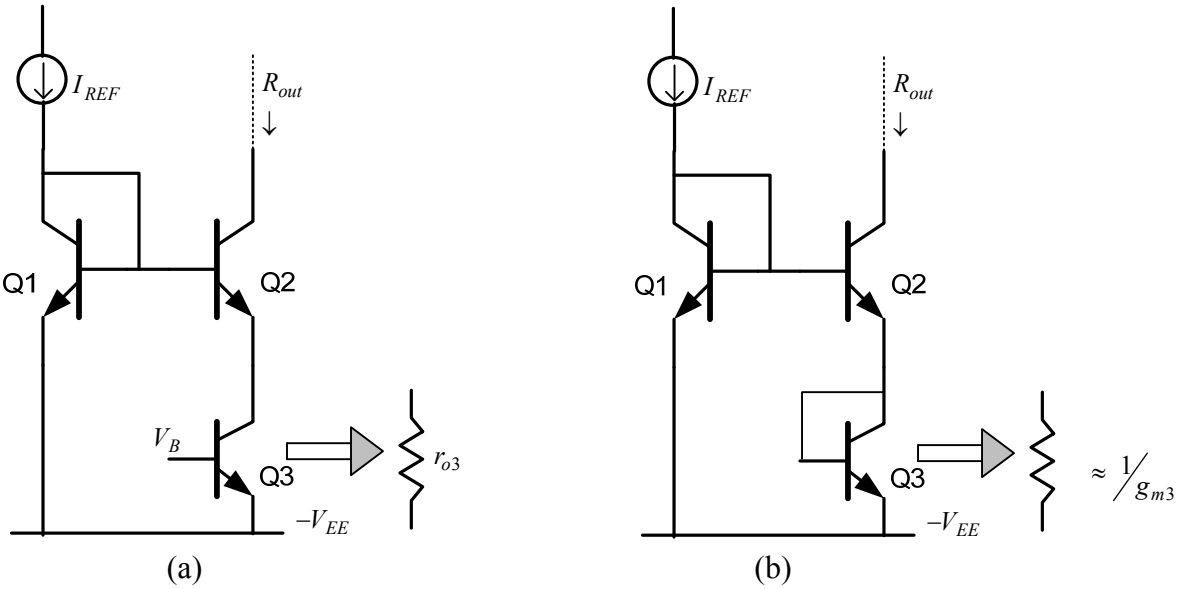
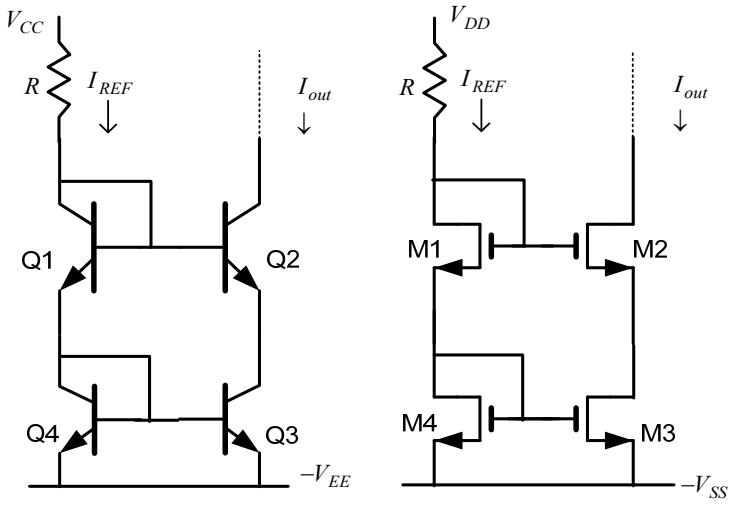


Figure 19: (a) Mirror of Fig.10(a) with R_E replaced by fixed V_{BE} across Q_3, (b) R_E replaced by diode connected Q_3

In practical integrated circuit implementation of the current mirror, we need to replace the I_{REF} by actual circuit elements providing a bias current. This has already been shown in Fig.9, for example.

Finally, use of too many (more than two) independent DC voltage sources is not practical in an actual integrated circuit substrate floor. Hence the arrangement around Q_3 in Fig.15(a) needs a change to reflect Q_3 as providing an *ac* output resistance of r_o. This can be achieved by including Q_3 as part of a current mirror as shown in Fig. 2(a), for example.

2.2.3 B: *Cascode current mirror*



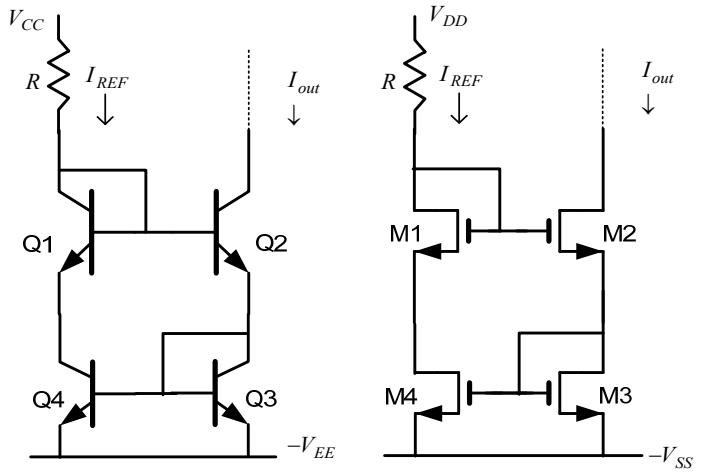
(a) (b)

Figure 20: (a) BJT cascode mirror, (b) MOS cascode mirror.

In Fig.19(a), by making Q_3 as part of the output device of a current mirror, we arrive at the circuit of Fig.20(a). Figure 20(b) shows the version with MOS transistors. These configurations are known as *cascode* current mirrors- Fig. 20(a) is the BJT version and Fig.20(b) is the MOS version of cascode current mirrors.

2.2.3 C: *Wilson current mirror*

In Fig.19(b), by making Q_3 as the diode connected part of a current mirror, we arrive at the circuit of Fig.21(a). Figure 21(b) shows the version with MOS transistors. These configurations are known as *Wilson* current mirrors- Fig. 21(a) is the BJT version and Fig.21(b) is the MOS version of Wilson current mirrors.



(a) (b)

Figure 21: (a) Wilson current mirror with BJT devices, (b) Wilson current mirror with MOS devices.

2.3: Differential amplifiers:

- Differential amplifiers with discrete resistance circuits.
- Differential amplifiers with active loads.

A differential amplifier amplifies difference of two signals. So this amplifier shall have two input nodes. The output can have one or two nodes. In the first case (one output node), the system is simply referred to as a differential-in single-out amplifier. In the second case (output having two nodes), the system will be called as differential-in, differential- out amplifier. Typical schematics of a differential amplifier using BJT and MOS devices are shown below. It can be seen that the emitter terminals of the input devices in a BJT differential amplifier are connected together and a DC current source provides the bias current through this tail-end. For a MOS amplifier, the source terminals of the input devices are connected together. In a discrete component version of the system, the loads are resistances. In an integrated circuit version, the loads will be replaced by active loads.

When the transistors are matched (i.e., identical and of same semiconductor process technology), the output of the differential amplifier will be zero when the two input signal are equal. Thus, a differential amplifier provides good rejection (i.e., produces zero output) for common mode

signals (same signal at the two input nodes). So it is preferably used in a noisy environment (such as the wafer of an IC chip with many systems/subsystems on the same wafer and placed very close to each other). For large signal operation, the differential output system will cancel out the even-order harmonic components of the signal. So this helps in reducing the harmonic distortion at the output. Reducing harmonic distortion and canceling common mode noise are two important features of differential amplifiers.

2.3.1 Differential amplifiers (DA) with transistors and resistances

2.3.1.1 BJT device based DA (Large signal operation)

Figure 22 shows a differential amplifier with BJT devices, and resistive loads. For large signal operation, the basic diode equation can be employed at the base-emitter junction. The analysis follows. All the transistors are assumed to be operating in the active region.

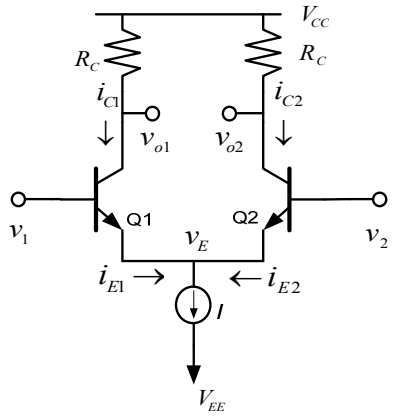


Figure 22: Differential amplifier schematic with BJT and discrete resistances

With identical transistors (i.e., matched transistors) and with zero input signals, $i_{E1} = i_{E2} = I/2$.
With the input signals v_1, v_2 applied, we use the exponential equation for the BE junctions of Q_1 and Q_2. Thus:

$i_{E1} = I_S \exp(\frac{v_1 - v_E}{V_T})$, $i_{E2} = I_S \exp(\frac{v_2 - v_E}{V_T})$, where I_S is the scale current, V_T is the thermal voltage (approx. 25 mV unless given otherwise), and $n = 1$ has been assumed.

When the signals are applied, $I = i_{E1} + i_{E2}$ always holds, although i_{E1} may be $\neq i_{E2}$. This is because I is a steady DC current which distributes between i_{E1} and i_{E2} as the signals v_1 and v_2 changes. On

writing $v_D = v_1 - v_2$= the differential input voltage (ac+DC), and after few algebraic manipulations using the *properties of ratio and proportions*, we can get

$$i_{E1} = I\frac{\exp(v_D/V_T)}{1+\exp(v_D/V_T)}, \quad i_{E2} = I\frac{\exp(-v_D/V_T)}{1+\exp(-v_D/V_T)}. \qquad (3.1.1.1)$$

Now assuming that the transistors have very high β , we can set $i_{C1} = \alpha i_{E1} \approx i_{E1}$, $i_{C2} \approx i_{E2}$. Then

$$v_{o1} = V_{CC} - R_C I\frac{\exp(v_D/V_T)}{1+\exp(v_D/V_T)}, \quad v_{o2} = V_{CC} - R_C I\frac{\exp(-v_D/V_T)}{1+\exp(-v_D/V_T)}, \text{ and}$$

$$v_{o1} - v_{o2} = R_C I\left[\frac{\exp(-v_D/V_T)}{1+\exp(-v_D/V_T)} - \frac{\exp(v_D/V_T)}{1+\exp(v_D/V_T)}\right] \qquad (3.1.1.2)$$

The large signal differential voltage gain is: $G_v = \frac{v_{o1}-v_{o2}}{v_1-v_2} = \frac{v_{o1}-v_{o2}}{v_D}$.

Clearly, the gain is dependent upon the input differential voltage. This implies a non-linear system.

If we write $x = e^{v_D/V_T}$, then $1/x = e^{-v_D/V_T}$, and $v_{o1} - v_{o2} = R_C I[\frac{1}{1+x} - \frac{x}{1+x}]$.

The above can be simplified to $v_{o1} - v_{o2} = -R_C I\frac{e^{v_D/2V_T} - e^{-v_D/2V_T}}{e^{v_D/2V_T} + e^{-v_D/2V_T}} = -R_C I[\text{Tanh}(v_D/2V_T)]$.

2.3.1.2 MOS device based DA (Large signal operation)

An MOS based differential amplifier is shown in Figure 23. Compared to BJT based DA, the MOS DA has infinite input resistance. This feature fits well with the requirement of ideal controlled sources (such as VCVS, VCCS). Using the square law equation (i.e., ignoring the channel length modulation), the large signal operation can be derived as follows. The transistors are assumed to be in the saturation region.

In absence of any signal, $i_{S1} = i_{S2} = I/2$. In presence of signals v_1, v_2, using square-law formula (i.e., ignoring channel length modulation), we can write:

$$i_{D1} = i_{S1} = \mu_n C_{ox}(\frac{W}{2L})_1(v_1 - v_S - V_{THN})^2, \quad i_{D2} = i_{S2} = \mu_n C_{ox}(\frac{W}{2L})_2(v_2 - v_S - V_{THN})^2 \qquad (3.1.2.1)$$

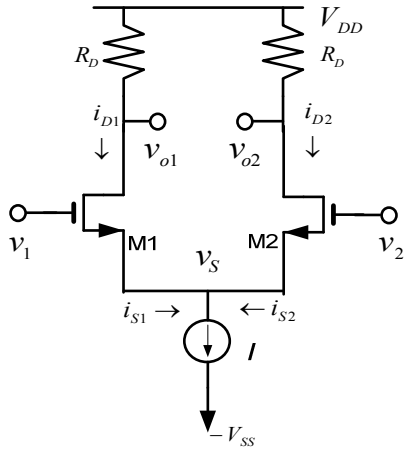


Figure 23: Differential amplifier schematic with NMOS transistors and discrete resistances

The above equations are for NMOS transistors with technological parameters μ_n (electron mobility), C_{ox} (gate oxide capacitance), and V_{THN} (Threshold voltage). For transistors with identical W and L values (i.e., same physical dimensions) $(W/L)_1 = (W/L)_2 = (W/L)$. The body (substrate) terminal of the MOS transistors have not been shown to improve clarity of the diagram. In reality, the body terminal of each of M1 and M2 will be connected to the most negative DC voltage in the system, i.e., to $-V_{SS}$. We can now write

$$v_1 - v_s - V_{THN} = \sqrt{\frac{2L}{W}\frac{1}{K_n} i_{S1}}, \quad v_2 - v_s - V_{THN} = \sqrt{\frac{2L}{W}\frac{1}{K_n} i_{S2}}, \quad K_n = \mu_n C_{ox} \qquad (3.1.2.2)$$

From the above, we get $v_1 - v_2 = v_D = \sqrt{\frac{2L}{K_n W}}(\sqrt{i_{S1}} - \sqrt{i_{S2}})$ (3.1.2.3)

Since I is the DC bias current, $i_{S1} + i_{S2} = I$ always holds. Replacing i_{S2} in terms of I and i_{S1}, and writing $\beta_n = K_n W/2L$; we find $\sqrt{i_{S1}} - \sqrt{I - i_{S1}} = \sqrt{\beta_n}\, v_D$. Squaring both sides we get $I - 2\sqrt{i_{S1}(I - i_{S1})} = \beta_n v_D^2$. Changing sides and squaring again we get, $(I - \beta_n v_D^2)^2 = 4 i_{S!}(I - i_{S1})$.

Then re-arranging as a quadratic equation in i_{S1}, we get $i_{S1}^2 - i_{S1} I + \frac{1}{4}(I - \beta_n v_D^2)^2 = 0$. Solving for i_{S1}, we get $i_{S1} = \frac{I}{2} \pm \frac{1}{2}\sqrt{2\beta_n v_D^2 I - \beta_n^2 v_D^4}$. Selecting $i_{S1} = \frac{I}{2} + \frac{1}{2}\sqrt{2\beta_n v_D^2 I - \beta_n^2 v_D^4}$, we will get $i_{S2} = I - i_{S1} = \frac{I}{2} - \frac{1}{2}\sqrt{2\beta_n v_D^2 I - \beta_n^2 v_D^4}$. Knowing that $i_{D1} = i_{S1}$, $i_{D2} = i_{S2}$ and with more simplification, we arrive at

$$i_{D1} = \frac{I}{2} + \sqrt{\frac{\beta_n I}{2}}\sqrt{1 - \frac{\beta_n v_D^2}{2I}}v_D\,,\; i_{D2} = \frac{I}{2} - \sqrt{\frac{\beta_n I}{2}}\sqrt{1 - \frac{\beta_n v_D^2}{2I}}v_D \qquad (3.1.2.4)$$

Since, $v_{o1} = V_{DD} - R_D i_{D1}, \quad v_{o2} = V_{DD} - R_D i_{D2}$, we can get to:

$$v_{o1} - v_{o2} = -R_D v_D\left[\sqrt{2\beta_n I}\sqrt{1 - \beta_n v_D^2 \big/ 2I}\right] \qquad (3.1.2.5)$$

The differential voltage gain is $G_v = \frac{v_{o1} - v_{o2}}{v_D} = -R_D\left[\sqrt{2\beta_n I}\sqrt{1 - \beta_n v_D^2 \big/ 2I}\right]$ (3.1.2.6)

Since the gain depends upon the input differential voltage, the gain is not constant. This is the characteristic of a non-linear system. Under the condition $\frac{\beta_n v_D^2}{2I} << 1$, i.e., $v_D << \sqrt{2I \big/ \beta_n}$, we can get the linear approximation which is good for small signal application. The result is:

$G_v\,|_{linear} = \frac{v_{o1} - v_{o2}}{v_D} = -R_D\sqrt{2\beta_n I}$.

2.3.1.3 Small signal operation (BJT based DA)

The basic schematic and the associated ac equivalent circuit of a BJT-based DA are shown in figures 24(a)-(c). Note that for simplicity of analysis the output resistance r_o has been ignored (assumption $r_o \rightarrow$ infinity).

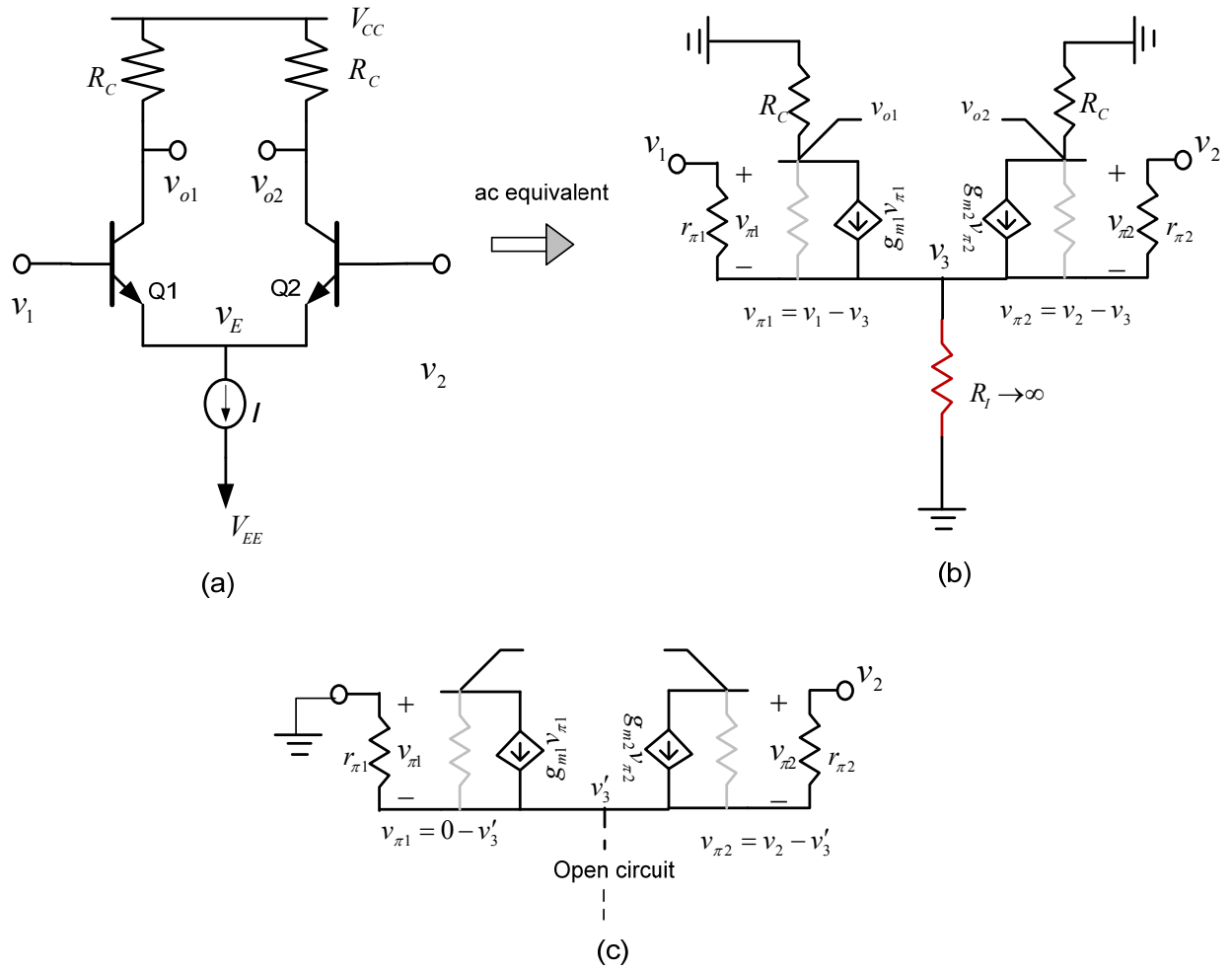


Figure 24: (a) schematic of the differential amplifier, (b) ac equivalent circuit (approximate), (c) equivalent circuit for partial (i.e., with v_1 =0, v_2 effective) calculations.

2.3.1.3 A: *emitter node voltage*

To calculate v_3 we can use principle of superposition (the small signal ac equivalent circuit has linear circuit elements, so superposition principle is applicable). Thus, with v_1=0, we get the part v_3' due to v_2 alone. From Fig $-\frac{v_2 - v_3'}{r_\pi} - g_m(v_2 - v_3') - g_m(0 - v_3') + \frac{v_3'}{r_\pi} = 0$ .24(c), assuming that the transistors are matched (i.e., $r_{\pi 1} = r_{\pi 2} = r_\pi$, $g_{m1} = g_{m2} = g_m$), the KCL at the v_3' node leads to

$$-\frac{v_2 - v_3'}{r_\pi} - g_m(v_2 - v_3') - g_m(0 - v_3') + \frac{v_3'}{r_\pi} = 0 \qquad (3.1.3.1)$$

On simplification, we get $v_3' = v_2/2$. Similarly, keeping v_2=0 and applying v_1, we can get the part v_3'' of v_3 as $v_3'' = v_1/2$.

Thus, $v_3 = v_3' + v_3'' = (v_1 + v_2)/2$ (3.1.3.2)

2.3.1.3 B: *Small signal voltage gain* (balanced differential operation)

For balanced differential (i.e., v_1=-v_2), v_3 =0. Then

$$v_{o1} = -g_m v_1 R_C,\ v_{o2} = -g_m v_2 R_C,\quad v_{o1} - v_{o2} = -g_m R_C (v_1 - v_2) \qquad (3.1.3.3)$$

The voltage gain is thus (v_{o1}-v_{o2})/(v_1-v_2) =-$g_m R_C$.

The gain expression derived above is remarkably the same as one would obtain for a CE amplifier with r_o of the device assumed to → infinity. Thus the differential amplifier, with balanced differential input, functions like a simple CE amplifier! The observation can be easily appreciated by recognizing that with balanced differential input signals the voltage $v_3 = v_1$+v_2 =0, i.e., the emitter terminals of the two transistors are at (virtually) zero signal potential. Hence each of the left and right halves of the system behaves like a CE amplifier with the emitter returned to signal ground.

The above observation leads to a simplified analysis of differential amplifiers in terms of two single stage half circuits.

2.3.1.3 C: *Differential input resistance* (balanced differential operation)

With the assumption of r_o = infinity for both the transistors, simple observation on Fig.24(c) will lead to the conclusion that $R_{in}|_{\text{bal diff}} = 2r_\pi$.

2.3.1.3 D: *Single-ended small signal voltage gain*

The associated ac equivalent circuit can be derived from Fig.24(c) and is shown in Fig.25.

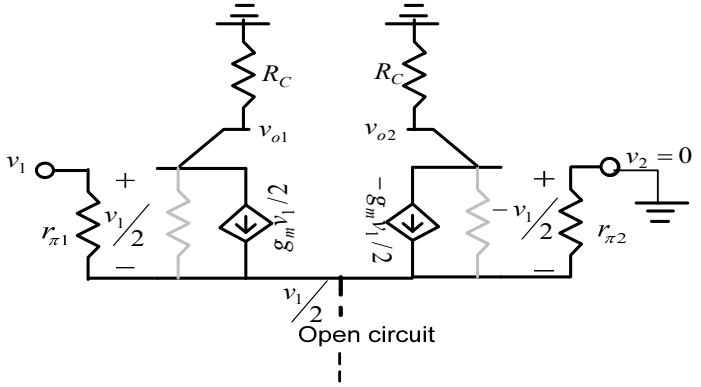


Figure 25: Small signal equivalent circuit for single input operation

Clearly, $v_{o1} = -g_m R_C v1/2$, $v_{o2} = g_m R_C v_1/2$. Then the differential output voltage signal = $v_{o1} - v_{o2}$ $=- g_m R_C v_1$.The voltage gain is then $-g_m R_C$.

2.3.1.3 E: *Common mode voltage gain*

Now we shall consider $v_1=v_2=v_{CM}$. Then $v_3= v_{CM}$ (see eq. 3.1.3.2). In this case, we shall have v_{o1} = v_{o2} = 0. Accordingly, the differential output voltage is zero! Since we are considering identical matched transistors calculating a differential voltage gain with *zero* differential input signal voltage becomes meaningless.

We therefore calculate the single-ended voltage gain, i.e., v_{o1}/v_{CM}. We now divide the amplifier into two halves (half circuits) as shown in Fig.26. Each half is like a CE amplifier with un-bypassed resistance in the emitter. The derivation follows. Consider only one half-circuit. KCL at the node of v_x gives

$$-\frac{v_{CM}-v_x}{r_\pi} - g_m(v_{CM}-v_x) + \frac{v_x}{2R_I} = 0 \qquad (3.1.3.4)$$

Solving for v_x, we get $$v_x = \frac{2v_{CM}(g_m r_\pi + 1)R_I}{r_\pi + 2R_I(g_m r_\pi + 1)} \qquad (3.1.3.5)$$

The output signal voltage $v_{o1} = -g_m R_C (v_{CM} - v_x) = -\frac{g_m r_\pi R_C v_{CM}}{r_\pi + 2R_I(g_m r_\pi + 1)}$ (3.1.3.6)

Remembering that $g_m r_\pi = \beta, r_\pi = (\beta+1)r_e, (\beta+1)/\beta = 1/\alpha$, we can finally get the common mode gain $G_{CM} = -v_{o1}/v_{CM} = -\frac{\alpha R_C}{r_e + 2R_I} \approx \frac{\alpha R_C}{2R_I}$. This is approximately same as the voltage gain of a CE BJT amplifier with an un-bypassed emitter resistance of r_e (internal to the transistor) in series with $2R$ (external to the transistor).

Half circuit #1 **Half circuit #2**

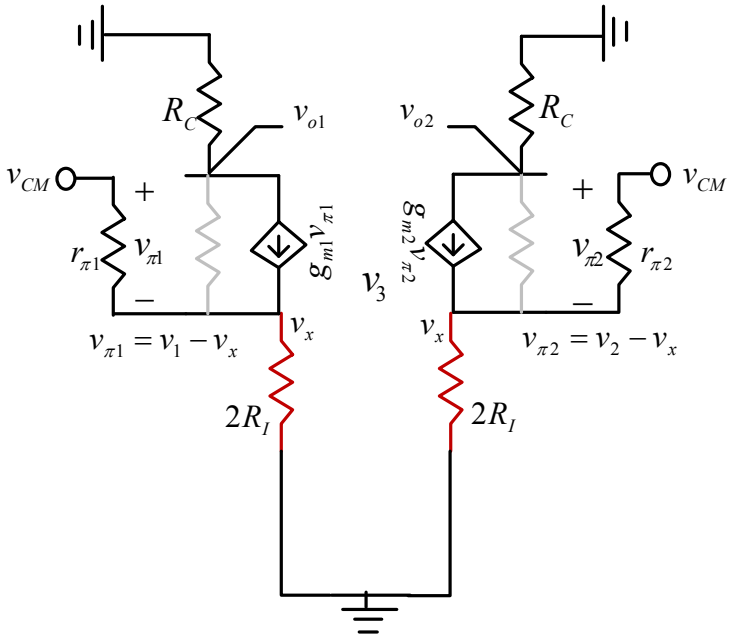


Figure 26: Decomposition of the differential amplifier schematic into two half-circuits.

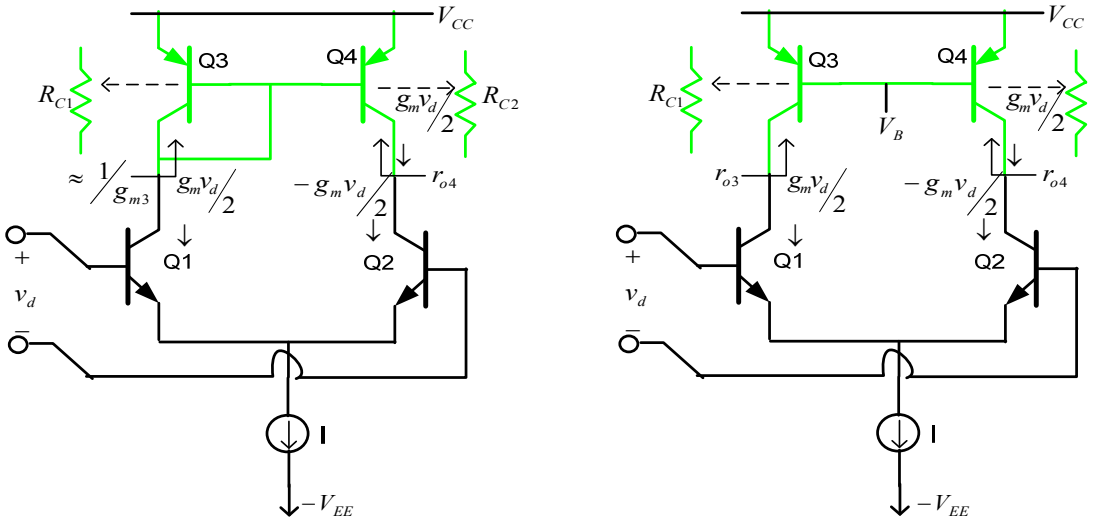
For the balanced differential operation with $v_1=v_d/2$, we would have $v_{o1} = -g_m R_C(v_d/2)$, so that differential voltage gain (for only one input effective) would be $A_d = -g_m R_C/2$.

2.3.1.3 F : *Common mode rejection ratio* (CMRR)

The quality of a differential amplifier is quite often judged by the decibel ratio of the differential gain to the common mode gain. This is referred to as common mode rejection ratio (CMRR). This is then $20\log_{10}(A_d / A_c) = 20\log_{10}(\frac{g_m R_C/2}{\alpha R_C/2R}) = 20\log_{10}(\frac{g_m R}{\alpha})$, where $R=R_I$ is the small signal resistance of the bias current source. Typical values of CMRR are between 60 dB to 90 dB.

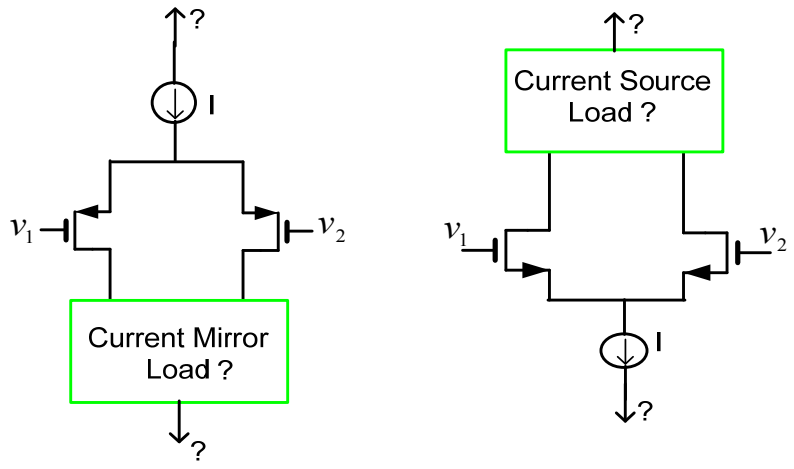
2.3.2 Differential amplifier with active loads

In an integrated circuit environment, discrete resistors are not preferred. Active loads are used instead of the resistors. Depending upon the nature of the output signal, either current mirror load or current source load is used. The two possibilities for BJT based differential amplifiers are shown in figures 27(a)-(b).



(a) (b)

Figure 27: BJT based differential amplifier with active loads; (a) current mirror load, (b) current source load



(a) (b)

Figure 28: MOST-based DA with active loads; (a) current mirror load, (b) current source load.

The student is asked to fill up the details. The body (bulk) terminals of the MOSTs are not shown

Figures 28(a)-(b) depict the MOS transistor (MOST) based differential amplifiers (DA) with current mirror and current source active loads respectively. The student may try to fill up the details using his/her understanding of the active loads.

The MOS or CMOS technology is primarily used now- a- days for integrated circuits and systems. So we can work with a MOST-based DA for signal related analysis or calculations.

For a current mirror based DA, consider figures 29(a) and (b) for the schematic and the associated small signal the equivalent circuit respectively. The amplifying devices are NMOS while the active loads are comprised of PMOS transistors.

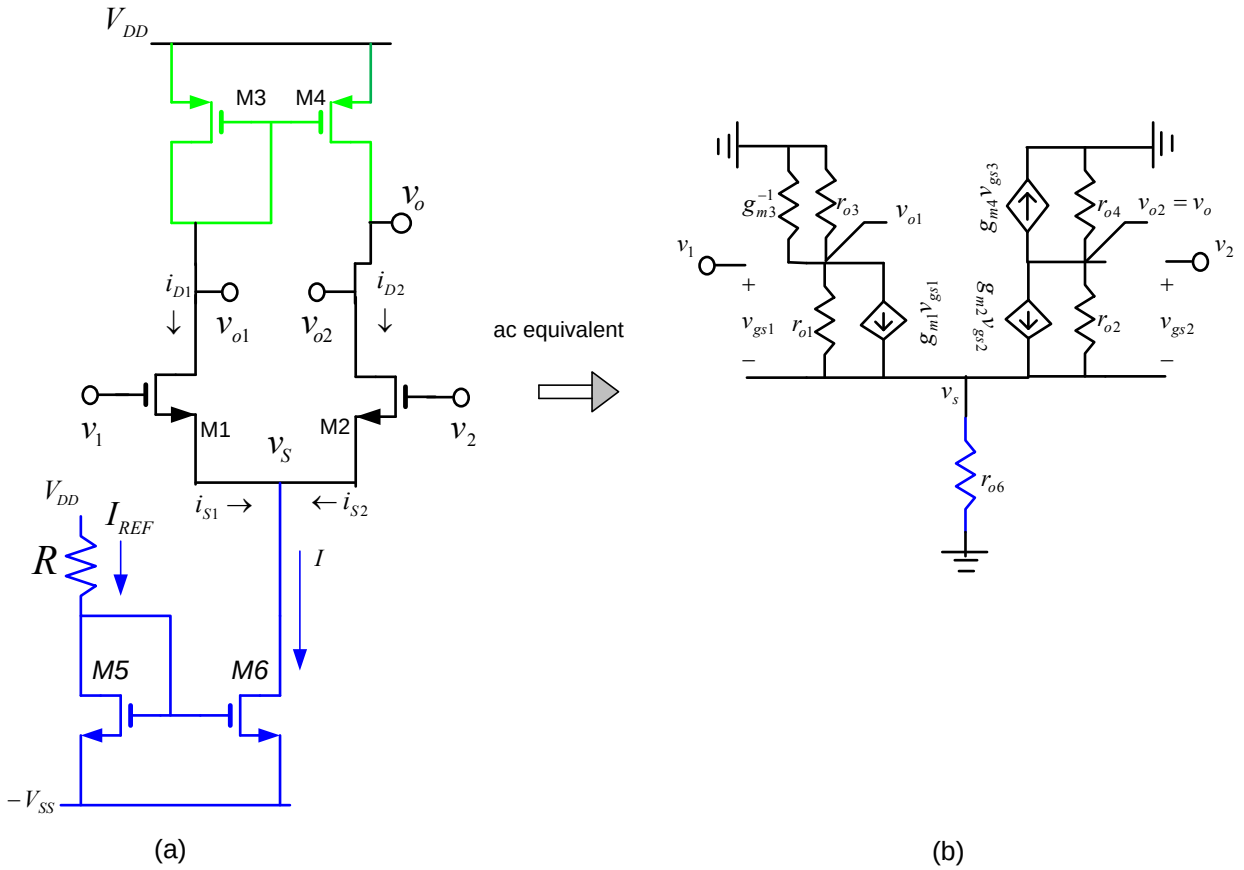


Figure 29: (a) A CMOS DA with current mirror load and current mirror bias current source, (b) ac equivalent circuit at low frequency (i.e., ignoring any parasitic capacitances).

Analysis: To begin an approximate analysis, we will introduce several simplifying assumptions. Thus the NMOS transistors M1,M2 are considered matched pair of transistors. So $g_{m1}=g_{m2}=g_{mn}$, $r_{o1}=r_{o2}=r_{dn}$. Similarly, the PMOS pair M3,M4 are considered matched. So $g_{m3}=g_{m4}=g_{mp}$, and $r_{o3}=r_{04}=r_{dp}$. Let us introduce the conductance parameter $g_{xy}=1/r_{xy}$.

We will then carry out the analysis for *balanced* differential input signals, i.e., $v_1=v_d/2$, $v_2=-v_d/2$. Consequently, $v_s=0$, $v_{gs1}=v_d/2$, $v_{gs2}=-v_d/2$. Further the circuit configuration of the current mirror dictates $v_{gs3}=v_{o1}$

The KCL at v_{o2} node is: $g_{dp}v_{o2} + g_{mp}v_{o1} - g_{mn}\frac{v_d}{2} + g_{dn}v_{o2} = 0$ (2.3.2.1)

The KCL at v_{o1} node is: $g_{dp}v_{o1} + g_{mp}v_{o1} + g_{mn}\frac{v_d}{2} + g_{dn}v_{o1} = 0$ (2.3.2.2)

From (2.3.2.2) $v_{o1} = \frac{-g_{mn}(v_d/2)}{g_{dp} + g_{mp} + g_{dn}}$ g (2.3.2.3)

Substituting for v_{o1} from (2.3.2.3) in (2.3.2.1), we will get

$$v_{o2} = \frac{1}{2}\frac{g_{mn}(2g_{mp} + g_{dp} + g_{dn})}{(g_{dp} + g_{dn})(g_{dp} + g_{dn} + g_{mp})}v_d \quad (2.3.2.4)$$

Considering that in a practical case g_{mn} is >> g_{dp} or g_{dn}, and hence ignoring g_{dn}+g_{dp} in comparison with g_{mn}, (2.3.2.4) simplifies to: $v_{o2} = \frac{g_{mn}}{g_{dp} + g_{dn}}v_d$ (2.3.2.5)

The *differential-in* , *single- out* voltage gain is therefore: $\frac{g_{mn}}{g_{dp} + g_{dn}} = g_{mn} \times r_{on} \,||\, r_{op}$ (2.3.2.6)

In (2.3.2.6), r_{on} =1/g_{dn}, r_{op} =1/g_{dp}. The expression in (2.3.2.6) is surprisingly similar to the voltage gain expression of a CS- MOST amplifier circuit! So it should be easy to remember. Note that v_{o2} is in phase with v_d with +v_d/2 applied at the v_1 terminal of the differential amplifier in Fig. 29(a). Similarly, v_{o2} will be 180^o out of phase with v_2 (i.e., -v_d/2).

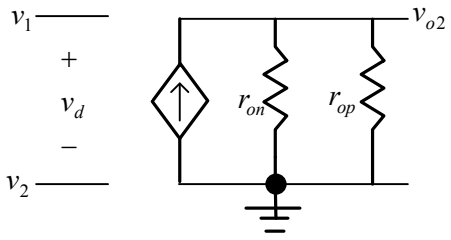


Figure 30: Simple ac equivalent circuit for the differential amplifier in Fig.29(a).

The expression in (2.3.2.6) can be modeled by an ac equivalent circuit as in figure 30. Note that the *input is differential* (i.e., both the terminals are floating, none is grounded), the output is *single-ended* (one of the output terminals is grounded). This is the characteristic of a DA using current mirror as active load, i.e., a *differential input* signal is amplified and delivered as a *single-ended* voltage at the output.

Viewed in another way, we need to *employ a DA with current mirror active load* if conversion *from a differential input* signal *to a single-ended output* signal is desired. For *fully differential* (i.e., differential-in, differential out) operation, the amplifying transistors (such as M1, M2 in Fig.29(a)) are to be used with *current source/sink active load* devices.

The student is suggested to draw up the schematics of

(i) A differential-in, single-out amplifier where PMOS transistors are used as the amplifying devices. That is to say, the PMOS devices receive the input signal.

(ii) A fully differential (i.e., differential-in, differential-out) amplifier with NMOS transistors as the signal amplifiers (i.e., NMOS devices receiving the input signal).

(iii) Repeat (ii) for PMPS transistors as the amplifying devices.

2.3.3 Multi-stage amplifier (MOST and BJT based Operational Amplifier examples)

The student is now fairly familiar with all the basic circuit modules employed in an integrated circuit. It is interesting to see how several such modules are interconnected to produce a versatile integrated circuit amplifier, such as an operational amplifier (OP-AMP).

2.3.3.1: A two-stage MOS operational amplifier (OP-AMP)

Figure 31 depicts the schematic of a two-stage CMOS operational amplifier[1]. Let us calculate the voltage gain that can be afforded by this circuit.

Toward this, we need to know about the bias currents and the characteristics of the devices, such as width (W), length (L), transconductance factor ($\mu_n C_{ox}$, $\mu_p C_{ox}$), threshold voltages (V_{THN}, V_{THP}), and the *Early* voltages (V_{AN}, V_{AP}). Consider the following given information.

W/L values (Table)

Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L (in μm)	20/0.5	20/0.5	5/0.5	5/0.5	40/0.5	10/0.5	40/0.5	40/0.5

[1] Figure 8.41, *Microelectronic Circuits* by Sedra and Smith, 6th edn., ©2010 , Oxford University Press Inc, ch.8.

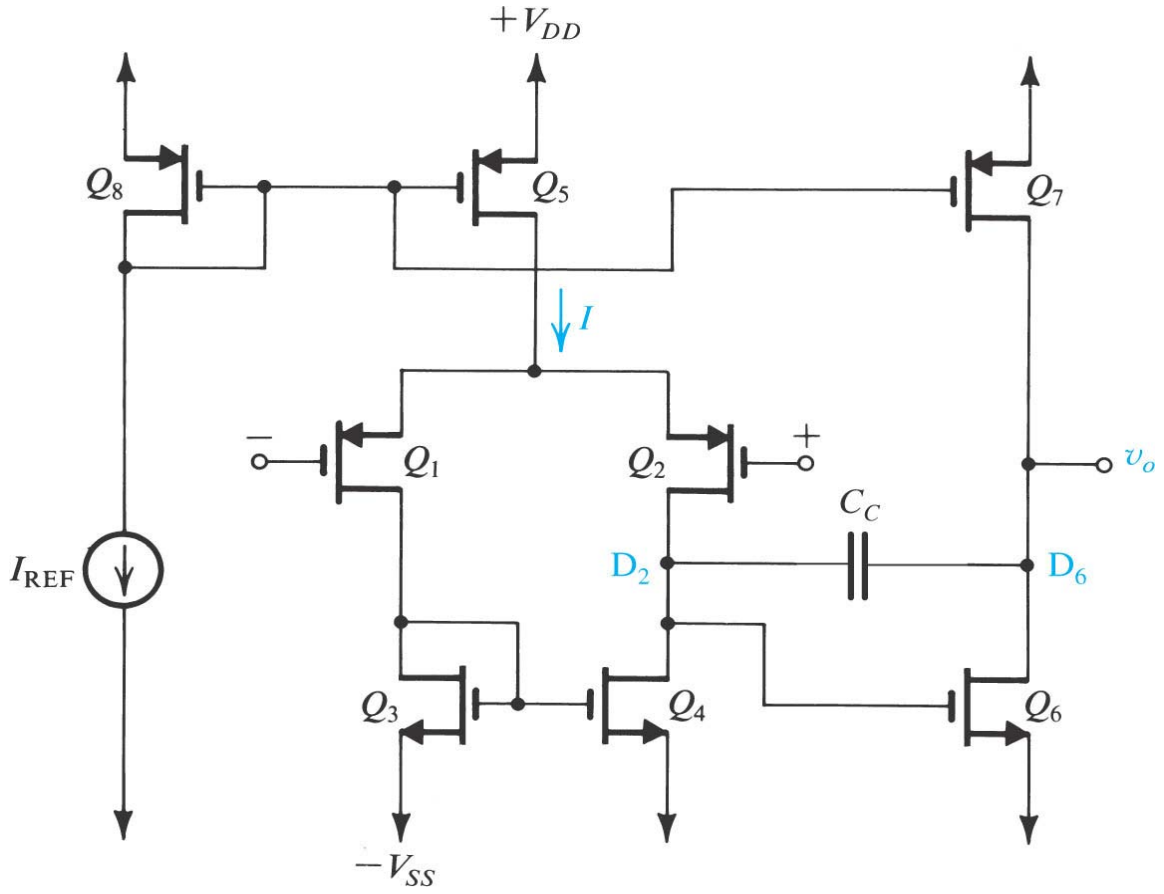


Figure 31: Schematic of a two-stage CMOS operational amplifier

Further, $\mu_n C_{ox}$=200 $\mu A/V^2$, $\mu_p C_{ox}$ =60 $\mu A/V^2$, V_{THN}=0.7 V, V_{THP}=-0.8 V, V_{AN} =10 V, V_{AP} =12 V, V_{DD} =V_{SS} =1.8 V, and I_{REF} = 120 μA.

Inspection of Fig.31 reveals that the OP-AMP has a DA as the signal input stage (Q_1, Q_2). The devices are PMOS transistors. A PMOS current mirror system (Q_5, Q_7, Q_8) *supplies the DC bias* current to the amplifying stages.

The DA has an NMOS current mirror as active load. The stage that follows the DA is an NMOS-CS amplifier (Q_6) with a PMOS (Q_7) current mirror as *active load.*

The capacitor C_C provides *frequency compensation* to ensure stable operation of the OP-AMP when connected in a negative-feedback for signal processing. The concept of frequency compensation will be discussed in chapter 3 of this note-pack.

Since the voltage gain depends upon g_m of the signal-driven transistor(s) and the output resistances of the signal-driven transistor and of the transistor forming the active load (i.e., r_{op}, r_{on}), we need to find the pertinent g_m values (i.e., of Q_1,Q_2,Q_6 –these are driven by the signal),and the output resistances of Q_2, Q_4, Q_6, and Q_7. The g_m and output resistance values depend upon the

DC bias current. So we need to find the bias currents through the different stages (a stage is a column of transistors in the schematic).

Thus, considering that Q_8, Q_5 and Q_7 form current mirrors and that the *W/L* values for these are identical (see the Table) we conclude that $I_5=I_7=I_{REF}=120\ \mu A$.

Since I_5 divides equally between Q_1 and Q_2, we can determine $I_1=I_2=I_{REF}/2=60\ \mu A$. Since Q_3 is in series with Q_1, and likewise Q_4 is with Q_2, we know $I_3=I_4=I_1=I_2=60\ \mu A$. Similarly, $I_6=I_7=120\ \mu A$.

Using the square-law equation for the drain current in the MOST, i.e., $I_D=(1/2)\mu C_{ox}(W/L)V_{ov}^2$, where $V_{ov}=|V_{GS}|-|V_{TH}|$, we can determine the following quantities

For Q_1, Q_2 :

I_D=120/2 μA, $\mu_n C_{ox}$=200 $\mu A/V^2$ (for NMOS), *W*/L = 20/0.5, V_{OV} =0.122 V.

Further, since the transconductance $g_m=\partial I_D/\partial V_{OV}=2I_D/V_{OV}$, we get $g_{mQ1}=g_{mQ2}=9.836\times10^{-4}$ mho.

For Q_2,Q_4 :

The output resistances are dependent upon the *Early* voltage and DC bias current. Thus, $r_{o2}=V_{AN}/I_{DQ2}$ =166.67 *k*Ω. Similarly, $r_{o4}=V_{AP}/I_{DQ4}$ =200 *k*Ω.

Then signal voltage gain of stage#1 (i.e., Q_2, Q_4 pair) is $-g_{mQ2}\times r_{o2}\,||\,r_{o4}$ = -89.42 V/V

For Q_6, Q_7 :

I_{DQ7}= 120 μA (by current mirroring principle, and since $(W/L)_{Q7}=(W/L)_{Q8}$).

Also, I_{DQ6} = 120 μA (since Q_6, Q_7 are in series).

For Q_6 , V_{OV} =0.245 V, $g_{mQ6}=9.796\times10^{-4}$, r_{o6} =83.33 *k*Ω.

For Q_7 , r_{07} =100 *k*Ω.

The signal voltage gain of stage#2 (i.e., Q_6 , Q_7 pair) is $-g_{mQ6}\times r_{o6}\,||\,r_{o7}$ = -44.53 V/V

Overall voltage gain of the two stage OP-AMP= $-89.42\times(-44.53)$=3989.92 V/V.

The above serves as an example to calculate the voltage gains in a cascade of multi-stage MOS amplifiers. The above gain is the gain of the two- stage OP-AMP as depicted in Figure 31.

The voltage gain is not the only parameter of interest for an OP-AMP. Several other performance characteristics, such as: (i) offset voltage, offset current, -3dB bandwidth, unity-gain bandwidth, CMRR, slew rate, settling time, power supply rejection ratio (PSRR), input common mode range (CMR), total DC power consumption, harmonic distortion, noise figure etc., are important. Interested students are

encouraged to read more advanced books[2] and or take a course on, for example, *introduction to analog VLSI*.

2.3.3.2: MOS based Operational Amplifier (a second example)[3]

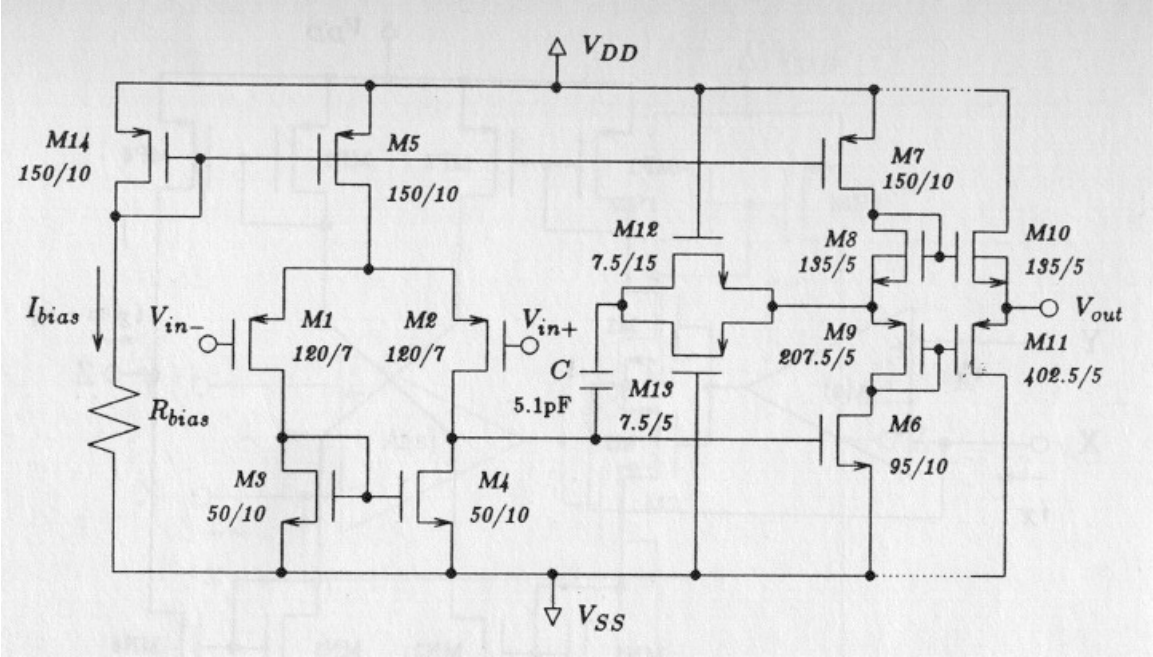


Figure 32: A CMOS OP-AMP with a class AB output stage.

Discussion: Figure 32 presents a three-stage OP-AMP including a class AB output stage. The output stage offers a low output impedance – an important criterion for a voltage amplifier (i.e., VCVS).

The input DA is comprised of two PMOS transistors (M1,M2), with PMOS current mirror (M14,M5) bias source and NMOS (M3,M4) current mirror (active) load.

The capacitor C together with transistors M12, M13 form a series C,R frequency compensation circuit.

[2] See the list at the end of this chapter

[3] *Analog IC design: the current-mode approach,* Edited by C. Toumazou, F.J. Lidgey & D.G. Haigh © April 1990: Peter Peregrinus Ltd., London, United Kingdom, ISBN 0 86341 215 7

The second stage of amplification comes from the NMOS transistor M6 which has an active load comprised of the diode connected transistors (M8,M9) in series with the current mirror load (M7).

Transistors M10 (NMOS), M11 (PMOS) together with the diode connected transistors (M8,M9) from a class AB output stage. Since the output is taken from the source terminals of M10, M11, the output resistance will be small.

The *W*/*L* data shown are in microns.

2.3.3.3: BJT based OP-AMP

Please refer to *Microelectronic Circuits* by Sedra and Smith, 6th edn., ©2010 , Oxford University Press Inc, ch.8, p.657-663.

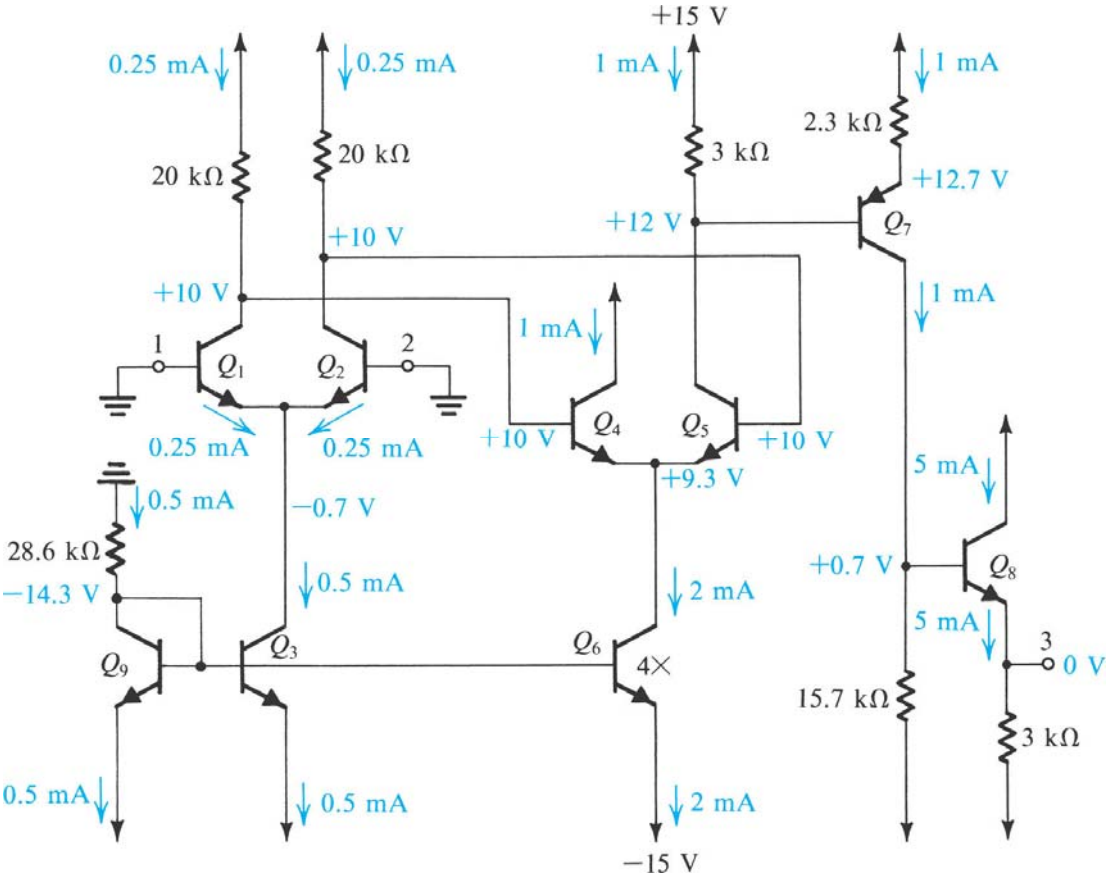
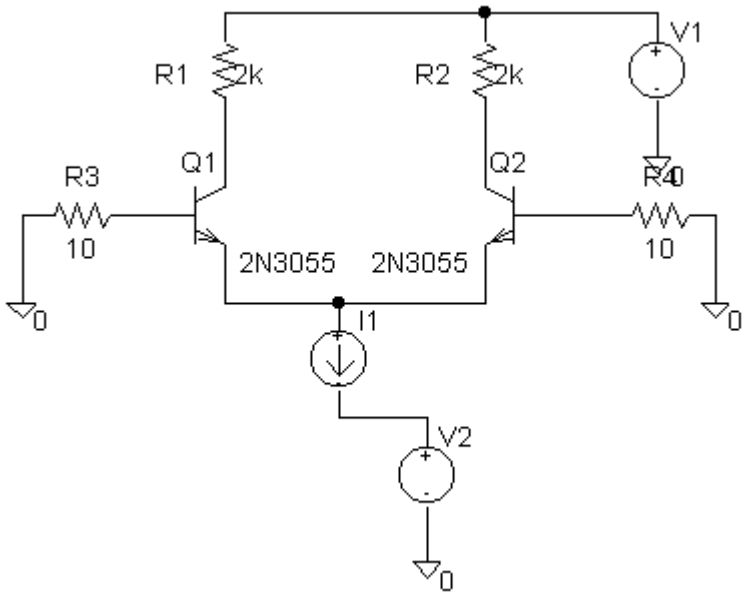


Figure 33: A four-stage BJT OP-AMP

For analyzing the circuit operation, and calculating the voltage gain and input/output resistances, please read ref#1, p.657-663.

2.4 : Practice Exercises

Q.1: Consider the schematic of a differential amplifier below. The output listing for the network in pSPICE format is appended. Using this listing do the following:



- Draw an ac equivalent circuit model for the amplifier.
- Using necessary theoretical formula and the relevant component values from the output listing, find the (a) voltage gain, and (b) input resistance for small signal operation.

* Schematics Netlist *

R_R1 $N_0002 $N_0001 2k
R_R2 $N_0003 $N_0001 2k
V_V1 $N_0001 0 DC 5
V_V2 $N_0004 0 DC -5

Q_Q1 $N_0002 $N_0005 $N_0006 Q2N3055

R_R4 $N_0007 0 10

R_R3 0 $N_0005 10

Q_Q2 $N_0003 $N_0007 $N_0006 Q2N3055

I_I1 $N_0006 $N_0004 DC 5m

SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) 5.0000 ($N_0002) .1730

($N_0003) .1730 ($N_0004) -5.0000

($N_0005)-864.9E-06 ($N_0006) -.5602

($N_0007)-864.9E-06

VOLTAGE SOURCE CURRENTS

NAME CURRENT

V_V1 -4.827E-03

V_V2 5.000E-03

TOTAL POWER DISSIPATION 4.91E-02 WATTS

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**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2
MODEL	Q2N3055	Q2N3055
IB	8.65E-05	8.65E-05
IC	2.41E-03	2.41E-03
VBE	5.59E-01	5.59E-01
VBC	-1.74E-01	-1.74E-01
VCE	7.33E-01	7.33E-01
BETADC	2.79E+01	2.79E+01
GM	9.32E-02	9.32E-02
RPI	4.59E+02	4.59E+02
RX	1.00E-01	1.00E-01
RO	2.08E+04	2.08E+04
CBE	4.48E-09	4.48E-09

CBC 2.58E-10 2.58E-10

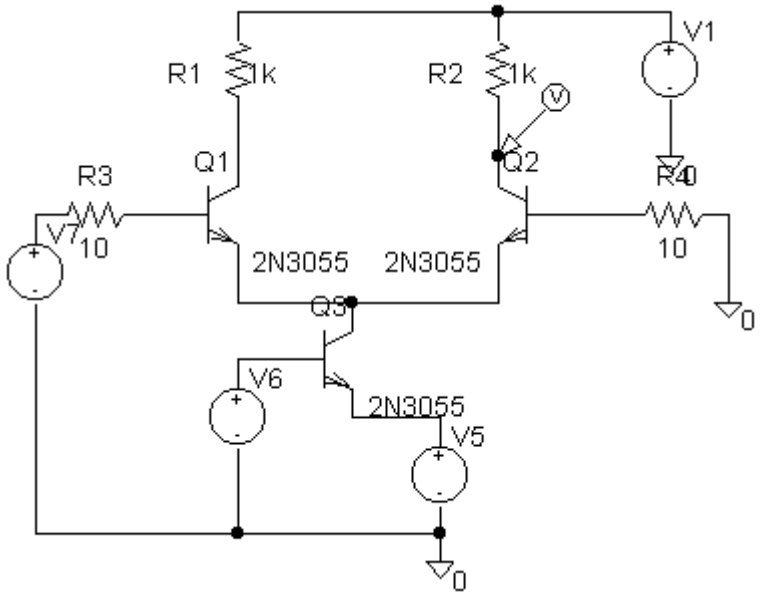
CJS 0.00E+00 0.00E+00

BETAAC 4.28E+01 4.28E+01

CBX 0.00E+00 0.00E+00

FT 3.13E+06 3.13E+06

Q.2: For the network below, the output listing is appended. Repeat the work done in Q.1 above.



* Schematics Netlist *

Q_Q1 $N_0002 $N_0001 $N_0003 Q2N3055

R_R4 $N_0004 0 10

Q_Q3 $N_0003 $N_0005 $N_0006 Q2N3055

R_R1 $N_0002 $N_0007 1k

V_V1 $N_0007 0 DC 5

R_R3 $N_0008 $N_0001 10

R_R2 $N_0009 $N_0007 1k

V_V5 $N_0006 0 DC -5

V_V6 $N_0005 0 DC -4.4295

V_V7 $N_0008 0 DC 0 AC 1

Q_Q2 $N_0009 $N_0004 $N_0003 Q2N3055

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001)-719.5E-06 ($N_0002) 3.0812

($N_0003) -.5527 ($N_0004)-719.5E-06

($N_0005) -4.4295 ($N_0006) -5.0000

($N_0007) 5.0000 ($N_0008) 0.0000

($N_0009) 3.0812

VOLTAGE SOURCE CURRENTS

NAME CURRENT

V_V1 -3.838E-03

V_V5 4.096E-03

V_V6 -1.149E-04

V_V7 -7.195E-05

TOTAL POWER DISSIPATION 3.92E-02 WATTS

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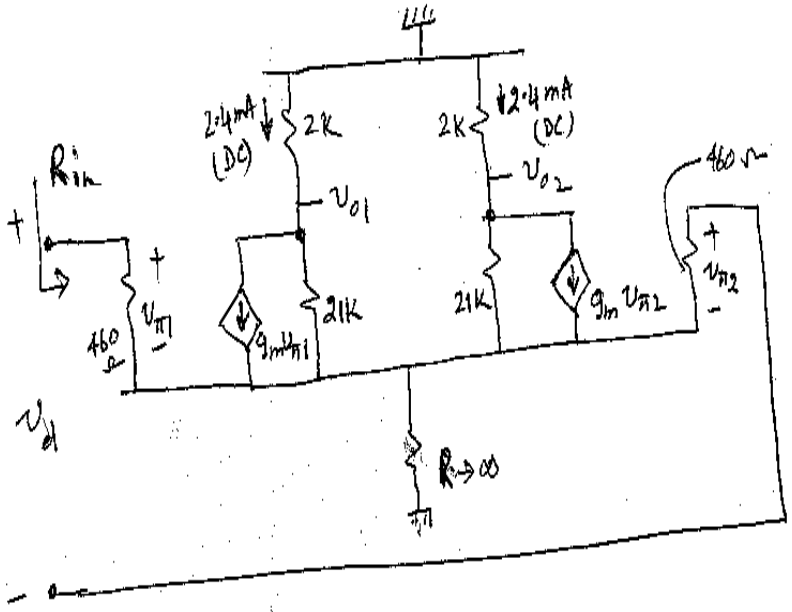
**** BIPOLAR JUNCTION TRANSISTORS

NAME Q_Q1 Q_Q3 Q_Q2

MODEL Q2N3055 Q2N3055 Q2N3055

IB	7.19E-05	1.15E-04	7.19E-05
IC	1.92E-03	3.98E-03	1.92E-03
VBE	5.52E-01	5.71E-01	5.52E-01
VBC	-3.08E+00	-3.88E+00	-3.08E+00
VCE	3.63E+00	4.45E+00	3.63E+00
BETADC	2.67E+01	3.46E+01	2.67E+01
GM	7.41E-02	1.54E-01	7.41E-02
RPI	5.64E+02	3.35E+02	5.64E+02
RX	1.00E-01	1.00E-01	1.00E-01
RO	2.77E+04	1.35E+04	2.77E+04
CBE	3.73E-09	6.86E-09	3.73E-09
CBC	1.60E-10	1.51E-10	1.60E-10
CJS	0.00E+00	0.00E+00	0.00E+00
BETAAC	4.18E+01	5.15E+01	4.18E+01
CBX	0.00E+00	0.00E+00	0.00E+00
FT	3.03E+06	3.49E+06	3.03E+06

* Q3: The ac equivalent circuit of a BJT differential amplifier is shown below. Determine the input impedance and differential voltage gain $(v_{o1}-v_{o2})/v_d$



Given

$h_{fe} = 43$

$g_m = \frac{I_{DC}}{V_T}$

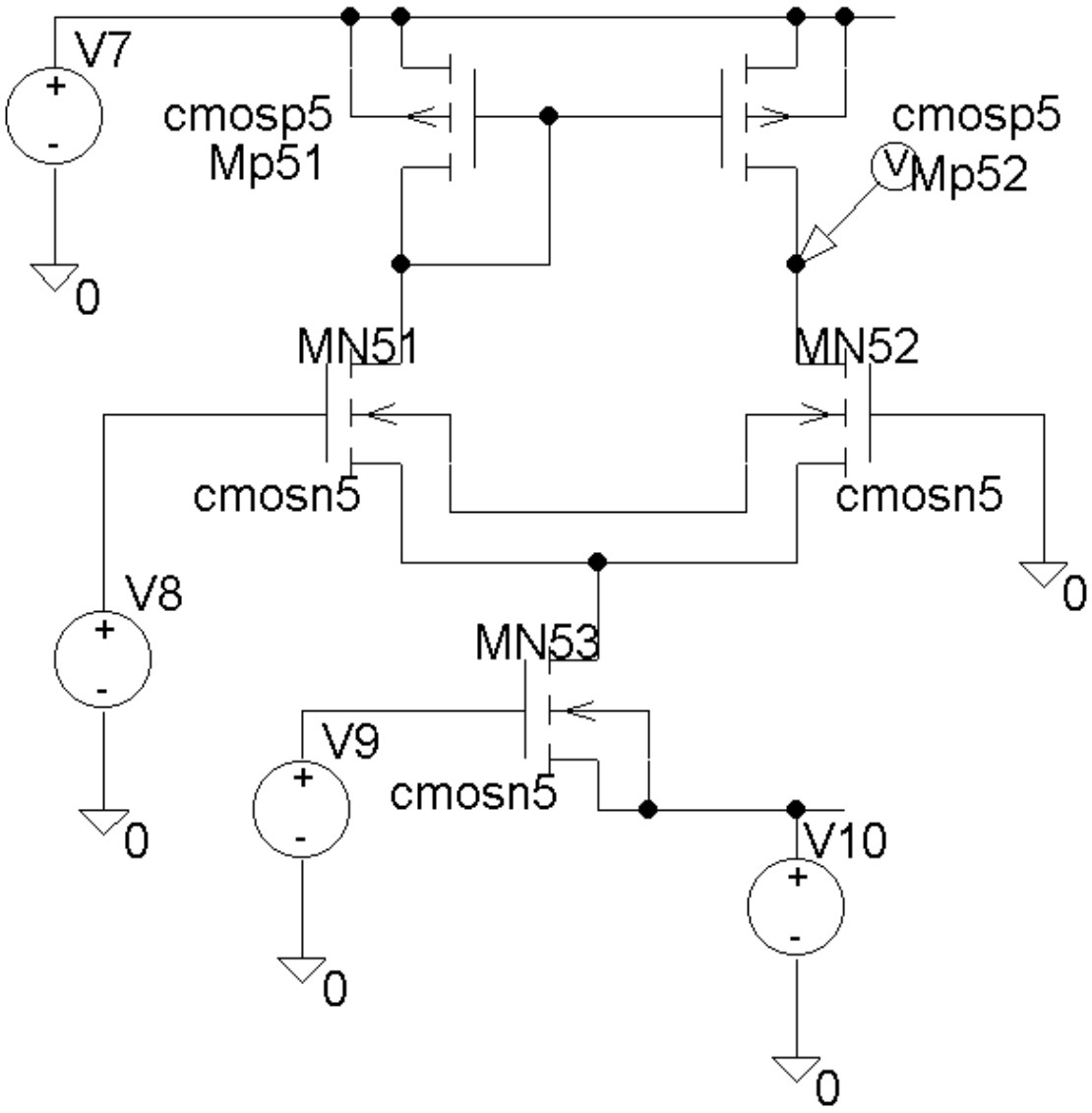
$V_T = \frac{kT}{q} \simeq 25mV$ at room temperature.

Q4 Repeat Q3 when $R = 14K\Omega$

Q.5: Deleted

Q.6: Consider the schematic and the output file listing for the differential amplifier shown below.

- Draw the ac equivalent circuit for the amplifier using standard symbols (i.e., g_m, r_{ds} ..)
- Estimate the voltage gain of the amplifier using the data form the output listing and relevant formula learned in your lecture class. The output node is where the voltage probe is attached.



**** INCLUDING CMR_study.net ****

* Schematics Netlist *

M_Mp51 $N_0001 $N_0001 $N_0002 $N_0002 cmosp5

+ L=2u

+ W=18u

M_Mp52 $N_0003 $N_0001 $N_0002 $N_0002 cmosp5

+ L=2u

+ W=18u

```
M_MN51        $N_0001 $N_0005 $N_0004 $N_0006 cmosn5
+ L=2u
+ W=5u
M_MN52        $N_0003 0 $N_0004 $N_0006 cmosn5
+ L=2u
+ W=5u
M_MN53        $N_0004 $N_0008 $N_0007 $N_0007 cmosn5
+ L=2u
+ W=10u
V_V10         $N_0007 0 DC -1.5
V_V9        $N_0008 0 DC -.5
V_V7        $N_0002 0 DC 1.5
V_V8        $N_0005 0 DC 0 AC 1


****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
********************************************************************************
 NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE
($N_0001)     .2325              ($N_0002)    1.5000

($N_0003)     .2325              ($N_0004)    -.9651

($N_0005)    0.0000              ($N_0006)    -.8457

($N_0007)   -1.5000              ($N_0008)    -.5000

   VOLTAGE SOURCE CURRENTS
   NAME        CURRENT

   V_V10       4.951E-05
   V_V9        0.000E+00
```

V_V7 -4.951E-05

V_V8 0.000E+00

TOTAL POWER DISSIPATION 1.49E-04 WATTS

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**** 01/02/104 09:58:50 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\CMR_study.sch

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

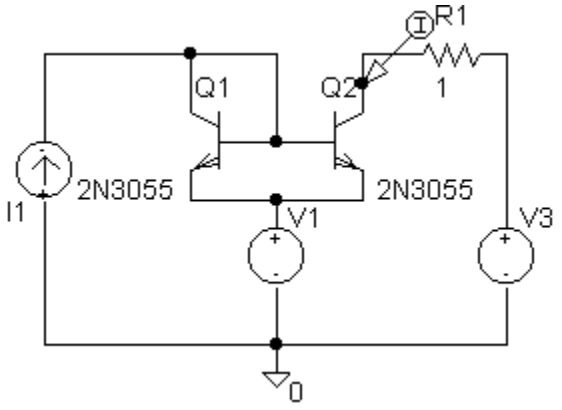
****

**** MOSFETS

NAME	M_Mp51	M_Mp52	M_MN51	M_MN52	M_MN53
MODEL	cmosp5	cmosp5	cmosn5	cmosn5	cmosn5
ID	-2.48E-05	-2.48E-05	2.48E-05	2.48E-05	4.95E-05
VGS	-1.27E+00	-1.27E+00	9.65E-01	9.65E-01	1.00E+00
VDS	-1.27E+00	-1.27E+00	1.20E+00	1.20E+00	5.35E-01
VBS	0.00E+00	0.00E+00	1.19E-01	1.19E-01	0.00E+00
VTH	-9.43E-01	-9.43E-01	6.46E-01	6.46E-01	6.82E-01
VDSAT	-3.20E-01	-3.20E-01	2.96E-01	2.96E-01	2.99E-01
GM	1.31E-04	1.31E-04	1.29E-04	1.29E-04	2.59E-04
GDS	1.10E-07	1.10E-07	2.46E-07	2.46E-07	5.42E-07
GMB	3.28E-05	3.28E-05	3.68E-05	3.68E-05	8.62E-05
CBD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CBS	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGSOV	4.31E-15	4.31E-15	1.53E-15	1.53E-15	3.05E-15

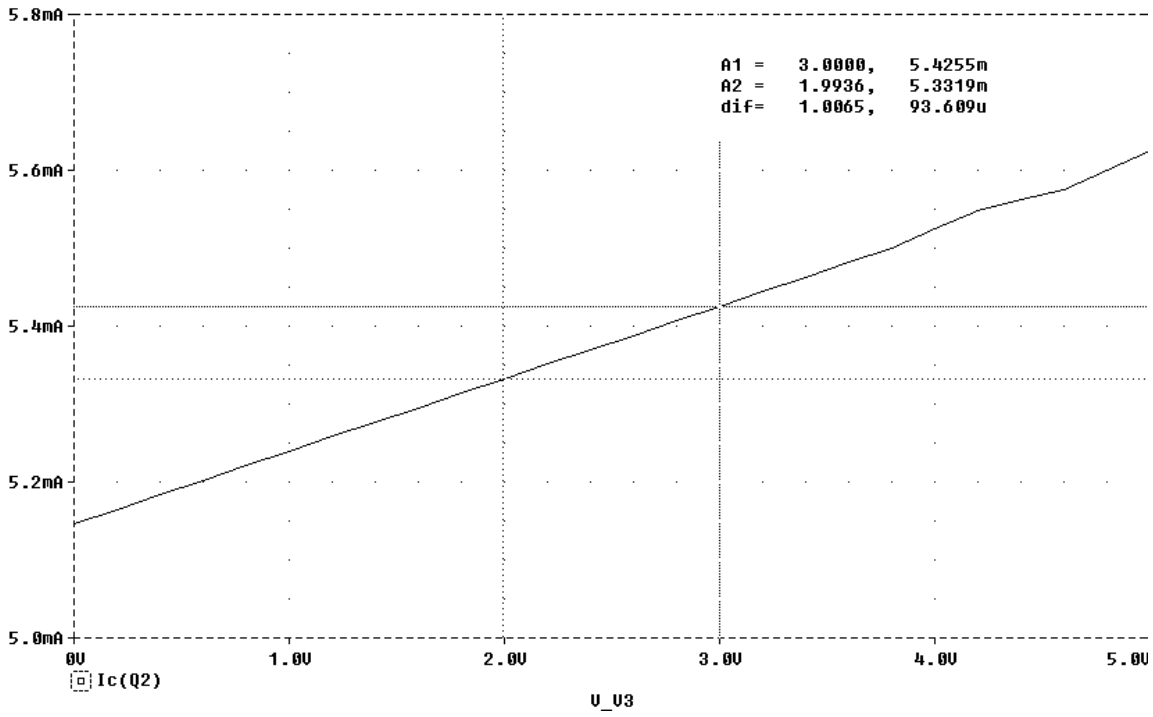
CGDOV	4.31E-15	4.31E-15	1.53E-15	1.53E-15	3.05E-15
CGBOV	7.25E-16	7.25E-16	7.67E-16	7.67E-16	7.67E-16
CGS	8.33E-14	8.33E-14	2.28E-14	2.28E-14	4.57E-14
CGD	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
CGB	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

Q.7: The figure below shows a BJT-based simple current mirror. The DC bias current in Q1 is 5 mA. The schematic represents a test set up to measure the output impedance of



Basic current mirror

the current mirror. The relevant graphical behavior is shown below. The Y-axis is the current into the collector pin of Q2 (the output transistor). What is the output resistance of this mirror?



Q.8: The simulation result for the above current mirror is appended below. What is the expected output resistance for the mirror? Use the pertinent data for the transistors to determine the output resistance. Compare this with the value you get from the above graph.

* Schematics Netlist *

I_I1 0 $N_0001 DC 5m
Q_Q1 $N_0001 $N_0001 $N_0002 Q2N3055
V_V1 $N_0002 0 DC -5
Q_Q2 $N_0003 $N_0001 $N_0002 Q2N3055
V_V3 $N_0004 0 DC 5
R_R1 $N_0003 $N_0004 1

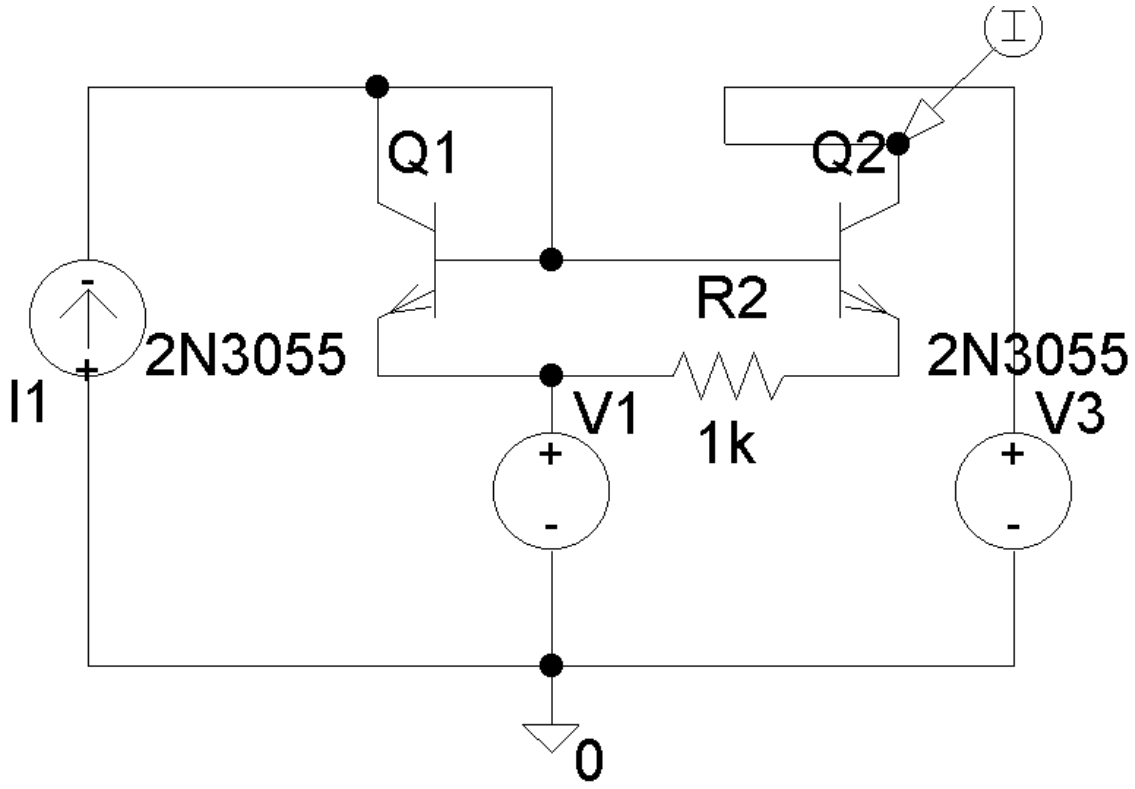
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

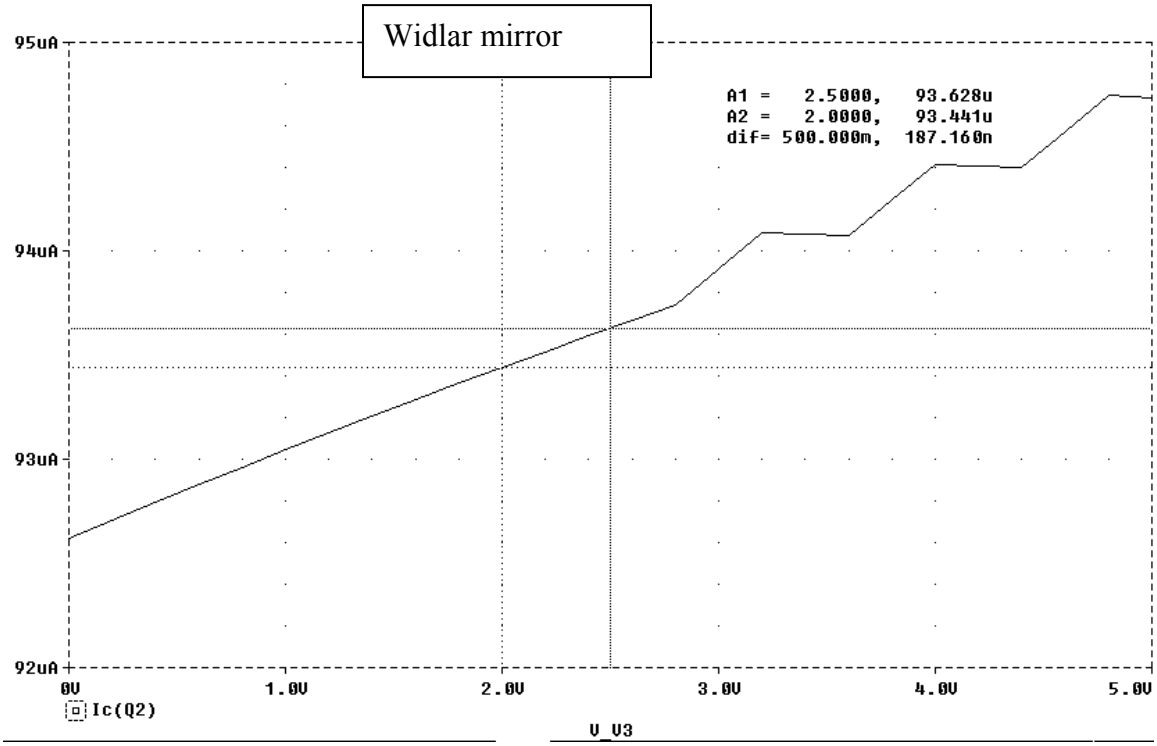
****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2
MODEL	Q2N3055	Q2N3055
IB	1.36E-04	1.36E-04
IC	4.73E-03	5.62E-03
VBE	5.77E-01	5.77E-01
VBC	0.00E+00	-9.42E+00
VCE	5.77E-01	9.99E+00
BETADC	3.48E+01	4.14E+01
GM	1.83E-01	2.17E-01
RPI	2.78E+02	2.78E+02
RX	1.00E-01	1.00E-01
RO	1.06E+04	1.06E+04
CBE	7.99E-09	9.33E-09
CBC	2.76E-10	1.16E-10
CJS	0.00E+00	0.00E+00
BETAAC	5.07E+01	6.03E+01
CBX	0.00E+00	0.00E+00
FT	3.52E+06	3.65E+06

Q.9: For the Widlar mirror below, the output current voltage characteristic is shown in the accompanying graph. Determine the output resistance.


Q1
Q2
R2
2N3055
2N3055
I1
V1
1k
V3
0


Widlar mirror
95uA
94uA
93uA
92uA
A1 = 2.5000, 93.628u
A2 = 2.0000, 93.441u
dif= 500.000m, 187.160n
0V
1.0V
2.0V
3.0V
4.0V
5.0V
Ic(Q2)
V_V3

Q.10: The simulated output listing for the above mirror is attached below. Use necessary formula and the relevant data to calculate the R_{out}. Compare with the value obtained from the graph.

Schematics Netlist *

```
Q_Q1        $N_0001 $N_0001 $N_0002 Q2N3055
V_V3        $N_0003 0 DC 5
V_V1        $N_0002 0 DC -5
R_R2        $N_0002 $N_0004  1k
Q_Q2        $N_0003 $N_0001 $N_0004 Q2N3055
I_I1        0 $N_0001 DC 5m
```

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) -4.4225 ($N_0002) -5.0000

($N_0003) 5.0000 ($N_0004) -4.8937

VOLTAGE SOURCE CURRENTS

NAME CURRENT

V_V3 -9.473E-05

V_V1 5.095E-03

TOTAL POWER DISSIPATION 2.59E-02 WATTS

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**** 01/03/104 10:06:09 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

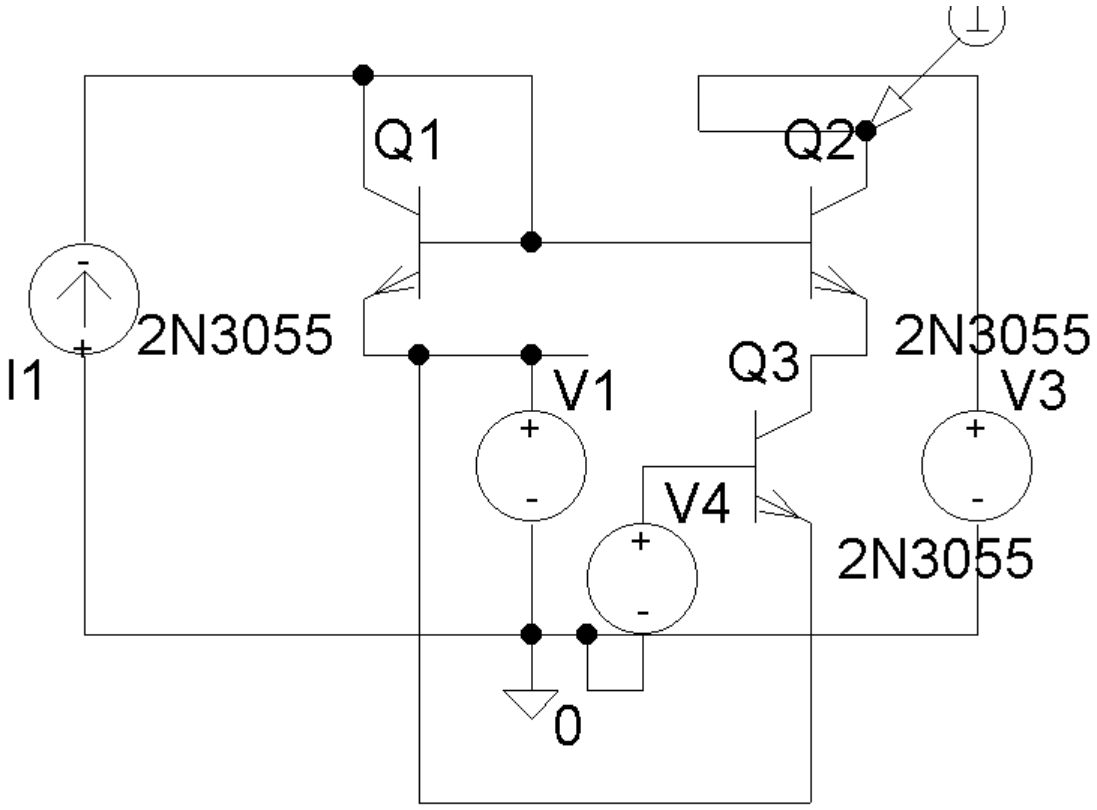
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

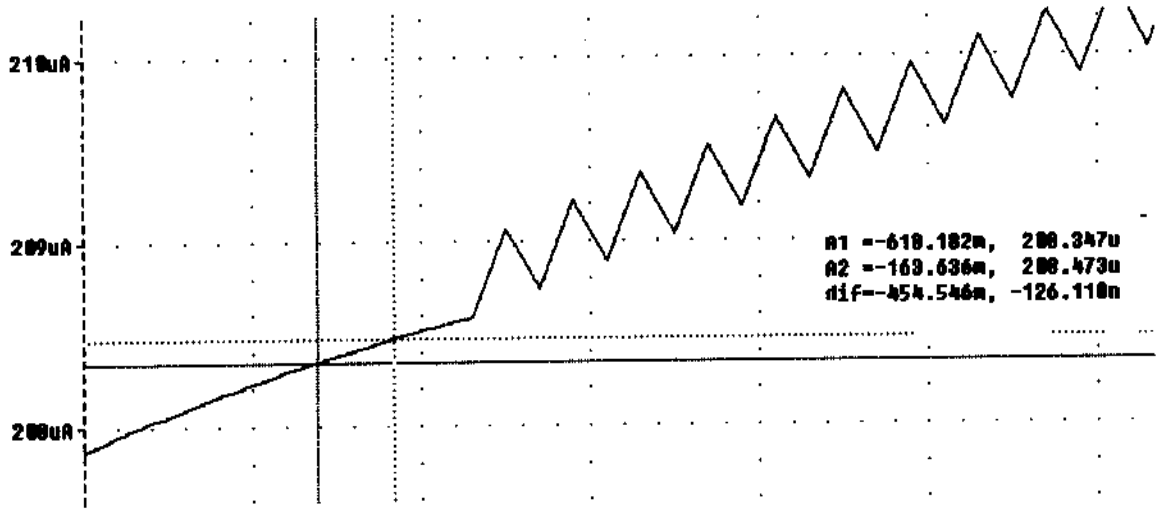
NAME	Q_Q1	Q_Q2
MODEL	Q2N3055	Q2N3055
IB	1.38E-04	1.16E-05
IC	4.85E-03	9.47E-05
VBE	5.78E-01	4.71E-01
VBC	0.00E+00	-9.42E+00
VCE	5.78E-01	9.89E+00
BETADC	3.51E+01	8.19E+00
GM	1.87E-01	3.66E-03
RPI	2.73E+02	4.07E+03
RX	1.00E-01	1.00E-01
RO	1.03E+04	6.27E+05
CBE	8.17E-09	9.22E-10
CBC	2.76E-10	1.16E-10
CJS	0.00E+00	0.00E+00
BETAAC	5.10E+01	1.49E+01
CBX	0.00E+00	0.00E+00
FT	3.53E+06	5.62E+05

Q.11 In order to enhance the output resistance of the Widlar mirror, the resistance R2 is replaced by a BJT device as shown below. Draw the ac equivalent circuit for the modifier current mirror. Label the circuit components clearly.



The output I-V characteristic is shown below. Determine the output resistance and compare with the value predicted by the theoretical formula.

You have to use the component values given in the output listing.



* Schematics Netlist *

```
Q_Q1        $N_0001 $N_0001 $N_0002 Q2N3055
V_V3        $N_0003 0 DC 5
V_V1        $N_0002 0 DC -5
I_I1        0 $N_0001 DC 5m
Q_Q2        $N_0003 $N_0001 $N_0004 Q2N3055
Q_Q3        $N_0004 $N_0005 $N_0002 Q2N3055
V_V4        $N_0005 0 DC -4.5
```

SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE	NODE	VOLTAGE
($N_0001)	-4.4225	($N_0002)	-5.0000				
($N_0003)	5.0000	($N_0004)	-4.9144				
($N_0005)	-4.5000						

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
V_V3	-2.105E-04
V_V1	5.235E-03
V_V4	-2.453E-05

TOTAL POWER DISSIPATION 2.71E-02 WATTS

_**** 01/03/104 10:33:30 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

NAME	Q_Q1	Q_Q2	Q_Q3
MODEL	Q2N3055	Q2N3055	Q2N3055
IB	1.38E-04	1.80E-05	2.45E-05
IC	4.84E-03	2.10E-04	2.29E-04
VBE	5.78E-01	4.92E-01	5.00E-01
VBC	0.00E+00	-9.42E+00	4.14E-01
VCE	5.78E-01	9.91E+00	8.56E-02
BETADC	3.51E+01	1.17E+01	9.32E+00
GM	1.87E-01	8.13E-03	8.95E-03
RPI	2.73E+02	2.55E+03	2.11E+03
RX	1.00E-01	1.00E-01	1.00E-01
RO	1.03E+04	2.82E+05	2.91E+03
CBE	8.16E-09	1.11E-09	1.16E-09
CBC	2.76E-10	1.16E-10	6.93E-10
CJS	0.00E+00	0.00E+00	0.00E+00
BETAAC	5.10E+01	2.07E+01	1.89E+01
CBX	0.00E+00	0.00E+00	0.00E+00
FT	3.53E+06	1.06E+06	7.69E+05

Q.12: By a mistake the bias voltage at the base of Q3 was altered from –4.5 V to –4.4 V. What effect will this have in the output resistance of the current mirror? The simulation output listing is attached below. Calculate the output resistance and compare it with the value found in Q.11 above. Discuss your results.

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) -4.4229 ($N_0002) -5.0000

($N_0003) 5.0000 ($N_0004) -4.9837

($N_0005) -4.4000

VOLTAGE SOURCE CURRENTS
NAME CURRENT

V_V3 -3.024E-03
V_V1 1.038E-02
V_V4 -2.352E-03

TOTAL POWER DISSIPATION 5.67E-02 WATTS

**** 01/03/104 10:51:17 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

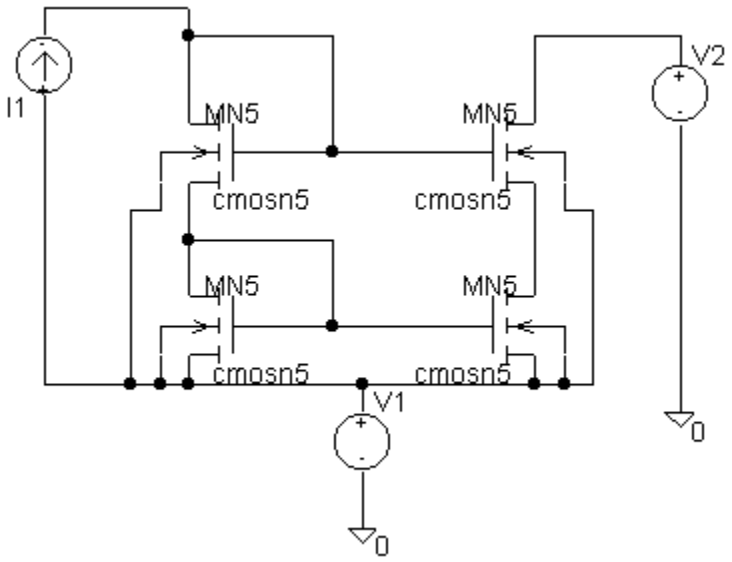
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

****

**** BIPOLAR JUNCTION TRANSISTORS

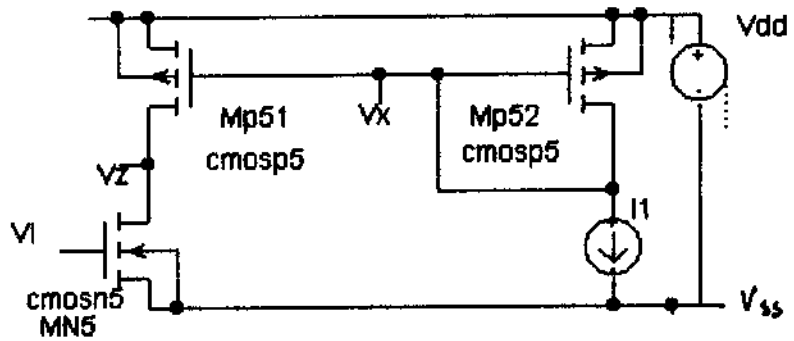
NAME	Q_Q1	Q_Q2	Q_Q3
MODEL	Q2N3055	Q2N3055	Q2N3055
IB	1.37E-04	8.97E-05	2.35E-03
IC	4.77E-03	3.02E-03	3.11E-03
VBE	5.77E-01	5.61E-01	6.00E-01
VBC	0.00E+00	-9.42E+00	5.84E-01
VCE	5.77E-01	9.98E+00	1.63E-02
BETADC	3.49E+01	3.37E+01	1.32E+00
GM	1.84E-01	1.17E-01	2.01E-01
RPI	2.76E+02	4.41E+02	1.38E+02
RX	1.00E-01	1.00E-01	1.00E-01
RO	1.05E+04	1.97E+04	4.24E+00
CBE	8.06E-09	5.41E-09	1.79E-08
CBC	2.76E-10	1.16E-10	2.33E-07
CJS	0.00E+00	0.00E+00	0.00E+00
BETAAC	5.08E+01	5.15E+01	2.78E+01
CBX	0.00E+00	0.00E+00	0.00E+00
FT	3.52E+06	3.37E+06	1.28E+05

Q.13: The schematic below presents a cascode current mirror using NMOS transistors.



Draw the ac equivalent circuit for the system and indicate in the circuit how you could determine the output resistance of the current mirror.

Q.14: Consider the NMOS amplifier with PMOS active load as shown below. Assume that the I-V equation is of the form $I(NMOS)= K_n(V_{GS}-V_{TN})^2(1+\lambda_n V_{DS})$ and $I(PMOS)=K_p(V_{SG}-|V_{TP}|)^2(1+\lambda_p V_{SD})$. Given $K_n=90\ \mu A/V^2$, $K_p=30\ \mu A/V^2$, $V_{TN}=1$ V, VTP= -1 V, $\lambda_n=0.01\ V^{-1}$, $\lambda_p=0.02\ V^{-1}$, $V_{dd}=10$ V, $V_{SS}=-3$V, and I1=200 μA, find the DC voltages at various nodes (i.e., V_x, V_z) of the system. Assume V_i =0 V. The PMS transistors are identical.



Q.15,16 : deleted

Q.17. In a MOS differential amplifier using current mirror load, the voltage gain is given by $g_m/(g_{dp}+g_{dn})$ where $g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DC}}$ for the amplifying device and $g_{dp} = \frac{1}{r_{op}}$, $g_{dn} = \frac{1}{r_{on}}$. The suffixes 'p', 'n' standing for PMOS and NMOS transistors.

Given $\mu C_{ox} = 100\ \mu A/V^2$, $I_{DC} = 100\ \mu A$, $V_{TN} = 1V$, $V_{AP} = 20V$, $V_{An} = 30V$.

Design the aspect ratio W/L of the amplifying transistors for a gain of 40.

Soln:

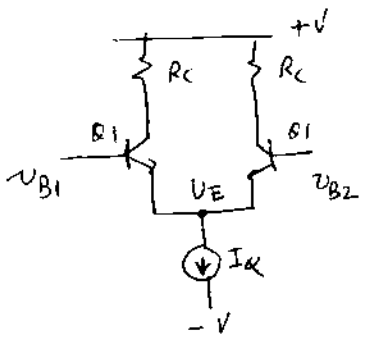
$$40 = \frac{g_m}{g_{dp}+g_{dn}}$$

$g = \frac{1}{r}$; $r = \frac{V_A}{I_{DC}}$

$$40 = \frac{\sqrt{2 \times 100 \times 10^{-6} \frac{W}{L} \times 100 \times 10^{-6}}}{100 \times 10^{-6}\left(\frac{1}{20}+\frac{1}{30}\right)}$$

Solving $\sqrt{\frac{2N}{L}} = \frac{10}{3}$; $\frac{W}{L} = \frac{50}{9}$

Q.18: For the BJT DA, find an expression for the common emitters node voltage v_E when the DA has two large signal (, input voltages v_{B1}, v_{B2}.



Ans: For large signal operation you use the exponential equation for the BE junctions of each transistor.

For Q_1, $i_{E1} = I_S e^{(v_{B1}-v_E)/nV_T} \simeq I_S e^{(v_{B1}-v_E)/V_T}$ assuming $n=1$

For Q_2, $i_{E2} = I_S e^{(v_{B2}-v_E)/V_T}$.

$V_T \rightarrow$ thermal voltage $= \frac{kT}{q}$

But by KCL at v_E node, $i_{E1} + i_{E2} = I_Q$

So $I_Q = I_S \cdot e^{\frac{v_{B1}-v_E}{V_T}} + I_S e^{\frac{v_{B2}-v_E}{V_T}}$, assuming identical transistors.

$$= I_S e^{-\frac{v_E}{V_T}} \cdot \left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)$$

So $$e^{-v_E/V_T} = \frac{I_Q}{I_S} \cdot \frac{1}{\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)}$$

Taking natural log on both sides

$$-\frac{v_E}{V_T} = \ln\left(\frac{I_Q}{I_S}\right) - \ln\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)$$

$$\text{or } v_E = V_T \left[\ln\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right) - \ln\left(\frac{I_Q}{I_S}\right)\right].$$

Q: What if $v_{B1} = \frac{v_d}{2}$; $v_{B2} = -\frac{v_d}{2}$? and v_d is very small } TRY YOURSELF!