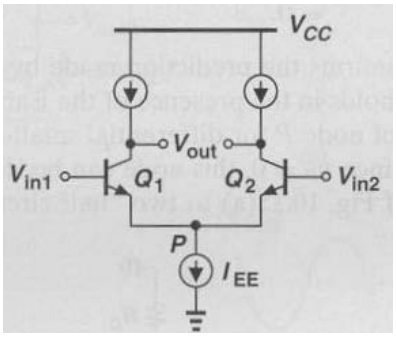
ELEC 312_Winter 2013 term

ELEC 312: ELECTRONICS – II ASSIGNMENT set 1

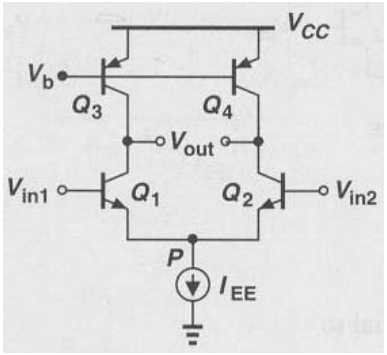
Department of Electrical and Computer Engineering

Winter 2013

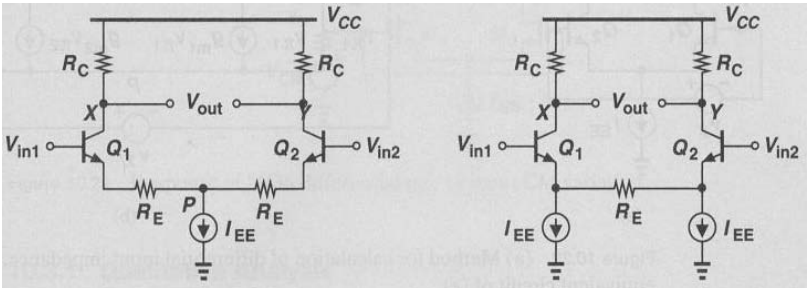
1. Find an expression for the differential gain of the following circuit, where ideal current sources are used as loads to maximize the gain. V_{in1}, V_{in2} may be assumed to be balanced differential signals.



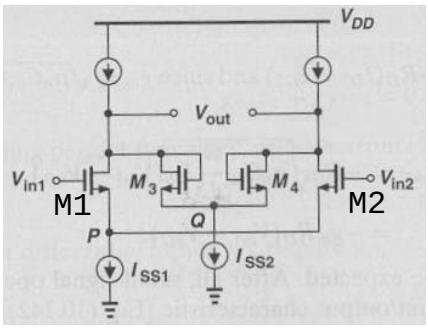
2. The following figure illustrates an implementation of a differential amplifier with active load using complementary BJT devices. Calculate the differential voltage gain $V_{out}/(V_{in1} - V_{in2})$.



3. Determine the gain of the emitter degenerated differential pairs shown in the following figure. Assume $V_A = \infty$.



4. Assuming $\lambda = 0$, compute the voltage gain of the following circuit. I_{SS2} is used to bias the transistors M_3,M_4. Consider all I-sources as ideal.



5. Consider the basic current mirror in Figure 5 built with the NMOS-transistors M1, M2. For both the transistors L=0.5 microns ,W/L =8, V_{THN} =0.5V, $\mu_n C_{oxn} = 300\,\mu A/V^2$ Further, V_{DD}=1.5V, and I_{REF} =100 μA.

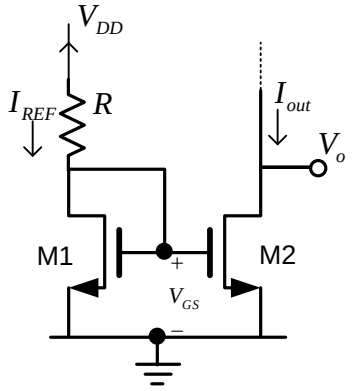


Figure 5

(i) Design *R* for I_{out} =100 μA.
(ii) What is the lowest value that could be allowed for V_o for proper operation of the system?
(iii) If the transistors have an *Early voltage* of 20V, what is the output resistance of the current source (i.e., at the location of I_{out})?
(iv) How much (as a %) will I_{out} change if V_o changes by $\pm 0.5V$?

6. Consider the basic current mirror (Figure 6) implemented using *npn*-BJT devices (Q1,Q2). Derive an expression for the current transfer ratio I_{out}/I_{in}. If β of the transistors has a minimum value of 50, what will be the largest current transfer ratio?

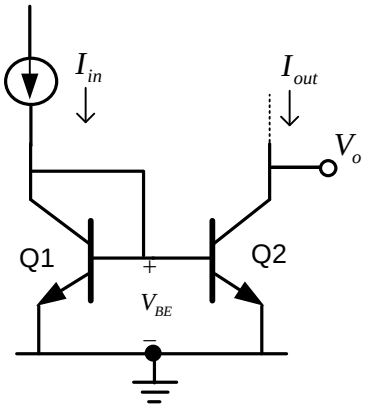


Figure 6

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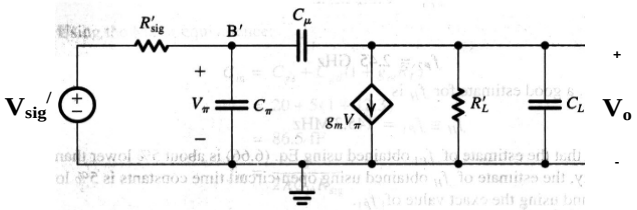
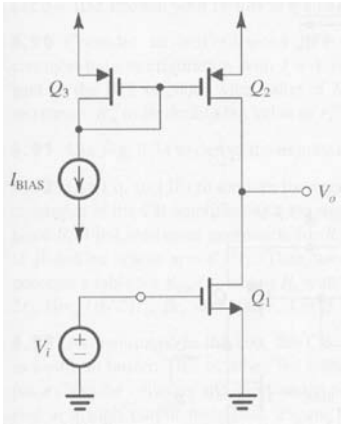
1. A common-emitter amplifier that can be represented by the following equivalent circuit, has $C_\pi = 10$ pF, $C_\mu = 0.5$ pF, $C_L = 2$ pF, $g_m = 20$ mA/V, $\beta = 100$, $r_x = 200$ Ω, $R_L' = 5$ kΩ and $R_{sig} = 1$ kΩ. Find (i) the mid band gain A_M, (ii) the frequency of the zero f_Z, and (iii) the approximate values of the pole frequencies f_{P1} and f_{P2}. Hence estimate the 3-dB frequency f_H. Note that R'_{sig} is the equivalent Thevenin resistance looking towards the signal source and includes the effects of R_{sig}, r_x and r_π. For approximate estimates, you may use OCTC method.



2. Analyze the high-frequency response of the CMOS amplifier shown below. The dc bias current is 100 μA. For Q_1, $\mu_n C_{ox} = 90$ μA/V^2, $V_A = 12.8$ V, W/L = 100 μm/1.6 μm, $C_{gs} = 0.2$ pF, $C_{gd} = 0.015$ pF. For Q_2, $C_{gd} = 0.015$ pF, $C_{gs} = 36$ fF and $|V_A| = 19.2$ V. Assume that the resistance of the input signal generator is negligibly small. Also, for simplicity assume that the signal voltage at the gate of Q_2 is zero. Find the low-frequency (i.e., at DC) gain, the frequency of the pole, and the frequency of the zero. You may use nodal analysis.

   Note: fF=10^{-15} F, pF=10^{-12} F.

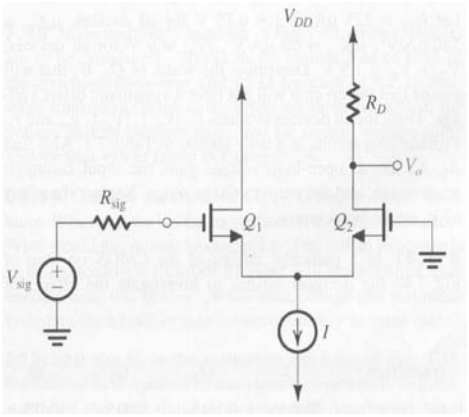


3. A CG amplifier is specified to have $C_{gs} = 2$ pF, $C_{gd} = 0.1$ pF, $C_L = 2$ pF, $g_m = 5$ mA/V, $\chi = 0.2$, $R_{sig} = 1$ kΩ and $R_L' = 20$ kΩ. Neglecting the effects of r_o, find the low-frequency gain v_o/v_{sig}, the frequencies of the poles f_{P1} and f_{P2} and hence an estimate of the 3-dB frequency f_H. For a CG amplifier you can use $g_{mb} = \chi g_m$. Use ac equivalent circuit.

4. (a) Consider a CS amplifier having C_{gd} = 0.2 pF, R_{sig} = R_L = 20 kΩ, g_m =5 mA/V, C_{gs} = 2 pF, C_L (including C_{db}) = 1 pF, and r_o = 20 kΩ. Find (i) the low-frequency gain A_M, and (ii) estimate f_H using open-circuit time constants.

   Hence determine the gain-bandwidth (GBW=mid-freq. gain *times* f_H).

5. Consider the following circuit for the case: I = 200 µA and V_{OV} = 0.25 V, R_{sig} = 200 kΩ, R_D = 50 kΩ, C_{gs} = C_{gd} = 1 Pf (for both transistors). Find the dc (i.e., low-frequency) gain, the high-frequency poles, and an estimate of f_H. (hint: need to find g_m from I and V_{OV} data!).



6: (a) Consider a CS stage having C_{gd} = 0.2 pF, R_{sig} = 20 kΩ, g_m =5 mA/V, C_{gs} = 2 pF, and r_o = 20 kΩ.

(b) A CG stage is connected in totem-pole configuration with the CS transistor in (a) to create a cascode amplifier. The ac parameters of this stage are identical with those of the CS stage. Regarding the body-effect in the CG stage assume χ = 0.2. Further R_L= 20 kΩ, and is shunted by a load capacitance C_L=1 pF.

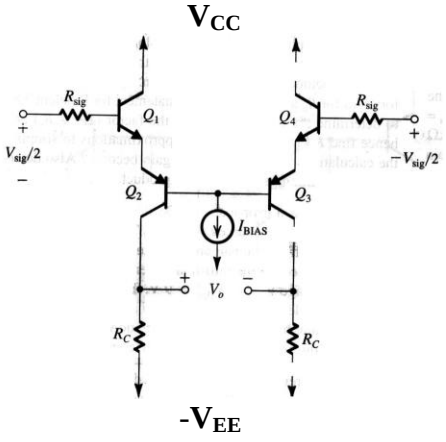
Show a schematic diagram of the system using NMOS transistors. Show the *ac* equivalent circuit.

Find (i) the low-frequency gain $A_{M,}$ and (ii) estimate the gain-bandwidth of the system. You may use OCTC method to determine the dominant high frequency pole f_H of the system.

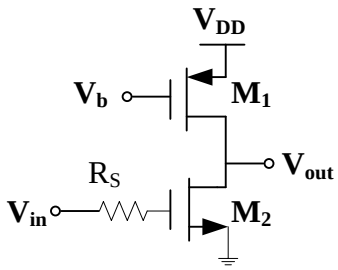
7: For the following circuit, let the bias be such that each transistor is operating at 100-μA collector current. Let the BJTs have h_{fe} = 200, f_T = 600 MHz, and C_μ = 0.2 pF, and neglect r_o and r_x. Also, $R_{sig} = R_C$ = 50 kΩ.

Show the *ac* equivalent circuit.

Find (i) the low-frequency gain, (ii) the high-frequency poles, and (iii) an estimate of the dominant high frequency pole f_H of the system. Now find the GBW (gain-bandwidth) of the system. You may use half-circuit technique.



8: In the following circuit assume both transistors operate in saturation and $\lambda \neq 0$. For each transistor you can assume the parasitic capacitances as C_{gsi}, C_{gdi}, (i=1,2).



Draw the *ac* equivalent circuit, analyze and derive the expression for the dominant pole frequency.

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ELEC 312: ELECTRONICS – II : ASSIGNMENT-set-3

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1. A series-series feedback circuit represented by Fig.1, transconductance amplifier operates with V_s = 100 mV, V_f = 95 mV, and I_o = 10 mA. What are the corresponding values of A and β? Include the correct units for each.

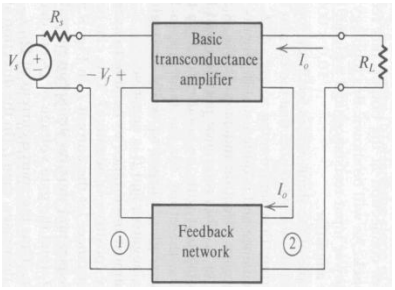

Figure 1:

2. For an amplifier connected in a negative feedback loop in which the output voltage is sampled (i.e., a shunt connection), measurement of the output resistance before and after the loop is connected shows a change by a factor of 80. Is the resistance with feedback higher or lower? What is the value of the loop gain Aβ? If R_{of} is 100 Ω, what is R_o without feedback?

3. The shunt-shunt feedback amplifier in the Figure 3 has I = 1 mA and V_{GS} = 0.8 V. The MOSFET has V_t = 0.6 V and V_A = 30 V. For R_S = 10 kΩ, R_1 =1MΩ, and R_2 = 4.7 MΩ, find the voltage gain v_o/v_s, the input resistance R_{in} and the output resistance R_{out}. You need to figure out the *ac* parameters for the MOS device.

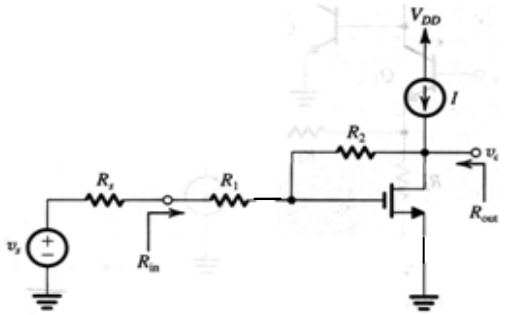

Figure 3:

4. An op amp having a low-frequency gain of 10^3 and a single-pole transfer function with -3dB frequency of 10^4 rad/s is connected in a negative feedback loop via a feedback network having a transmission $\beta(s)$ given by $\beta(s) = \frac{\beta_o}{(1 + s/10^4)^2}$. Find the value of β_o above which the closed-loop amplifier becomes unstable.

5. A DC amplifier has an open-loop gain of 1000 and two poles, a dominant one at 1 kHz and a high-frequency one whose location can be controlled. It is required to connect this amplifier in a negative feedback loop that provides a dc closed-loop gain of 100 and a maximally flat response. The transfer function of the amplifier can be modeled as:

$$A(s) = \frac{1000}{(1 + s/\omega_1)(1 + s/\omega_2)}$$

In the above ω_1 is the dominant pole frequency. It is required that under feedback, the amplifier will have a maximally flat response according to the model

$$A_f(s) = \frac{1000\omega_1\omega_2}{s^2 + (\omega_p / Q_p)s + \omega_p^2}$$, with Q_p=0.707.

Calculate the required ω_2.

ELEC 312: ELECTRONICS – II : ASSIGNMENT-set-4

Department of Electrical and Computer Engineering

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Q.1: Show the design of a class-A power amplifier using BJT devices, employed to deliver 10 W of ac signal power to a load of 10 ohms. Find the V_{CC} required, the I_Q required and design the active circuit to provide the required I_Q . Comment on the heat dissipation limits of the BJT devices used in your design.

Q.2: Design an idealized class-B output stage as shown in Figure 2, to deliver an average power of 25 W to an 8 Ω speaker. The peak output voltage must be no larger than 80% of supply voltages V_{CC}. Assume that the input signal is sinusoidal.
Determine: (i) the required value of V_{CC}, (ii) the peak current in each transistor, (iii) the average power dissipated in each transistor, and (iv) the power conversion efficiency.

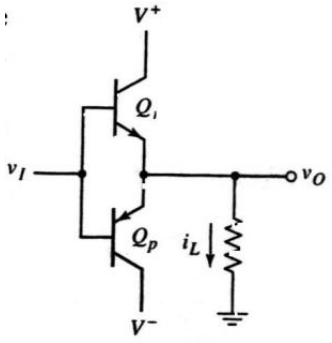

Figure 2: Basic class-B output stage

Q.3: Determine the required biasing in a MOSFET class-AB output stage. The circuit is shown in Figure 3. The parameters are V_{DD} = 10 V and R_L = 20 Ω. The transistors are matched, and the parameters are K = 0.20 A/V^2 and $|V_T|$ = 1 V. The quiescent drain current is to be 20% of the load current when v_o = 5 V.
The I-V equation for either transistor is: $I_D = K(V_{GS} - |V_T|)^2$

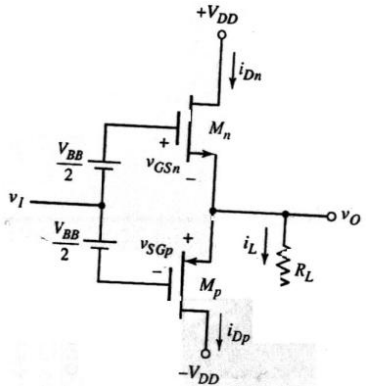

Figure 3: MOSFET class-AB output stage