# Appendix-I

(Electronics-I and Network Analysis Background)

## 1. BJT and MOS circuit calculations

1. DC calculations

1.1 For a dc bias current $I_E$ at the emitter of a BJT, the collector current is: $\alpha_{DC} I_E$.

1.2 For a dc bias current $I_E$ at the emitter of a BJT, the base current is: $I_E /(1+\beta_{DC})$.

1.3 The relationships between $\alpha$ and $\beta$ for DC calculations are: $\alpha_{DC} = \beta_{DC} /(1+\beta_{DC}); \beta_{DC} = \alpha_{DC} /(1-\alpha_{DC})$.

1.4 A resistance $R_E$ connected between the emitter node and *ac* ground appears as a resistance $R_E(1+\beta_{DC})$ at the base node.

1.5 A resitance $R_B$ connected between the base node and *ac* ground appears as a resistance $R_B /(1+\beta_{DC})$ at the emitter node.

1.6 Either of 1.4 or 1.5 can be used to carry out DC circuit calculations with reference to the base side and emitter side respectively.

1.7 For DC and large signal (i.e., in digital circuits) calculations, the EB junction behaves like a constant battery. If a value is not given, you can assume this to be 0.7 volts. For NPN, the voltage is $V_{BE}$ while for PNP it is $V_{EB}$.

1.8 For an enhancement type MOSFET (E-MOS) with N-channel, the DC current formulae are:

$$V_{GS} < V_{THN},\ I_{DS} \cong 0 \text{ (sub-threshold region)}$$

$$V_{GS} > V_{THN}, \text{ and } V_{DS} < V_{GS} - V_{THN},\quad I_{DS} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{THN})V_{DS} - \frac{V_{DS}^2}{2}] \text{ (linear region)}$$

$$V_{GS} > V_{THN}, \text{ and } V_{DS} \geq V_{GS} - V_{THN},\quad I_{DS} = \mu_n C_{ox} \frac{W}{2L}[(V_{GS} - V_{THN})^2(1+\lambda_n V_{DS})] \text{ (saturation region)}$$

>=

1.9 For a P- channel E-MOS, the formulae become (note the changes in the symbols!):

$V_{SG} < |V_{THP}|, I_{SD} \cong 0$ (sub-threshold region)

$V_{SG} > |V_{THP}|$, and $V_{SD} < V_{SG} - |V_{THP}|$, $I_{SD} = \mu_p C_{ox} \frac{W}{L}[(V_{SG} - |V_{THP}|)V_{SD} - \frac{V_{SD}^2}{2}]$ (linear region)

$V_{SG} > |V_{THP}|$, and $V_{SD} \geq V_{SG} - |V_{THP}|$, $I_{SD} = \mu_p C_{ox} \frac{W}{2L}[(V_{SG} - |V_{THP}|)^2(1 + \lambda_p V_{SD})]$ (saturation region)

>=

2. AC (i.e., small signal) calculations

2.1 A DC current $I_C$ at the collector produces an ac equivalent circuit with a transconductance $g_m = I_c / V_T$, where $V_T$ is the thermal voltage kT/q. Unless given otherwise, assume $V_T$ = 25 mV at room temperature (300° Kelvin).

2.2 A DC current $I_E$ at the emitter produces a resistance of $r_e = V_T / I_E$, in the ac equivalent circuit of the BJT. Unless given otherwise, assume $r_e$ = 25mV/$I_E$ at room temperature (300° Kelvin).

2.3 Since $I_C = \alpha_{ac} I_E$, it follows that $g_m = \alpha_{ac} / r_e$. For quick and approximate calculations you can assume that $g_m = 1 / r_e$.

2.4 For ac components of the BJT in CE mode of operation, $i_c = h_{fe}\, i_b$, $i_e = (h_{fe} + 1) i_b$, where $h_{fe}$ is the ac current gain in CE mode of operation. Similarly, for CB mode of ac operation $\alpha_{ac} = h_{fb} = h_{fe} / (1 + h_{fe})$.

2.5 For small (ac) signals (i.e., ≤$V_T$ /10), the BJT base-emitter junction behaves like a diode with an ac resistance of $r_e$ at the emitter node. Looking from base node this transforms into a resistance of $r_e$ ($h_{fe}$ +1). This is the famous reflection rule for CE BJT amplifier.**

2.6 An extension of the reflection rule is : if $R_E$ is the total resistance from the emitter lead to ground (ac voltage =0), the equivalent resistance by looking at the base node will be $R_E(h_{fe} + 1)$. On the other hand if there is an ac equivalent resistance $R_B$ connected between the base and ac ground, the resistance that appears across these two terminals is $R_B/(h_{fe}+1)$. This is the inverse reflection rule.

2.7 The rules as above arise because for same signal voltage across the base-emitter junction, there is a difference in the values of signal currents in the base with that at the emitter. The factor is ($h_{fe}$ +1). Continuity of voltage and current through the EB junction is maintained if this scaling factor is used to scale up (or down) the respective resistances.**

2.8 The reflection rule applies equally well for impedances connected at the emitter or at the base terminal.**

2.9 Because of the reflection rule, the ac resistance of the intrinsic transistor, when looked from the base side becomes ($h_{fe}$ +1) $r_e = r_\pi$.**

** The above cases (2.5-2.9) can be applied as a rule of thumb only if $r_o$ is infinite (i.e., $V_A$ = infinity, or unspecified). For finite value of $r_o$, the rule is applicable if one end of $r_o$ is *grounded for ac signals.*

2.10 How to figure out if to use $r_e$ or $r_\pi$ in the equivalent circuit? If, while following the path of signal flow (from the signal source end), you encounter the E-terminal of the BJT before the B-terminal, you will use $r_e$ . But if you meet with the B-terminal before the E-terminal, you will use $r_\pi$ . Another clue is: for CE and CC amplifier you will use $r_\pi$ and for CB amplifier you will use $r_e$ .

2.11 $V_A$ is the early voltage for the transistor, the output resistance of the intrinsic device (BJT or MOS) is $r_o$ ($r_{ds}$ for MOS) = $V_A$ / $I_{DC}$ , where $I_{DC}$ is the DC bias current value at the collector (drain for MOS) of the transistor.

2.12 An E- MOS transistor, when operating in saturation region, has the ac transconductance $g_m$ : $\sqrt{2\mu C_{ox}(W/L)I_{DC}}$

2.13 An E- MOS transistor, operating in the linear region, has an output resistance of: $[\mu C_{ox}(W/L)(V_{GS}-V_{THN})]^{-1}$; for PMOS use $V_{SG}$, and $|V_{THP}|$.

The informations above will be useful to draw the ac equivalent circuit for a transistor and to perform quick and simple hand calculations regarding certain charcteristics of the transistor amplifier.

## Appendix-II: Linear Network Analysis Fundamentals

The time domain integro-differential equations for linear networks (i.e., networks containing linear circuit elements like R,L and C, linear controlled sources such as VCVS,VCCS,CCCS and CCVS) can be arranged in a matrix form:

$$w(p)\, x(t) = f(t)$$

where, w(p) is an impedance/admittance matrix operator containing integro-differential elements ( x(t) is the current/voltage variables (vectors) in the edges of the network graph and f(t) are the source voltage/current variables (vectors). The p-operator implies $p = d/dt$ and $1/p = dt$. On taking Laplace transform of both sides, one could derive

$$W(s)\, X(s) = F(s) + h(s)$$

where h(s) contain the contributions due to *initial values.*On inserting $s = j\omega$ one can get the *Frequency Domain* characterization of the system. The above sequence of operation, is, however, rather lengthy and impractical. A more efficient technique is to characterize each network component (R,L and C) in s-domain including the contribution of initial conditions and formulate the network equations as was done before. Impedance elements so expressed are *transformed impedances* and the network becomes a *transformed network.*

**2.1** Transformed Impedances

The transformed impedances are impedance elements referred to a transform (i.e., Lapalce Transform) domain. Characterizations for transformed basic network elements are discussed below. For ideal voltage or current sources the transformed quantities are simply the Lapalce transforms (e.g., $V_g(s)$, $I_g(s)$). For the i-v relation across a resistor, one can write either $V_R(s)=I_R(s)R$ or the dual $I_R(s)=V_R(s)/R$. Thus there are two characterizations (viz., an I-mode and a V-mode) for each element. The particular choice depends upon which of I(s) and V(s) is the independent variable. In *loop analysis, the I(s) becomes independent variable* and the voltage and impedance around the loop are recorded as part of the systematic procedure to obtain the matrix formulation (for example, by inspection). In this case the series equivalent model of the transformed impedance has to be used.The cases of interest are shown in Figures 1.1(a)-(b) and 1.2 (a)-(b) for the inductance and capacitance respectively.

For an inductance, the v - i relations

$$v_L(t) = L\frac{di_L}{dt}, \text{ and } i_L(t) = \frac{1}{L}\int_0^t v_L(t)dt + i_L(0\_),$$

lead to the s - domain equations :

$V_L(s) = sLi_L(s) - Li_L(0\_)$ and,

$I_L(s) = \frac{V_L(s)}{sL} + \frac{i_L(0\_)}{s}$. These lead to the two equivalent networks shown on right. Figure(a) is the series representation and Figure(b) is the shunt representation.

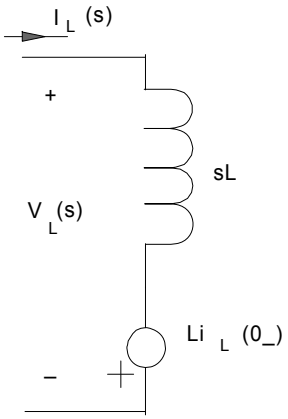


Figure 1.1(a)

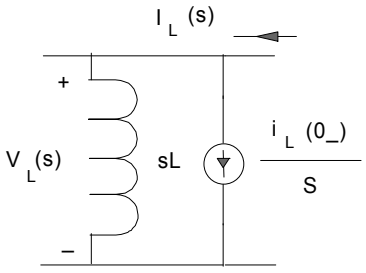


Figure 1.1(b)

Similarly, the capacitance current $i_c = C\frac{dv_c}{dt}$, and

$v_c = \frac{1}{C}\int_0^t i_c dt + v_c(0\_)$, lead to the s - domain equations :

$I_c(s) = sCV_c(s) - Cv_c(0\_)$, and $V_c(s) = \frac{I_c(s)}{sC} + \frac{v_c(0\_)}{s}$.

These lead to the two network representations shown to the right. Figure (a) is the series representation, while Figure (b) is the shunt representation.

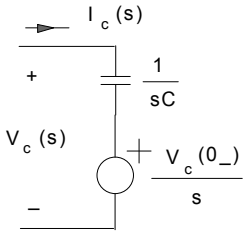


Figure 1.2(a)

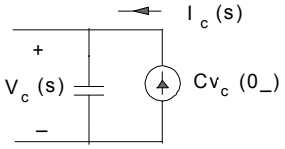


Figure 1.2(b)

In *nodal analysis*, where the node voltage becomes independent variable, the shunt architecture are to be used for the transformed impedances.

A network containing transformed impedances is referred to as transformed network.

## Appendix-III: Network analysis technique

### 3.1 Nodal analysis

In *nodal analysis, a voltage source in series with an element should be transformed into a current source with a shunt element* by employing source transformation (i.e., Thevenin to Norton equivalent). This will reduce the number of nodes and also make *the analysis more homogeneous in that we have to deal with only node voltages and current sources (independent, dependent)* which are the principal variables in nodal analysis. It may be recalled that the nodal system of equations is represented by the matrix equation Y(s)V(s) = J(s), where Y(s) is the admittance matrix, V(s) is the node voltage vector (i.e., a column matrix) and J(s) is the current source vector.

If a voltage source feeds more than one unique impedance in a parallel connetion, E-shift technique [1]is to be used before embarking on the source transformation operation. The given network has to be converted to a network with transformed impedances with shunt model representation for inductances and capacitances.

Steps to setup the matrix equation for Nodal Analysis

Step 1: **Identification of the sources:** identify all dependent and independent sources. These are to be included initially as elements of the vector J(s).

Step 2: **Set up the matrix elements**

(a) $y_{ii}$ elements are *sum* of admittances (conductances) meeting at the node. This is the *self admittance*.

(b) $y_{ij}$ elements are *negative* of the admittances running between the node pair (i,j). This is *trans admittance.*

The above two sets are to be included in the Y(s) part of the matrix equation Y(s)V(s) = J(s).

(c) $j_{nk}$ element is the sum of current sources meeting at $k^{th}$ node, taken *positive if towards and negative when away* from the node. These are to be included in the J(s) part of the matrix equation Y(s)V(s) = J(s)

Step 3: **In** J(s) **decode the dependent I-sources** in terms of the node (voltage) variables i.e., elements of V(s).

Step 4: **Transpose** the quantities obtained in step 3 to the other side and allocate them to appropriate locations in the Y(s) matrix.

The above four steps complete the setting up of the node system of matrix equation in the form Y(s)V(s) = J(s).

[1]Linear Networks and Systems, 2nd edition, vol.1, by Dr. Wai-Kai Chen.

## 3.2 Loop analysis

The *first thing is to draw the equivalent circuit* with transformed impedances using series model versions for inductors and capacitances. Further, all current sources are to be converted to equivalent voltage sources with series impedances using source transformation (i.e., Norton to Thevenin). If a current source exists with no unique impedance in parallel, I-shift technique is to be used before applying source transformation. It may be recalled that the loop system matrix equation has the form Z(s)I(s) = E(s), where Z(s) is the impedance matrix, I(s) is the loop current vector and E(s) is the loop voltage vector.

Steps to setup the matrix equation for Loop Analysis

Step 1 **(Identification of sources):** look up all voltage sources (independentn and dependent) to be initially included as elements of the E(s) vector.

Step 2 **(Identify the loop impedance matrix operator elements and loop voltage source vector)**

(a) *self loop impedance* $z_{ii}$ is the sum of all impedances in the loop i.

(b) *mutual loop impedance* $z_{ij}$ is the impedance shared by loop i and loop j. If currents in loops i and j are in the same direction $z_{ij}$ is taken with a positive sign. On the other hand, if the currents in loops i and j are in opposite directions, it is taken with a negative sign.

( c) *loop source vector* $e_l$ is the algebraic sum of all the voltage sources in loop i. The components are taken with a positive sign if a *potential rise* occurs in the direction of the loop current. If a *potential drop* takes place in the direction of the loop current, the voltage element is taken with a negative sign. We tus have the preliminary form Z(s)I(s) = E(s).

Step 3 **In** E(s) found above and **express the dependent sources** in terms of the loop current variables (i.e.,elements of I(s)).

Step 4 **Transpose the dependent components** of E(s) on the other side and allocate the associated coefficiens to proper location of the Z(s) matrix.

The above four steps will produce the final matrix equation form Z(s)I(s) = E(s) for loop analysis.

## 3.3 Network Functions

If we study the relationships developed in connection with nodal and loop analysis, we can discover a general format, i.e., W(s) X(s) = F(s) + h(s), where W(s) can be either an admittance or an impedance matrix, X(s) can be nodal voltage vector or loop current vector, F(s) the vector of independent sources and h(s) the vector of initial conditions. Using this equation ,one can

easily arrive at: $X(s) = W^{-1}(s)F(s) + W^{-1}(s)h(s)$. The FIRST part of the solution on the RHS is the complete solution if initial values were zero (so h(s)=0). This is called **zero (initial) -state response.** The SECOND part of the solution on the RHS is the complete solution if the forcing functions were zero (so F(s)= 0). This is known as **zero -input or natural response.**

*A network function is defined with regard to zero-state response in a network when there is **only one independant voltage/current (driving function) forcing function** in the network.*. It is the ratio of the *Lapalce- transform of the zero-state response at a given point (node) in a network to the Lapalce- transform of the input (or another zero-state response) effective at another location of the network.*

Depending upon the location of the pair of points there are two nomenclatures. If *the pair of points are same,* we talk about **driving point impedance or driving point admittance.** If the *pair of points are separate,* we can derive (i) **transfer function in voltage, (ii) transfer function in current, (iii) transfer impedance and (iv) transfer admittance**

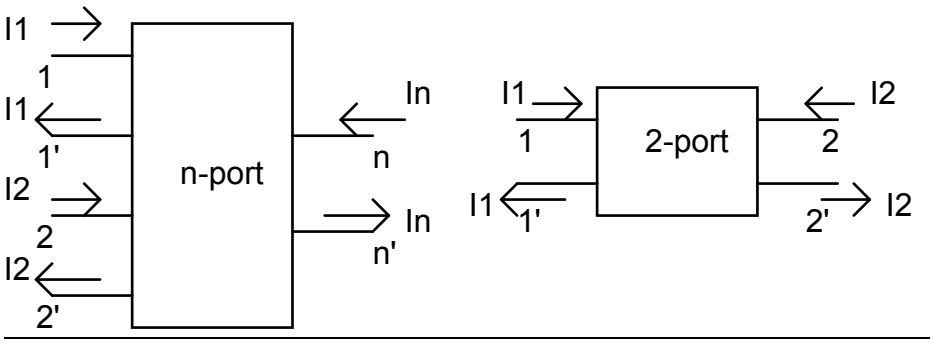
## 3.4 Characteristics of Network functions

It is well-known that Laplace transform of time-domain integro-differential equations are algebraic functions in the variable s, which is regraded as *complex frequency* i.e., $s = \sigma + j\omega$. When we set $\sigma = 0$, the resulting algebraic function (i.e., $s=j\omega$.) represents a frequency domain function. The network functions are thus rational algebraic functions of s . The parameter $\sigma$ relates to damping (or growth) of the time domain response while $\omega$ gives the frequency of the time-domain waveform.

When $\sigma > 0$, the system becomes unstable (time domain response grows) and when $\sigma << \omega$, the system exhibits frequency selectivity. For a self oscillatory network $\sigma <= 0$. For certain values of s, the network function ->0. These values (of s ) are the 'zeros' of the network function. Similarly, for some values of s, the network function -> $\infty$. These values (of s ) are called the 'poles' of the network function**.**

## 3.5 Two-port Networks

A **node pair**, such that current entering one node is exactly equal to the current exiting out of the other node constitute a **one-port**. If there is another node pair with the same property, we have another one-port. If the *node pairs belong to the same system, we have a two-port network system.* As an illustration, consider the following diagram. The concept of an n-port can also be developed similarly.




It is possible that the nodes 1',2' ... n' are one and the same node (i.e., ground). In 2-port network theory we consider only the external node pairs. The system is considered as a black box with no independent current/voltage source(s) residing inside the black box. Also all initial conditions are assumed to be zero (or taken care of by proper analysis prior to characterization as a 2-port network). The electrical characteristics of the two port is entirely defined in terms of the voltage/current source(s) effective at the external terminals of the (black box) network. Thus *the two port network theory can be very conveniently applied to fairly large sized networks.* There are several ways in which one can select a pair of independent voltage/current variables from the set V1, I1, V2 and I2. Thus we come across (i) *Short circuit* admittance parameters characterization, (ii) *Open circuit* impedance parameters .. , (iii) Hybrid parameters , and (iv) g-parameters.

### 3.5.1 Admittance Parameters

The characterization is best described by the matrix equation

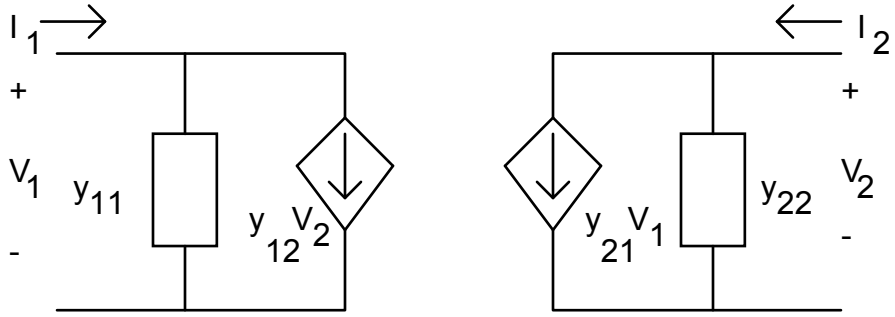
$$[Y][V] = [I]$$

The above corresponds to the set of linear equations

$y_{11}V_1 + y_{12}V_2 = I_1$ ; $y_{21}V_1 + y_{22}V_2 = I_2$ . The defining equations for the parameters are:

$y_{11} = [I_1 / V_1]_{V2=0}$, $y_{12} = [I_1 / V_2]_{v1=0}$ , and so on.

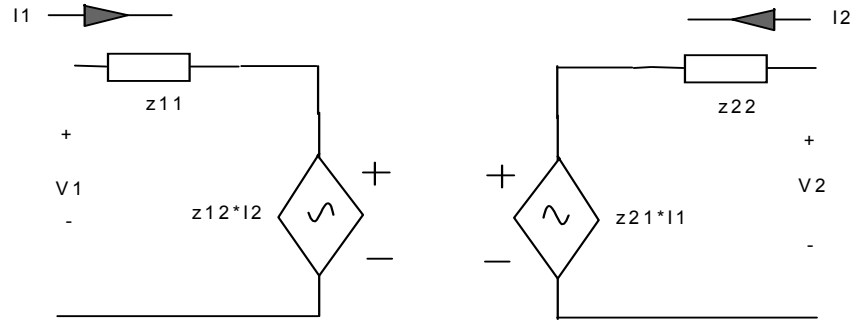
The electrical *network model (i.e., equivalent to the network inside the black box)* for the above set of equations is:



### 3.5.2 Impedance Parameters

Here the matrix relation is as **[Z] [I] = [V].** The set of equations are:

$z_{11} I_1 + z_{12} I_2 = V_1$ ; $z_{21} I_1 + z_{22} I_2 = V_2$. The network model is:

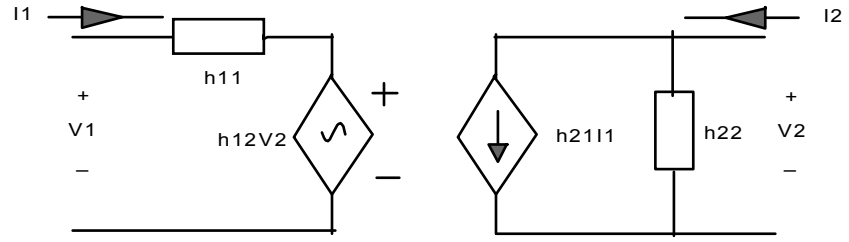



One can use the above relations to derive $z_{11} = (V_1 / I_1)$ with $I_2 = 0$, i.e., port 2 open, $z_{12} = (V_1/I_2)$ with $I_1 = 0$ and so on.

### 3.5.3 Hybrid (h-) Parameters

In this $V_1$ is related to $I_1$ (impedance) and $V_2$ (transfer ratio) while $I_2$ is related to $I_1$ (transfer ratio) and $V_2$ (conductance). That is why the name hybrid. It became popular to model transistor devices as a two port network. The system of equations are:

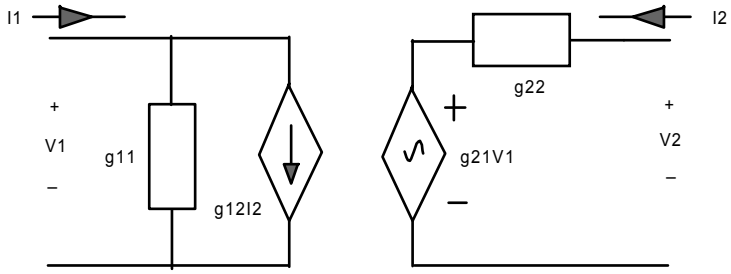
$h_{11} I_1 + h_{12} V_2 = V_1$ ; $h_{21} I_1 + h_{22} V_2 = I_2$ . Thus $h_{11} = (V_1/I_1)$ with $V_2 = 0$, i.e., port 2 short circuited, $h_{12} = (V_1/V_2)$ with $I_1 = 0$, i.e., port 1 open, and so on. The network model is:




### 3.5.4 Hybrid (g-) Parameters

Here the choice of variables are reversed compared with the h-parameter system. Thus $I_1$ and $V_2$ are related to $V_1$ and $I_2$. The system equations are:

$g_{11} V_1 + g_{12} I_2 = I_1$ ; $g_{21} V_1 + g_{22} I_2 = V_2$. Thus $g_{11} = (I_1 / V_1)$ with $I_2 = 0$, $g_{12} = (I_1/I_2)$ with $V_1 = 0$, and so on. The network model is:


I1
+
V1
–
g11
g12I2
g22
+
g21V1
–
+
V2
–
I2

## Appendix-IV: Interconnection of Two-port Networks

Various kinds of interconnection are possible between two *two ports*. The principle in obtaining the overall 2-port parameters involve (i) writing down the parameters for the individual 2-ports, (ii) identify the effect of the interconnection on the terminal variables which are being interconnected (they become identical, add up ... etc), (iii) re-write the new set of terminal variables according to the interconnection.

### 4.1 Parallel connection

In this connection, the terminal voltage pairs remain identical so that the currents at each port get added up because of the interconnection. Y parameter representation is the most preferred choice to begin with. *The overall Y-parameters is the sum of the constituent Y-parameters.* Thus, $[Y] = [Y]_a + [Y]_b$ , where networks $N_a$ and $N_b$ are connected in parallel at the input and at the output.

### 4.2 Series connection

Terminal currents remain same (series) so that the terminal voltage variables add up. Z parameter representation is the preferred choice. *The overall Z-parameter is the sum of the constituent Z-parameters.*Thus, $[Z] = [Z]_a + [Z]_b$ where $N_a$ and $N_b$ are the networks connected in series both at the input and at the output.

### 4.3 Series (input)- Parallel (output) connection

As the name suggest, the input ports (i.e., port #1) are connected in series while the output ports (#2) are connected in parallel. Thus at port#1 we will have $I_1=I_{1a}=I_{1b}$, but $V_1=V_{1a}+V_{2a}$, while at port#2 we get $I_2=I_{2a}+I_{2b}$, and $V_2=V_{2a}=V_{2b}$. Since $V_1$ and $I_2$ needs recalculation, it will be most profitable to start with the h-parameters. The overall H parameter matrix becomes equal to the sum of the component h-parameter matrices. Thus,

$$[H] = [H]_a + [H]_b$$

### 4.4 Parallel (input)- Series (output) connection

As the name suggest, the input ports (i.e., port #1) are connected in parallel while the output ports (#2) are connected in series. Thus at port#1 we will have $V_1=V_{1a}=V_{1b}$, but $I_1=I_{1a}+I_{2a}$, while at port#2 we get $V_2=V_{2a}+V_{2b}$, and $I_2=I_{2a}=I_{2b}$. Since $I_1$ and $V_2$ needs recalculation, it will be most profitable to start with the g-parameters. The overall G parameter matrix is given by:

$$[G] = [G]_a + [G]_b$$

## Appendix-V: Transfer Function and BODE Plot

In the above, the concept of a transfer function has been presented. It is a function of the variable s which is associated with the notion of a complex frequency in electronic circuits and systems. Let us designate this with the symbol T(s). Since T(s) is function of a complex variable (i.e., of s), it can have a magnitude and a phase angle. Bode plot involves plotting the functions 20log |T(s)| and /___T(s) as a function of frequency. Let us consider some simple concepts.

### 5.1 T(s) = Ks, where K is a constant.

For frequency domain analysis, we shall set s= jω. Thus, 20log |T(s)| = 20log (K) +20log (ω) =M(ω), say, and /____T(s) = arctan (ω/0) = 90 degrees. Since K is a constant, 20log (K) will be a constant. So far frequency dependence is concerned, M(ω) will be influenced by the term 20log (ω). As ω increases, M(ω) will increase linearly, beginning from negative infinity at ω =0. When ω =2, , M(ω) = 6dB, when ω =10, M(ω) = 20dB and so on. In another way, one can say that if there are two frequencies $\omega_1$ and $\omega_2$ , M($\omega_2$ ) will be 6 dB higher than M($\omega_1$ ) if $\omega_2 = 2\ \omega_1$ and M($\omega_2$ ) will be 20 dB higher than M($\omega_1$ ) if $\omega_2 = 10\omega_1$. These concepts are spelled out using the phrases: M(ω) changes at a rate of 6 db/octave (ratio =2), or M(ω) changes at a rate of 20 db/decade (ratio =10).

Thus the Bode plot of T(s)= Ks have the characteristics (a) the magnitude part *increases* at a rate of 6db/octave (or 20dB/decade), linearly with a positive slope and (b) the phase part is constant at 90 degrees.

### 5.2 T(s) = K/s.

Now M(ω)= 20log |T(s)| = 20log (K) - 20log (ω) and and /____T(s) = - arctan (ω/0) =- 90 degrees. Following the concept above, one can conclude that the Bode plot of T(s) has a phase angle of –90 degrees and a magnitude which *decreases* linearly at a rate of 6 dB/octave (or 20 dB/decade).

### 5.3 T(s) = K(s+a).

Now the phase angle = arctan (ω/a) and dB magnitude M(ω) = 20log (K) + 20log[ $(\omega^2 + a^2)^{1/2}$ ]= 20log (K) + 10log ($\omega^2 + a^2$ ). When ω is very small compared with a, M(ω) has a nearly constant value ~ 20 log(K) + 20log(a) dB, increasing slowly with increasing ω. When ω = a, M(ω) = 20log (K) + 20log $(2a^2)^{1/2}$, i.e., , M(ω) = 20log (K) + 20log (a ) + 20log $(2)^{1/2}$ =20log (K) + 20log (a ) + 3 dB. This is a distinct value. Thus the magnitude of T(s) has a Bode plot which is nearly a constant at small values of ω, increases slowly with ω and becomes 3 dB higher as ω becomes equal to a. Now from the concpet of poles and zeros, it is clear that T(s) has a zero at a. The values of M(ω) when ω has critical values of zero or infinity, are usually referred to as asymptotic values. Thus,

one can summarize that *when T(s) has a zero at (say) ω =a, the Bode magnitude plot of T(s) increases by 3 dB at ω =a compared to its asysmptotic value at ω =0.* As ω passes through a and becomes very large compared with a, the function T(s) approximates to T(s) ~ K(s) and hence behaves in the same manner as in case 1 above. Thus *as ω becomes very hgh compared with the zero of T(s),i.e., a, the magnitude plot changes linearly with ω approacing asymptotically a straight line of slope +6dB/octave (or 20dB/decade) erected at the frequency ω =a.* Further, as the phase angle is arctan (ω/a), it is nearly zero for small values of ω and increases slowly with ω. At ω=a, since arctan (a/a) =1, the phase angle is 45 degrees. *Thus at the zero of T(s) the phase angle is +45$^o$ relative to its previous asysmptotic value.* As ω becomes very high compared to a, the phase angle tends towards 90 degrees since arctan (infinity) is 90 degrees (i.e., tan (90$^o$) is infinity).

### 5.4 T(s)= K/(s+a).

Now the phase angle = 0 -arctan (ω/a) and dB magnitude M(ω) = 20log (K) -20log[ $(\omega^2 + a^2)^{1/2}$ ]= 20log (K) - 10log ($\omega^2 + a^2$ ). When ω is very small compared with a, M(ω) has a nearly constant value ~ 20 log(K) - 20log(a) dB, and it decreases slowly with increasing ω. When ω = a, M(ω) = 20log (K) - 20log $(2a^2)^{1/2}$, i.e., , M(ω) = 20log (K) - 20log (a ) - 20log $(2)^{1/2}$ =20log (K) +-20log (a ) - 3 dB. This is a distinct value. Thus the magnitude of T(s) has a Bode plot which is nearly a constant at small values of ω, decreases slowly with ω and becomes 3 dB lower as ω becomes equal to a. Now from the concpet of poles and zeros, it is clear that T(s) has a pole at a. Thus, one can say that *when T(s) has a pole at (say) ω =a, the Bode magnitude plot of T(s) decreases by 3 dB at ω =a compared to its asysmptotic value at ω =0.* As ω passes through a and becomes very large compared with a, the function T(s) approximates to T(s) ~ K/s and hence behaves in the same manner as in case 2 above. Thus *as ω becomes very high compared with the pole of T(s),i.e., a, the magnitude plot changes linearly with ω approacing asymptotically a straight line of slope -6dB/octave (or 20dB/decade) erected at the frequency ω =a.* Further, as the phase angle is - arctan (ω/a), it is nearly zero for small values of ω and decreases slowly with ω. At ω=a, since - - arctan (a/a) =-1, the phase angle is -45 degrees. *Thus at the pole of T(s) the phase angle is -45$^o$ relative to its previous asymptotic value.* As ω becomes very high compared to a, the phase angle tends towards - 90 degrees since - arctan (infinity) is - 90 degrees.

### 5.5 T(s)= K(s+$wz_1$)(s+$wz_{2)\ldots\ldots}$(s+$wz_m$)/[(s+$wp_1$)(s+$wp_2$)…(s+$wp_n$)]

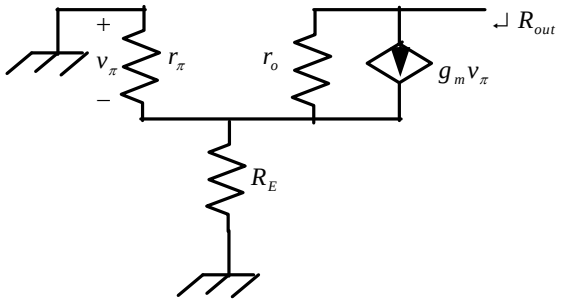
Now we have a general case where the transfer function has a number of zeros and a number of poles. After taking logarithms, one can derive M(ω) = 20log(K) + 10log($\omega^2 + wz_1^2$) + 10log($\omega^2 + wz_2^2$) + … +10log($\omega^2 + wz_m^2$) –10log($\omega^2 + wp_1^2$) - 10log($\omega^2 + wp_2^2$) -….- 10log($\omega^2 + wp_n^2$). Similarly, the phase angle will be Φ = artctan (ω/$wz_1$) + artctan (ω/$wz_2$)+.. + artctan (ω/$wz_m$) - artctan (ω/$wp_1$) - artctan (ω/$wp_2$)- ..- artctan (ω/$wp_n$). We can now apply the knowledge learned in

items 3 and 4 above like the principle of superposition at each zero and at each pole in accordance with their order of numerical values. Thus so far the magnitude (in dB) plot is concerned, M(ω) will start off with a constant value of $20\log(K) + 20\log(wz_1) + 20\log(wz_2) + \ldots +20\log(wz_m) - 20\log(wp_1) - 20\log(wp_2) - \ldots - 20\log(wp_n)$. This is the asymptotic value at ω = 0. *As ω increases, at each zero of T(s) the magnitude response changes by +3dB relative to the previous asysmptotic value and at each pole of T(s), the response changes by –3dB relative to the previous asysmptotic value*. Between two susccessive critical points (i.e., zero or pole), the plot tends to follow a straight line of slope +6dB per octave (+20dB per decade) if the current critical point is a zero of T(s). If the current critical point is a pole of T(s), the magnitude plot tends to folow a straight line of slope - 6dB per octave (-20dB per decade*). For a succession of zeros and poles of T(s), the values are to be added up successively.*

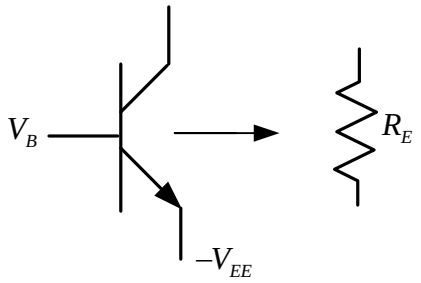
So far the phase angle is concerned, it starts with zero at ω =0. Thereafter, it changes by $+45^o$ at each zero of T(s) relative to its value at the previous critical point (zero or pole) and it changes by $-45^o$ at each pole relative to its value at the previous critical point (zero or pole). *For a succession of zeros and poles of T(s), the phase angle values are added up successively.*

## Appendix-VI: Practice Exercises

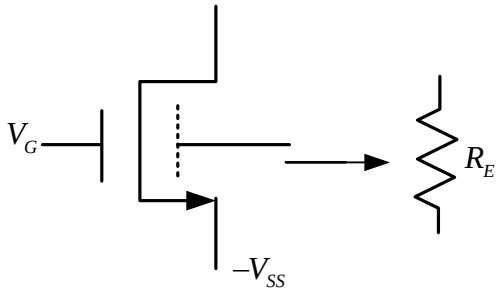
6.1 For the network shown below, find the output resistance for ac small signal case [hint; use dummy source at the output end and find v/I at that end].



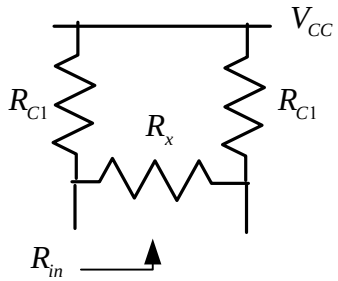

6.2 Repeat 1 with $R_E$ replaced by a BJT device as indicated below. [hint: use the ac equivalent circuit for the BJT device]



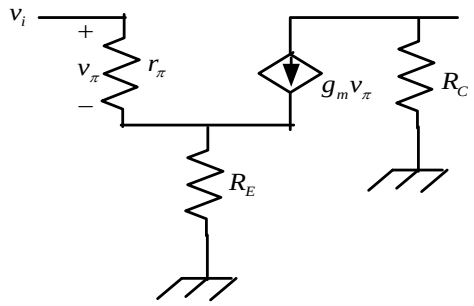

6.3 Repeat 1 with $R_E$ replaced by a MOS device as shown below.




6.4 A sub-network in a differential amplifier circuit appears as below. Find an expression fro $R_{in}$ considering small signal (ac) equivalent circuits. Use nodal matrix method.

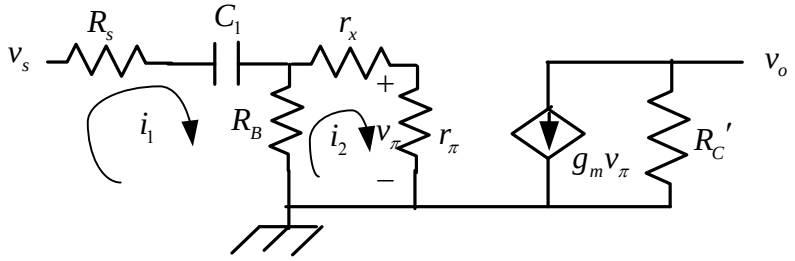


6.5 The ac equivalent circuit for a BJT amplifier with un-bypassed resistance $R_E$ at the emitter is shown below. Find, using nodal matrix analysis method, an expression for the voltage gain $v_o/v_i$.




6.6 Use the ac equivalent circuit and loop matrix analysis method to find the expression for the voltage gain $v_o/v_s$. [Ans. $-\frac{g_m R_c' R_B r_\pi}{R_{xx}} \cdot \frac{s}{s+1/C_1 R_{c1}}$, where

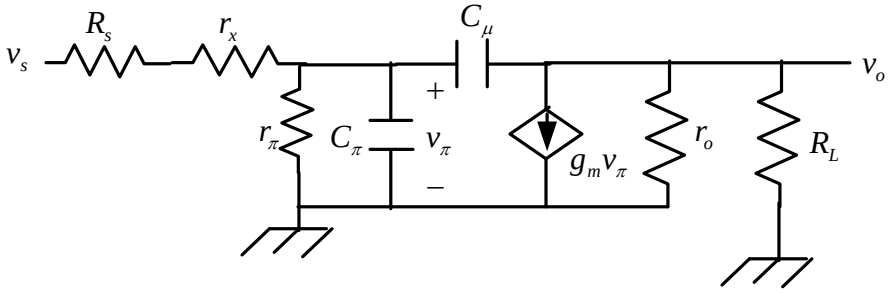
$R_{xx} = R_s R_B + R_s(r_\pi + r_x) + R_B(r_\pi + r_x);\ R_{c1} = R_s + R_B \,||\, (r_x + r_\pi)$ ]



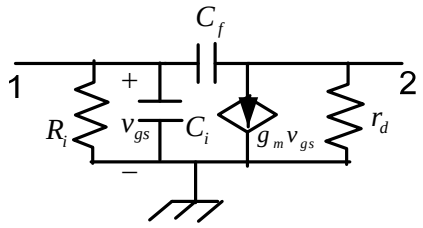

6.7 Consider the ac equivalent circuit of a BJT at high frequencies. Find $v_o/v_s$ using nodal matrix method. [Ans. $-\frac{(g_m - sC_\mu)g_s'}{\Delta}$; where

$\Delta = (g_s' + g_\pi)(g_o + g_L) + s[(g_\pi + g_s')C_\mu + (g_o + g_L)(C_\mu + C_\pi) + g_m C_\mu] + s^2 C_\pi C_\mu$, and

$g_s' = 1/(R_s + r_x)$, all $g_i = 1/r_i$.

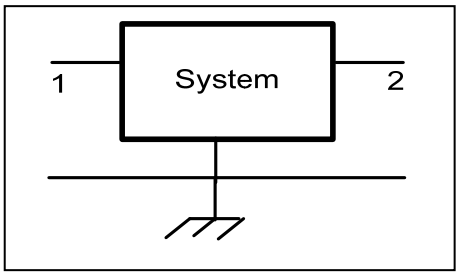


6.8 The high-frequency ac equivalent circuit of a MOSFET ampliflier is shown below. Find the two-port Y-matrix description for the system.[ hint: formulate $[I]=[Y][V], [Y]=\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$; then find $y_{11}, y_{12}$ ]




6.9 For the system as shown below, the measured $y_{11}$ data are tabulated as below. Find the ac equivalent model for the $y_{11}$ part of the system.[ hint: consider $y_{11}$ as a parallel combination of a resistance R and a reactance X. Find the values of R and the component associated (C or L) with X].

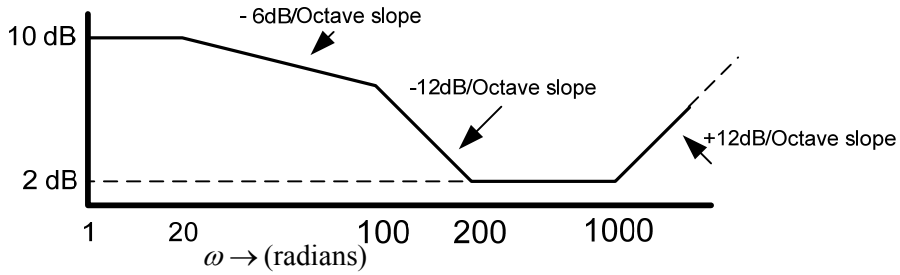
| Frequency | Re($y_{11}$) | Im($y_{11}$) |
|---|---|---|
| 100 | 1E-11 | 6.06E-6 |
| 1 K | 1E-11 | 60.6E-6 |
| 10 K | 1E-11 | 606E-6 |




6.10 A frequency domain transfer function is given by $T(s)=\frac{10}{s+20}$. Sketch the Bode plot for $|T(s)|$

6.11 A frequency domain transfer function is given by $T(s)=\frac{200s}{(s+10)(s+300)}$. Sketch $|T(s)|$ using Bode technique.

6.12 A sketch of $|T(s)|$ with $T(s)=\frac{1500(s+100)}{(s+20)(s+1000)}$, is shown below. If there is any error in the sketch, correct it and re-draw.


- 6dB/Octave slope
10 dB
-12dB/Octave slope
+12dB/Octave slope
2 dB
1
20
100
200
1000
$\omega \rightarrow$ (radians)

# CHAPTER 2

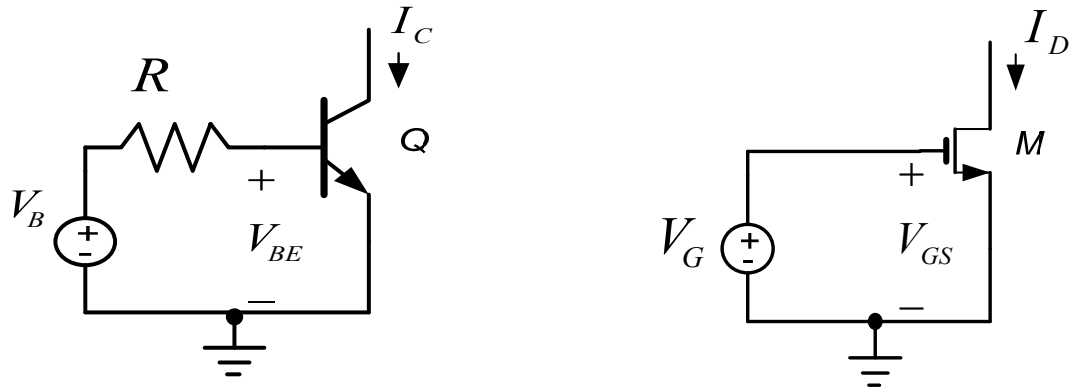
In this chapter we shall present additional (over those in Electronics-I course) electronic circuits that are used as subsystems in a larger electronic system, especially in connection with integrated circuit technology. In particular the following will be covered.

- Current source, current mirror and active loads
- Differential amplifiers (discrete as well as integrated circuit)
- Example of a multi-stage amplifier (such as an Operational Amplifier)

## 2.1 Current source, current mirror and current steering:

### 2.1.1: BJT and MOS current sources

Consider figures 1(a)-(b) which depict the basic configuration of a BJT, and an MOS current source, respectively.




(a) (b)

Figure 1: (a) basic BJT current mirror, (b) basic MOS current mirror

The output terminal (collector/drain) of the device delivers a constant DC current to the load (not shown explicitly) as long as the voltage $V_{BE}$ (for BJT) and $V_{GS}$ (for MOS) remains constant and the temperature remains fixed (say, 27 deg. C). The value of this DC current is given by:

(for BJT) $I_C \approx I_S \exp(V_{BE}/V_T)$

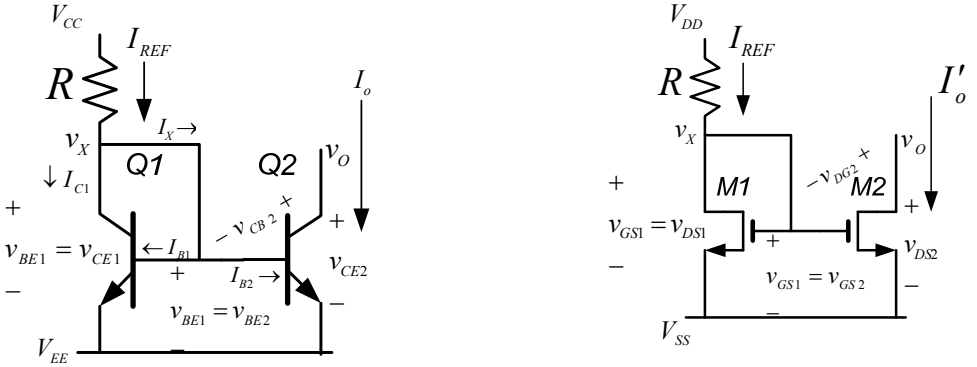
(for MOS) $I_D = \mu C_{ox} \frac{W}{2L}(V_{GS} - V_{TH})^2$

Note that the devices are assumed to operate in the active (for BJT) and saturation (for MOS) regions. In these regions, the I-V characteristics of the devices are almost parallel to the V-axis (i.e., $\Delta I/\Delta V = 0$). The output terminal is supposed to appear like an infinite resistance (internal resistance of an ideal current source) to the load system (not shown). But in reality this is never satisfied.

When the active device (i.e., transistor) is located nearer to the most positive DC supply line, the terms 'current source' is used. When the active device is nearer to the most negative (or ground) DC supply line, the name 'current sink' is used for the current source.

2.1.2: Basic BJT and MOS current mirrors

In an integrated circuit environment we need to provide DC bias currents to various subsystems located on the same wafer. It is not very economic to build an independent current source near the location of each of these subsystems. Instead, one reference current source is built and then current mirrors are used to generate several other DC currents which can feed the different subsystems. The basic configurations of a current mirror using BJT and MOS transistors are shown in figures 2(a)-(b).




(a) (b)

Figure 2: (a) BJT current mirror, (b) MOS current mirror

The operation of a current mirror can be easily understood as follows:

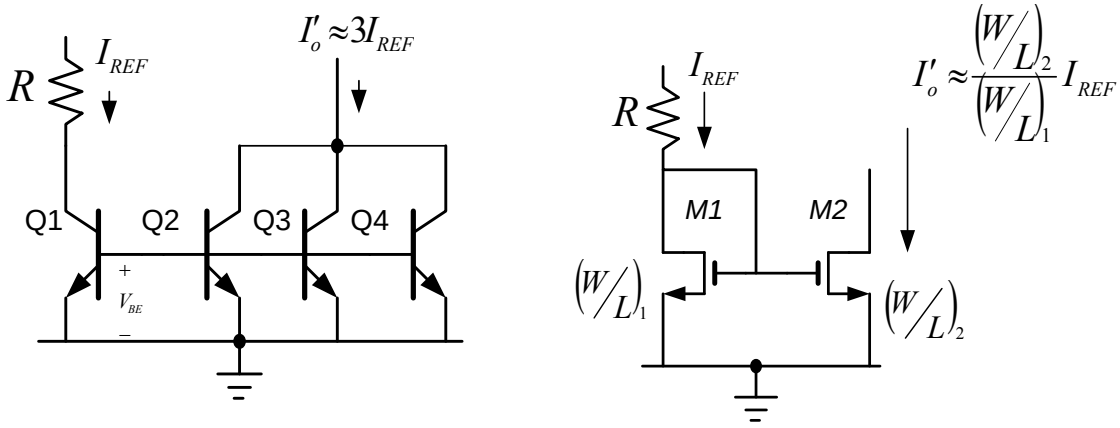
In case of the BJT: $I_o = I_{s2}\exp(V_{BE}/V_T)$; $I_{REF} \approx I_{C1} = I_{s1}\exp(V_{BE}/V_T)$

If the transistors are identical, we can put $I_{s1} = I_{s2}$. Then $I_o = I_{REF}$.

In case of the MOS: $I_o = \frac{\mu C_{ox}}{2}(\frac{W}{L})_2(V_{GS} - V_{TH})^2$; $I_{REF} = \frac{\mu C_{ox}}{2}(\frac{W}{L})_1(V_{GS} - V_{TH})^2$. So $I_o = I_{REF}\frac{(W/L)_2}{(W/L)_1}$.

If $(W/L)_2 = (W/L)_1; I_o = I_{REF}$.

Obviously, the key factor that makes the mirroring operation possible is maintenance of same $V_{BE}$ (for BJT) and same $V_{GS}$ (for MOS) for the pair (reference generator, and the mirror) of devices concerned. DC currents of different levels can be easily generated by adopting the following arrangements (Figures 3(a)-(b)).




(a) (b)

Figure 3: (a) BJT based current mirror with a gain of three (all BJTs identical), (b) MOS based current mirror with a gain equal to the aspect ratios (i.e., W/L values) of M1 and M2, the two NMOS are assumed to belong to same technology.

2.1.3: <u>DC bias design in case of current source/mirror</u>

To set up the reference current one has to employ a fixed DC power supply and a fixed resistance. Once this is done, the operation follows the equations already mentioned above. Let us consider two examples.

*Example 2.1.3.1 :*(BJT device):

$I_{ref} = \frac{V_{CC} - V_B}{R}$; $I_C = I_S e^{(V_B - V_{EE})/V_T}$, assuming n=1

KCL $I_{ref} - \frac{I_C}{\beta_1} - \frac{I_o}{\beta_2} = I_C$; $I_x = \frac{I_C}{\beta_1} + \frac{I_o}{\beta_2}$. Further,

$I_o = I_S e^{(V_B - V_{EE})/V_T}$. If $I_o$ is given, $I_S$ is known, and $V_{EE}$ is given, we can find $V_B$. Using the KCL equations above and assuming $\beta_1 = \beta_2 = \beta$, we can write

$\frac{V_{CC} - V_B}{R} - I_C(1 + \frac{1}{\beta}) - \frac{I_o}{\beta} = 0$. Now, if $V_{CC}$ and $\beta$ are known, We can solve the above equation for $R$.

Finding $R$ completes the DC design.

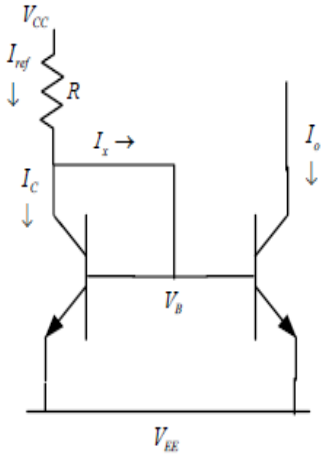



Figure 4 : Related to *Ex 2.1.3.1*

Consider $\beta_1=\beta_2=49$ ; $I_o$=3 mA ; $I_S$ =$10^{-14}$ A ; $-V_{EE}=V_{CC}$=5 V. Design the current source, assuming that both the BJT devices are identical.

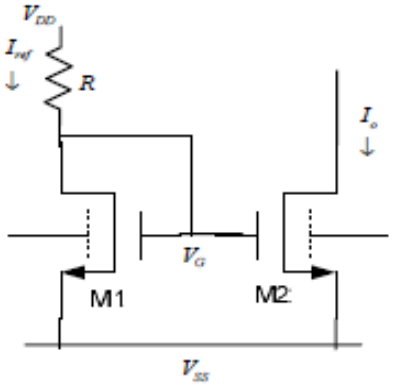
Designing the current source is to design the value of $R$.

Using $I_o = I_S e^{(V_B - V_{EE})/V_T}$, we can find $V_B$ =-4.34V. Then from $I_C = I_S e^{(V_B - V_{EE})/V_T}$, we can derive $I_C$ =2.92 mA. ( The accuracy may be affected by the calculator capability).

Then inserting the known values in $\frac{V_{CC} - V_B}{R} - I_C(1 + \frac{1}{\beta}) - \frac{I_o}{\beta} = 0$, we get

$\frac{5 + 4.34}{R} - 2.92 \times 10^{-3}(1 + 1/49) - 3 \times 10^{-3}/49 = 0$, gives $R$=3.071 kΩ. (This becomes 2.99 kilo ohms if $I_o=I_C$ = 3 mA is taken).

*Example 2.1.3.2* (MOS device):




$I_{ref} = \mu C_{ox}(\frac{W}{2L})_1(V_{GS} - V_{TH})^2$, will give $V_{GS}$ for M1, and with $V_{SS}$ known, we can determine $V_G$. Thus $V_G = V_{GS} + V_{SS}$. Then $R = \frac{V_{DD} - V_G}{I_{ref}}$. This completes the design of $R$

Figure 5 : Related to *Ex 2.1.3.2*

If $(W/L)_2$ is $A$ times that of $(W/L)_1$, and the two MOS transistors belong to the same technology, i.e., $\mu$, $C_{ox}$, $V_{TH}$ are identical for both, we can write $I_o = \mu C_{ox}(W/2L)_2(V_{GS} - V_{TH})^2 = AI_{ref}$ . Suppose $\mu C_{ox}$ =100 μA/volt$^2$, $(W/L)_1$=5, $(W/L)_2$=10, $V_{TH}$ =0.7 volts, can you design the current source (i.e., find $R$), for $I_o$=10 $\mu A$. Given $V_{DD}$ =-$V_{SS}$ =5 volts ?

*Solution :* From the given information, you find $A = \frac{(W/2L)_2}{(W/2L)_1}$ =10/5=2. Then $I_{ref}$ =$I_o$/$A$=5 $\mu A$.

Substituting in the square law equation for M1, $5\times10^{-6} = 100\times10^{-6}\times5\times(V_{GS}-0.7)^2$ , you can calculate $V_{GS}$ =0.6 or 0.8 volts.

For the MOS to conduct, $V_{GS}$ must be > $V_{TH}$ =0.7 volts (given). So you accept $V_{GS}$ =0.8 volts. Since $V_{SS}$ =-5 volts, $V_G$ -$V_{SS}$= 0.8, leads to $V_G$= -4.2 volts.

Now using the calculated values of $I_{ref}$, $V_G$, and the given value of $V_{DD}$, you can find $R$=1.84 Mega Ω.

2.1.4 Current steering : In the above we have cited only one kind of transistors, i.e., NPN (and NMOS) to illustrate the operation of current mirrors. In real systems, currents need be delivered to both kinds of devices. One can then start with a basic mirror made from, say, NMOS stages and steer the path of the current through PMOS stages. Steering implies continuation of the current mirroring operation through both P- and N-type devices in a large electronic system. An example is given in figure 6.

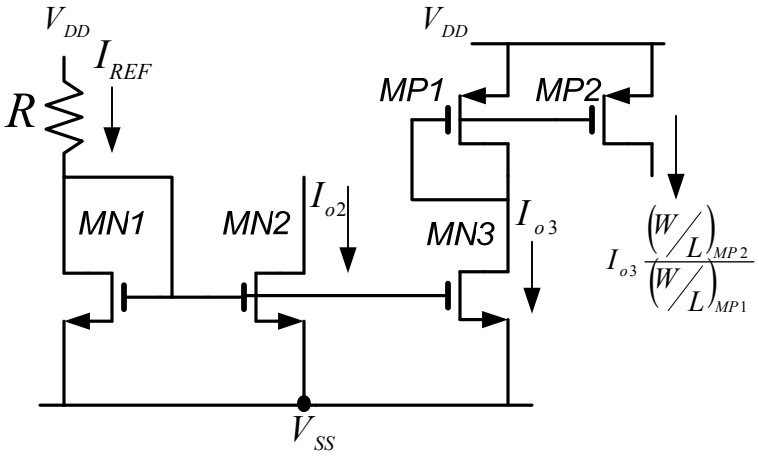



Figure 6: Current steering from a NMOS stage to a PMOS stage.

2.1.5 Non-ideal effects:

2.1.5 A: : *Base-width/Channel modulation effect:* We already have learnt that the current at the output of a BJT/MOS device increases slowly with $V_{CE}$ / $V_{DS}$, due to the base-width/channel modulation effect. In base-width modulation (for BJT), the increase of current is due to *more number* of charge carriers arriving at the collector. In channel modulation (for MOS), the reason is *faster* collection of the charges by virtue of the electric field at the drain-gate transition. Because of these, the output resistance of a current mirror, for small signal case, is never very large (not to think of infinite value!). For BJT the output resistance is of the order of 20-50 kilo ohms, while in MOS, it could be 100-1000 kilo ohms, in a basic current mirror.

The above effect(s) can be easily taken care of by suitably modifying the equation(s) pertaining to current mirroring operation.

2.1.5 B: *Effect of channel modulation in a MOS current mirror*

Since the variation of $I_{DS}$ with $V_{DS}$ in the saturation region of operation is a consequence of the channel length modulation, we need to consider the I-V equation (for an NMOS):

$I = \mu C_{ox}(W/2L)(V_{GS}-V_{TH})^2(1+\lambda V_{DS}) = I_o(1+\lambda V_{DS})$, where $I_o = \mu C_{ox}(W/2L)(V_{GS}-V_{TH})^2$.

From the geometrical drawing of figure 7, we can deduce the following:

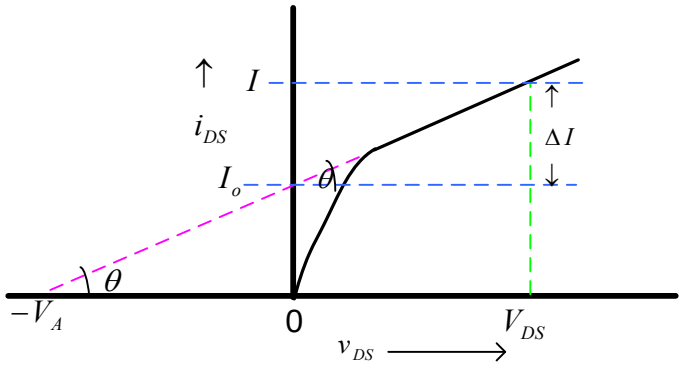



Figure 7: Calculations for the channel modulation effect (*Early* effect) in an NMOS device.

$\frac{\Delta I}{V_{DS}} = \tan\theta = \frac{I_o}{|V_A|}$, so $\Delta I = \frac{I_o}{|V_A|}V_{DS}$. Then $I = I_o + \Delta I = I_o + I_o\lambda V_{DS}$, so $\lambda = \frac{1}{|V_A|}$

The $V_{DS}$ in the reference MOS and the mirroring MOS will be different because of different loading condition, in general $I_{REF} = I_{MIRROR}$ will not hold (for two identical matched MOS transistors). The result of differing $V_{DS}$ bears upon the associated $V_{DG}$ as well. For the reference generator (drain-gate connected) $V_{DG}$ =0. For the mirror transistor $V_{DG}=V_{DS} - V_{GS}$ which is ≠0, since the gate is not connected to the drain. When the reference and the mirror transistors have different $V_{DS}$ values the current transfer ratio will be given by

$$\frac{I_{MIRROR}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})}$$

*Tracking error*: This is the difference between the ideal output bias current (i.e., ignoring the channel modulation efect) and the actual output bias current (including the channel modulation effect).

Note the following work, which includes the effect of $V_{DS}$ in both the reference generator transistor and the mirroring transistor. Consider figure 8.

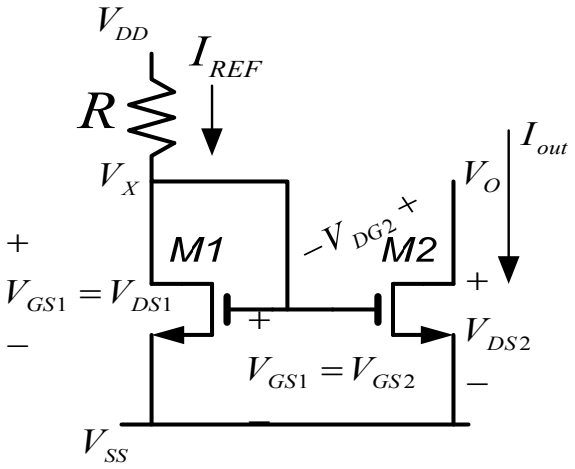



Figure 8: Illustrating the effect of unequal $V_{DS}$ in the reference and the mirroring MOS transistors

$I_{REF} = I_o(1+\lambda V_{DS1}) = I_o(1+\lambda V_{GS1})$, since $V_{DS1} = V_{GS1}$ because of gate-drain connection.

$I_{MIRROR} = I_{out} = I_o(1+\lambda V_{DS2})$, where $V_{DS2} = V_{DG2} + V_{GS2} = V_{DG2} + V_{GS1}$. Then $I_{REF}$ - $I_{MIRROR}$ $= -I_o\lambda V_{DG2}$.

Thus, $I_{MIRROR} = I_{REF} + I_o\frac{1}{V_A}V_{DG2} \approx I_{REF}(1+\frac{V_{DG2}}{V_A})$, **assuming** that $I_o \approx I_{REF}$.

Now, since $V_{DG2} = V_{DS2} - V_{GS2}$, and $V_{DS2} = V_o - V_{SS}$ (see the schematic), one can finally write

$I_{MIRROR} = I_{out} = I_{REF}(1 + \frac{V_O - V_{SS} - V_{GS2}}{V_A})$. The current tracking error is $I_{REF} - I_{out}$. Ideally this should be zero. (*quiz:* What will be the tracking error if $I_{REF} = I_{OUT}$ is not assumed?)

2.1.5 C: *Effect of finite β in case of a BJT mirror*

Because each BJT has a finite current gain $\beta$, a part of $I_{REF}$ is diverted to the base of the reference generator transistor, making $I_C = I_{REF} - I_X$ (see Fig.9). The mirror transistor having same $V_{BE}$ as the reference transistor will follow $I_C$ of the reference transistor. Thus $I_{OUT}$ of the mirror transistor differs from $I_{REF}$, introducing an error in tracking $I_{REF}$.

*Tracking error*: This is the difference between the ideal output bias current (i.e., assuming infinite $\beta$) and the actual output bias current (using finite $\beta$). Consider the following hints for the necessary derivations (see figure 9).

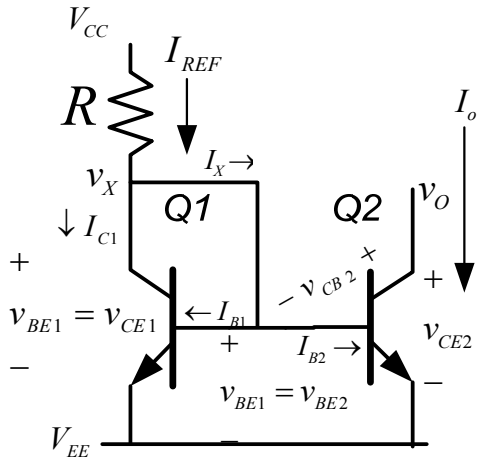



Figure 9: Illustrating the effect of finite β in a BJT current mirror

We need to find $I_{REF} - I_o$. Starting with $I_{REF}$, we have a KCL at the collector of *Q1*, i.e., at the node of $V_X$. Thus we get..

Then $I_X$ is……

Writing $I_{B1} = I_{E1}/...$,

**Assuming** matched transistors, $\beta_1 = \beta_2 = \beta$, so $I_{E1} = I_{E2} = I_E$, you get $I_{REF} = \left(\frac{\beta}{\beta+1} + \frac{2}{\beta+1}\right) I_E$. But $I_o = .... = \frac{\beta}{\beta+1} I_E$. Then, replacing $I_E$ in the expression of $I_{REF}$ by the expression of $I_o$, you can get…

Now find the expression for $I_{REF} - I_o = \Delta I$….

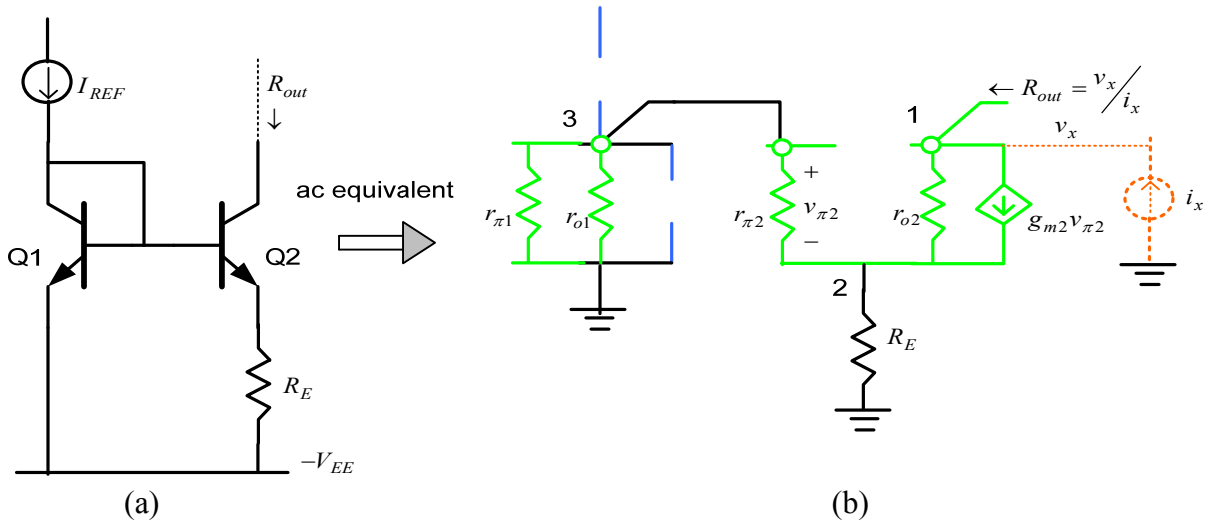
Relative tracking error $\Delta I/I$…

% tracking error…

2.1.5 D: *Improved current mirrors:*

The principal defect of the basic current mirror is the finite output resistance ($R_{out}$ ) for ac signals. This arises out of the finite slope of the $I_C$ vs. $V_{CE}$ (for BJT) or $I_D$ vs. $V_{DS}$ (for MOS) characteristic of a single transistor. Certain circuit techniques have been invented to reduce this slope thereby increasing the value of $R_{out}$ of the current mirror. The technique involves use of transistors stacked one on top of another and use of feedback principles. We shall examine the cases using network analysis principles. Increasing $R_{out}$ makes the current mirror appear more closely like an ideal current source.

- Widlar current mirror




(a) (b)

Figure 10: (a) schematic of the Widler current mirror circuit, (b) ac equivalent circuit for $R_{out}$ calculation.

Consider the ac equivalent circuit in Fig.10(b). By inspection we can derive the following

(i) The passive admittance matrix PAM (using $g_x$ for $1/r_x$, $x$ being a general element) is:

$$\begin{array}{c} \\ \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \begin{array}{c} \begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \end{array} \\ \begin{bmatrix} g_{o2} & -g_{o2} & 0 \\ -g_{o2} & g_{o2}+g_E+g_{\pi 2} & -g_{\pi 2} \\ 0 & -g_{\pi 2} & g_{\pi 1}+g_{o1}+g_{\pi 2} \end{bmatrix} \end{array}$$

(ii) The node voltage vector is : $[\ V_1 \quad V_2 \quad V_3\ ]^T$

(iii) The current source vector is:

$$\begin{array}{c} \\ \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \begin{bmatrix} i_x - g_{m2}v_{\pi 2} \\ g_{m2}v_{\pi 2} \\ 0 \end{bmatrix}$$

(iv) The dependant current source $g_{m2}v_{\pi 2}$ can be expanded as $g_{m2}(V_3\text{-}V_2)$. Substituting in the current source vector expression, we can re-write step (iii) as:

$$\begin{array}{c} \\ \text{Node\#1} \\ \text{Node\#2} \\ \text{Node\#3} \end{array} \begin{bmatrix} i_x - g_{m2}V_3 + g_{m2}V_2 \\ g_{m2}V_3 - g_{m2}V_2 \\ 0 \end{bmatrix}$$

(v) Combining (i), (ii) and (iv) in the general nodal admittance matrix (NAM) equation form **Y V =I,** we can derive:

$$\begin{array}{c} \begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \end{array} \\ \begin{bmatrix} g_{o2} & -g_{o2} & 0 \\ -g_{o2} & g_{o2}+g_E+g_{\pi 2} & -g_{\pi 2} \\ 0 & -g_{\pi 2} & g_{\pi 1}+g_{o1}+g_{\pi 2} \end{bmatrix} \end{array} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} i_x - g_{m2}V_3 + g_{m2}V_2 \\ g_{m2}V_3 - g_{m2}V_2 \\ 0 \end{bmatrix}$$

(vi) Transferring the voltages $V_2$, $V_3$ on the right hand side (RHS) to the left side, respectively in the columns of *Node#2* and *Node#3*, with a consequent change in sign we derive

$$\begin{array}{c} \begin{array}{ccc} \text{Node\#1} & \text{Node\#2} & \text{Node\#3} \end{array} \\ \begin{bmatrix} g_{o2} & -g_{o2}\boxed{-g_{m2}} & \boxed{g_{m2}} \\ -g_{o2} & g_{o2}+g_E+g_{\pi 2}\boxed{+g_{m2}} & -g_{\pi 2}\boxed{-g_{m2}} \\ 0 & -g_{\pi 2} & g_{\pi 1}+g_{o1}+g_{\pi 2} \end{bmatrix} \end{array} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} i_x \\ 0 \\ 0 \end{bmatrix}$$

(vii) The solution $v_x$=$V_1$=f($g_x$)$i_x$, produces the expression of $R_{out}$ =f($g_x$). Specifically, using Krammer's rule we can evaluate (*use of MAPLE* can be helpful)

$$R_{out} = \frac{g_{o2}g_{\pi 1} + g_{o2}g_{o1} + g_{o2}g_{\pi 2} + g_E g_{\pi 1} + g_E g_{o1} + g_E g_{\pi 2} + g_{\pi 1}g_{\pi 2} + g_{\pi 2}g_{o1} + g_{m2}g_{\pi 1} + g_{m2}g_{o1}}{g_{o2}g_E g_{\pi 1} + g_{o2}g_E g_{o1} + g_{o2}g_E g_{\pi 2} + g_{o2}g_{\pi 1}g_{\pi 2} + g_{o1}g_{o2}g_{\pi 2}}$$

- *Numerical evaluation*:

If we assume that the two BJTs are identical with $V_A$=50 volts, $I_C$=$I_{REF}$ =1 mA, $\beta$=99, $R_E$=1 $k\Omega$, we can determine all the parameters in the expression for $R_{out}$, and finally get $R_{out}$ =**901 *kΩ*** (approximately). This is a large value. This is the result of inserting $R_E$ at the emitter of Q2.

To gather an idea of $R_{out}$ without the emitter resistance $R_E$, we can set $R_E$ =0, i.e., $g_E$ =infinity. We can evaluate

$R_{out}\,|_{R_E=0} = \dfrac{g_{\pi 1} + g_{o1} + g_{\pi 2}}{g_{o2}g_{\pi 1} + g_{o1}g_{o2} + g_{o2}g_{\pi 2}}$ (lot simpler!)= 50 $k\Omega$ (i.e., simply $r_{o2}$). Thus inclusion of $R_E$ at the emitter increases $R_{out}$ by a factor of about 901/50 =18 times!

- *Demonstration by SPICE (Circuit Simulation)*

  *Case I:* $R_E$ is very small (1 milli ohms), i.e., it is like an ordinary current mirror with emitter of Q2 (almost) shorted to ac ground.

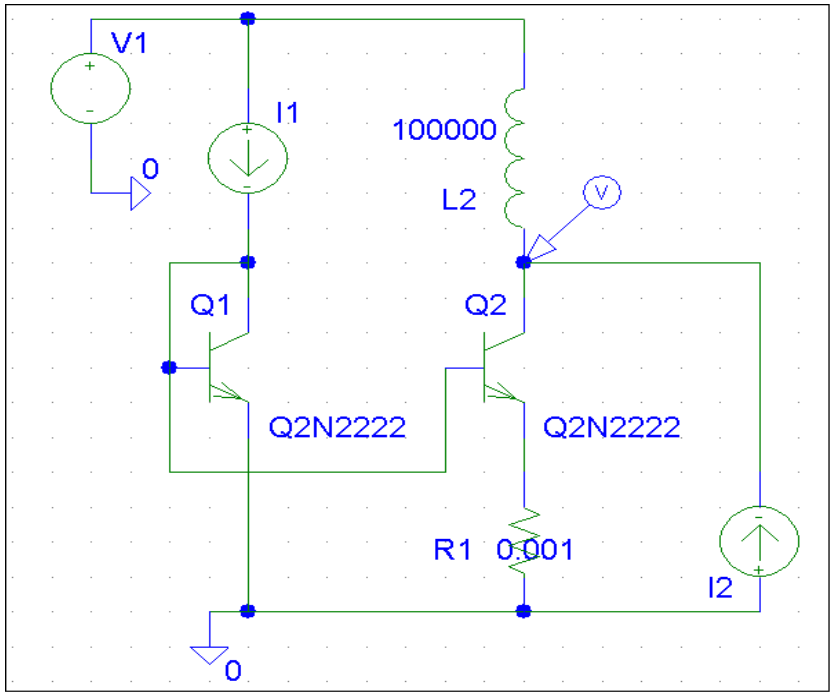



Figure 11:

The ouput list shows DC and ac equivalent circuit parameters for Q1 and Q2

**** BIPOLAR JUNCTION TRANSISTORS

| NAME | Q_Q1 | Q_Q2 |
|---|---|---|
| MODEL | Q2N2222 | Q2N2222 |
| IB | 6.69E-06 | 6.69E-06 |
| IC | 9.87E-04 | 1.11E-03 |
| VBE | 6.46E-01 | 6.46E-01 |
| VBC | 0.00E+00 | -9.35E+00 |
| VCE | 6.46E-01 | 1.00E+01 |
| BETADC | 1.48E+02 | 1.66E+02 |
| GM | 3.80E-02 | 4.28E-02 |
| RPI | 4.29E+03 | 4.29E+03 |
| RX | 1.00E+01 | 1.00E+01 |
| RO | 7.50E+04 | 7.50E+04 |
| CBE | 5.20E-11 | 5.40E-11 |
| CBC | 7.31E-12 | 3.01E-12 |
| CJS | 0.00E+00 | 0.00E+00 |
| BETAAC | 1.63E+02 | 1.84E+02 |
| CBX/CBX2 | 0.00E+00 | 0.00E+00 |
| FT/FT2 | 1.02E+08 | 1.20E+08 |

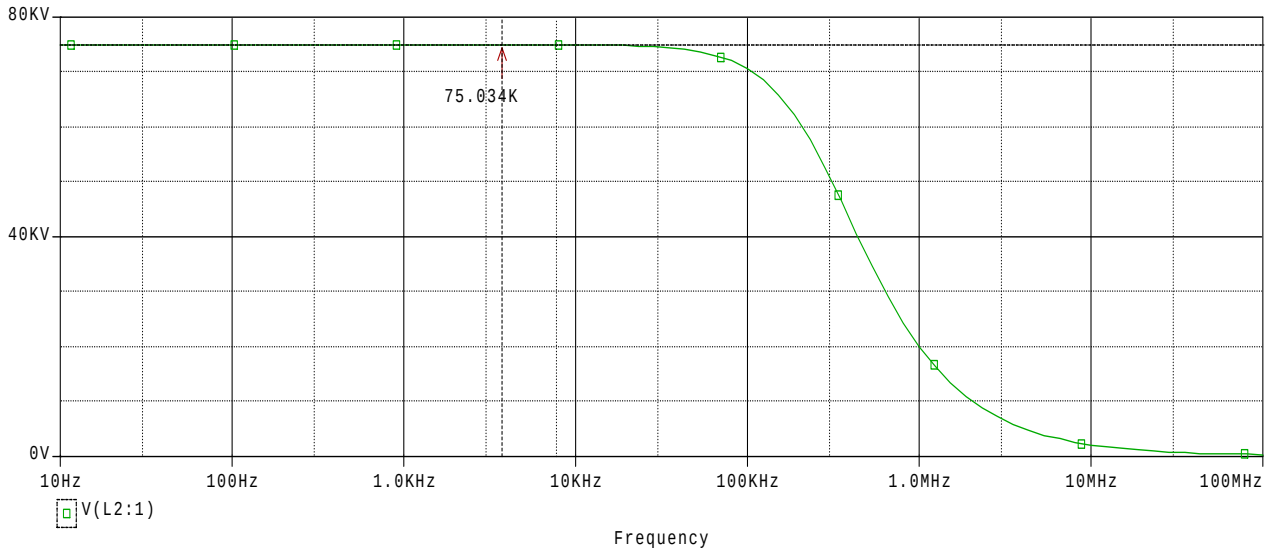



Figure 12:

$R_{out}$ is about 75 kilo ohms which is equal to $r_o$ of Q2 (check from the list, shown in GREEN shade)

*Case II*: $R_E$ is increased to 1000 ohms (i.e.,it is like the normal Widlar current mirror). The schematic changes.

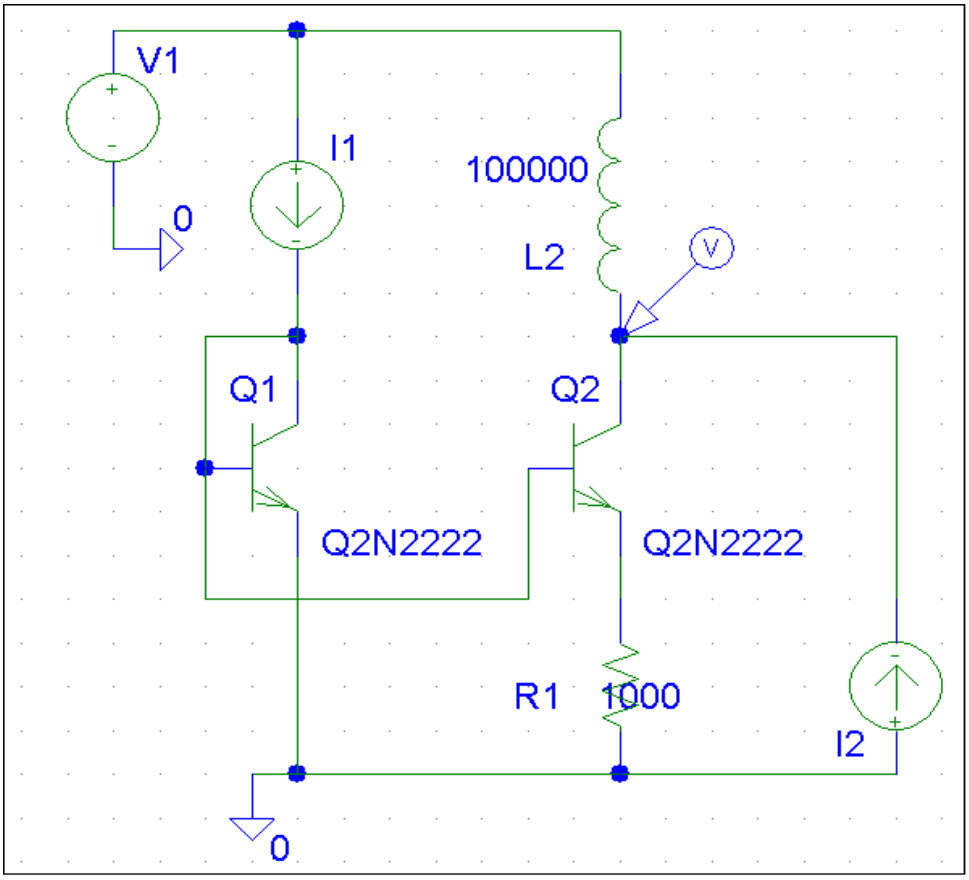



Figure 13:

The DC and ac equivalent circuit parameters now become different in case of Q2. Check the output list below.

**** BIPOLAR JUNCTION TRANSISTORS

| NAME | Q_Q1 | Q_Q2 |
|---|---|---|
| MODEL | Q2N2222 | Q2N2222 |
| IB | 6.72E-06 | 5.88E-07 |
| IC | 9.93E-04 | 7.09E-05 |
| VBE | 6.46E-01 | 5.74E-01 |
| VBC | 0.00E+00 | -9.35E+00 |
| VCE | 6.46E-01 | 9.93E+00 |
| BETADC | 1.48E+02 | 1.21E+02 |
| GM | 3.82E-02 | 2.74E-03 |
| RPI | 4.27E+03 | 5.09E+04 |
| RX | 1.00E+01 | 1.00E+01 |
| RO | 7.46E+04 | 1.18E+06 |

| | | |
|---|---|---|
| CBE | 5.21E-11 | 3.54E-11 |
| CBC | 7.31E-12 | 3.01E-12 |
| CJS | 0.00E+00 | 0.00E+00 |
| BETAAC | 1.63E+02 | 1.40E+02 |
| CBX/CBX2 | 0.00E+00 | 0.00E+00 |
| FT/FT2 | 1.02E+08 | 1.13E+07 |

On inserting the relevant values in the expression

$$R_{out} = \frac{g_{o2}g_{\pi 1} + g_{o2}g_{o1} + g_{o2}g_{\pi 2} + g_E g_{\pi 1} + g_E g_{o1} + g_E g_{\pi 2} + g_{\pi 1}g_{\pi 2} + g_{\pi 2}g_{o1} + g_{m2}g_{\pi 1} + g_{m2}g_{o1}}{g_{o2}g_E g_{\pi 1} + g_{o2}g_E g_{o1} + g_{o2}g_E g_{\pi 2} + g_{o2}g_{\pi 1}g_{\pi 2} + g_{o1}g_{o2}g_{\pi 2}}$$, we

can find (use MAPLE program if required) $R_{out}$ =4.112 Meg ohms

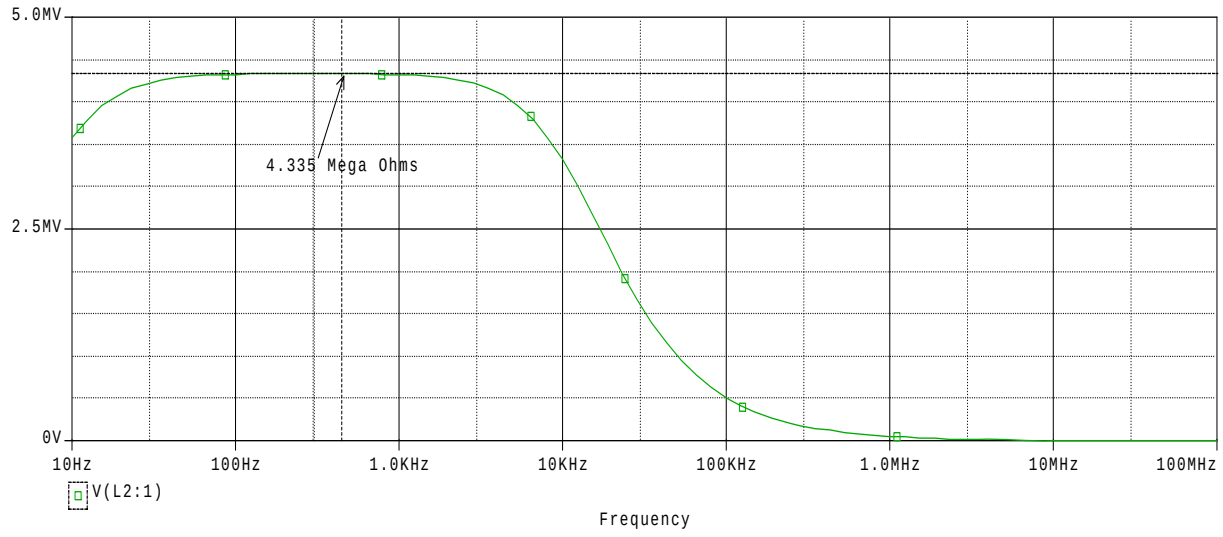



Figure 14:

The simulated value of $R_{out}$ is 4.335 Mega ohms. The increase is by a factor of 4335/75=57.8 times!

*Comment* : Between the values obtained by the theoretical formula and circuit simulation, we will accept the circuit simulation value as more realistic.

## 2.2 Active loads and uses:

An active load implies a resistance made from a transistor (active device). The resistance is primarily effective for small signal application. Sometimes transistors are also used like potentiometric resistances to deliver different levels of DC voltages, in an integrated circuits

environment. To understand the operation of a transistor as an active load (resistance), we need to consider the ac equivalent circuit of the transistor.

2.2.1*:* AC equivalent circuits for active loads

2.2.1 A*: Diode connected transistor:* This is easily obtained by connecting the gate and drain of a MOS (base and collector of a BJT). The resulting ac resistance is approximately $1/g_m$, where $g_m$ is the transconductance of the device (obtained by proper DC biasing). Consider the analysis below (see Fig. 15(a)-(c)).

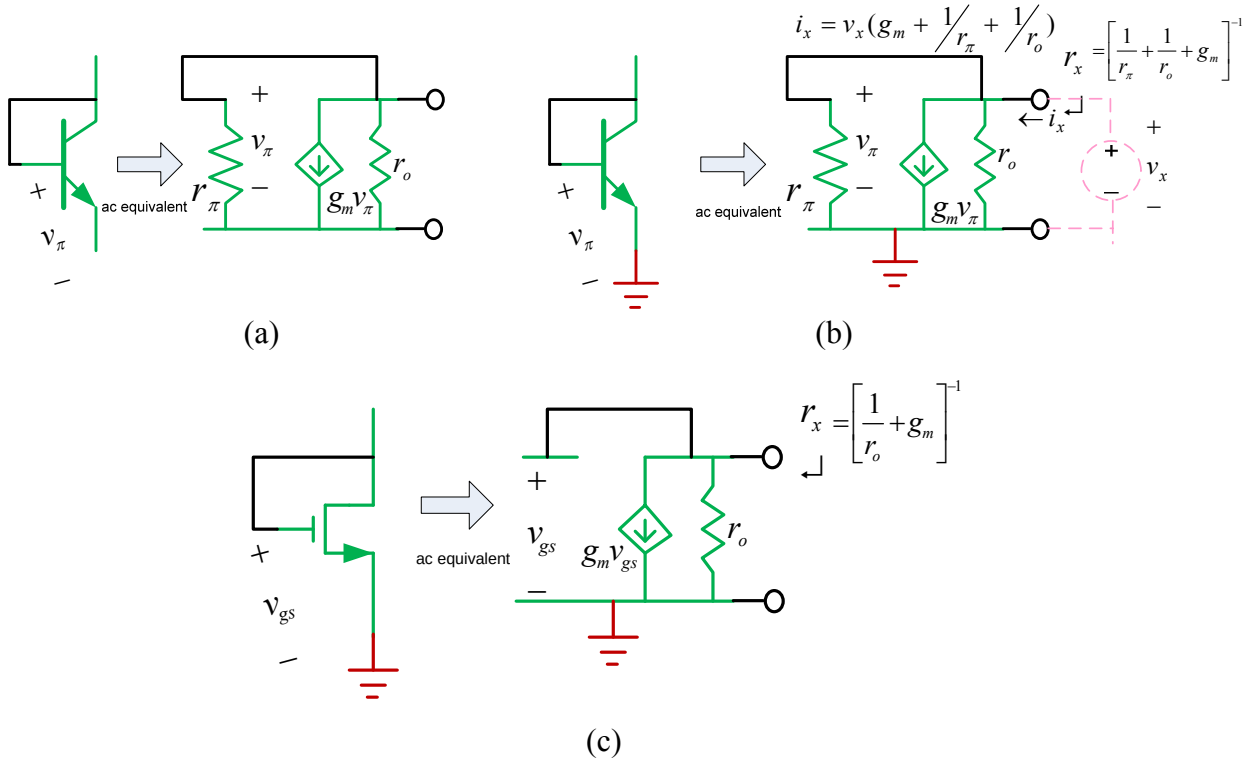
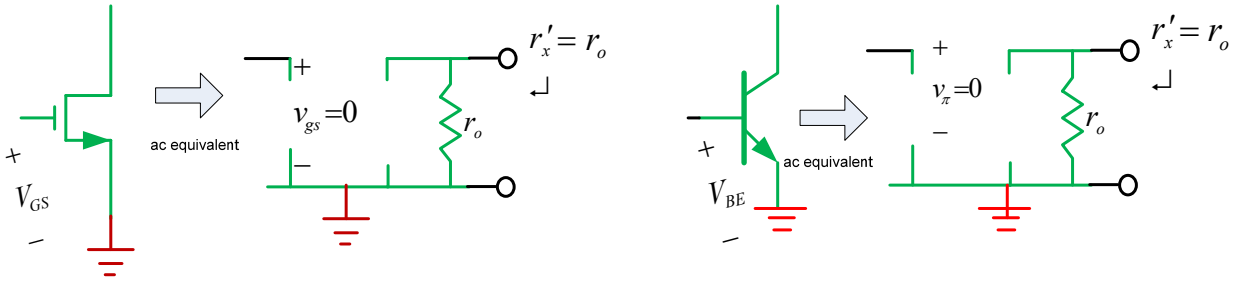



Figure 15: (a) diode connected BJT and ac equivalent circuit, (b) ac output resistance $r_x$ with emitter grounded (i.e., CE configuration) for ac signals, (c) diode connected MOS in CS configuration and the associated ac output resistance.

2.2.1 B: *Current source/sink connected transistor:* In this, the transistor is biased to operate in the active (for BJT) or saturation (for MOS) region in the output characteristics. Thus the collector-emitter (for BJT)/ drain-source (for MOS) nodes pair appear to function like a current source (for DC current) with an attended high value of resistance for small signal

application. A current mirror system can also used for the same purpose. The value of the resistance is approximately the output resistance of the device, i.e., $r_o$. Since $r_o >> 1/g_m$, when the transistor is operating in the active/saturation region (for BJT/MOS respectively), the current source/sink/mirror configuration is preferred when a high value of small signal resistance is required. Consider the cases below.




(a) (b)

Figure 16: (a) MOS transistor with fixed $V_{GS}$ (or fixed $V_{SG}$ for PMOS), (b) BJT device with fixed $V_{BE}$ (or $V_{EB}$ for NPN BJT).

In figures 16(a)-(b), the control voltages for the VCCS element in the transistors are fixed, i.e., DC. DC implies zero ac. Hence, the controlled current sources do not exist. The output resistance becomes simply $r_o$ of the transistors. This is a high value. Note that the terminal of the device is the *drain* terminal of the MOSFET and the *collector* terminal of the BJT. This is always the case irrespective of whether the device is an NPN/NMOS or PNP/PMOS type.

In summary, if we need a high-valued active resistance, we arrange the device (MOS or BJT) with a DC bias voltage between the controlling node pair (GS for MOS, BE for BJT), and look into the collector/drain of the active device. The ground terminals in Fig.16(a)-(b) could be a DC voltage bus (i.e., zero ac). Thus the transistors are configured to function as a current source/sink.

One must note that the high valued resistance $r_o$ is effective only when the signal follows the direction from collector/drain to emitter/source through the device. The emitter/source end is grounded to ac signals in this case. If, however, the signal follows the path from the emitter/source to collector/drain (i.e., opposite to the first case), the high valued resistance $r_o$

is not effective. In this case the resistance is approximately $1/g_m$ (the student is suggested to prove it). The collector/drain terminal in this case has to be grounded for ac signals. This situation does not arise for a *diode connected* transistor (i.e., case 2.2.1A).

## 2.2.2: Use of active loads in single stage amplifiers

### 2.2.2 A: *CE/CS amplifier*

The schematics for a CE/CS amplifier with an active loads are shown in Figures 17(a), (b) with current mirror active loads and in Figures 17(c), (d) with current source active loads.

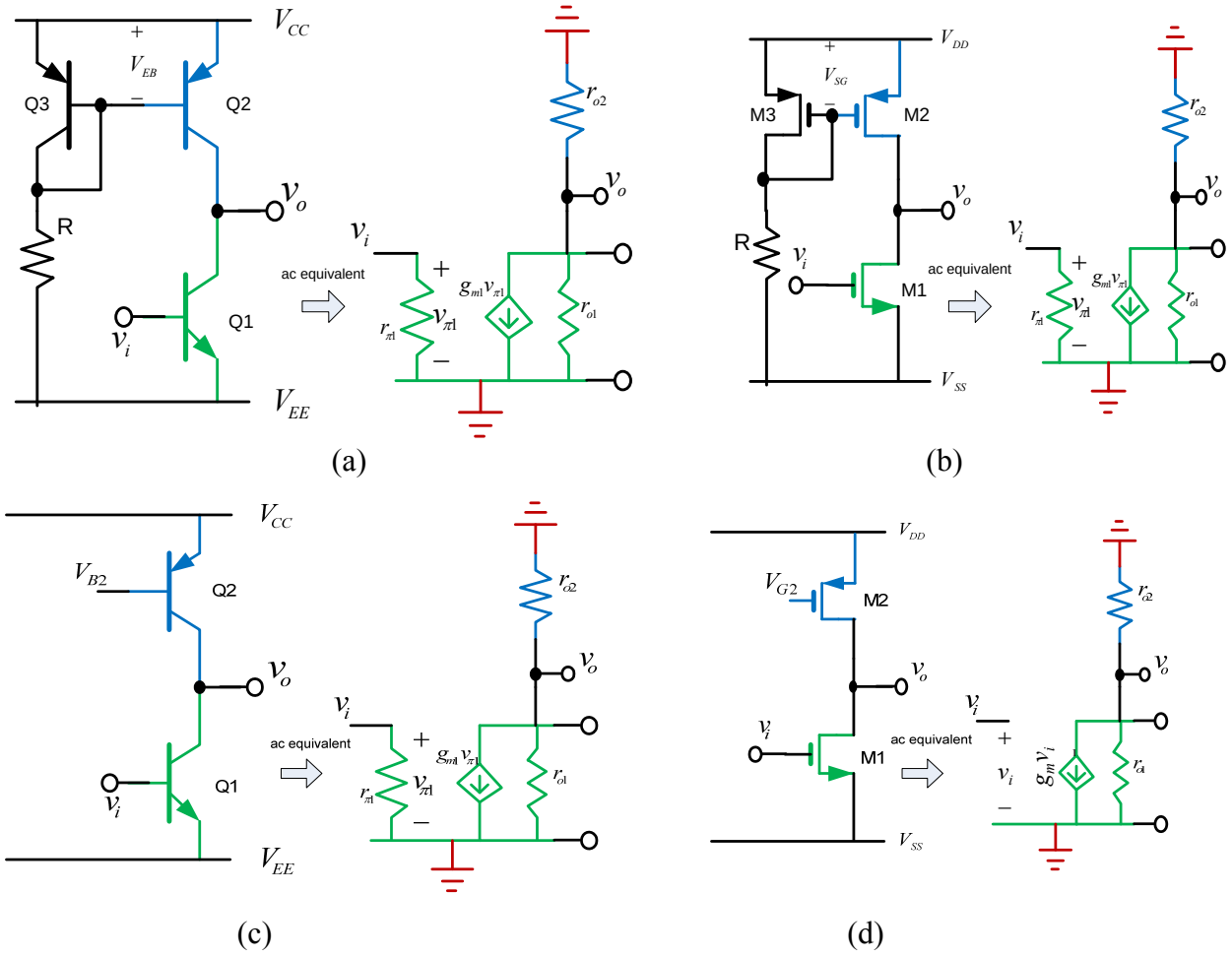



Figure 17: (a) CE BJT amplifier, and (b) CS MOS amplifier, with *current mirror* active load; (c) CE BJT amplifier, and (d) CS MOS amplifier, with *current source* active load

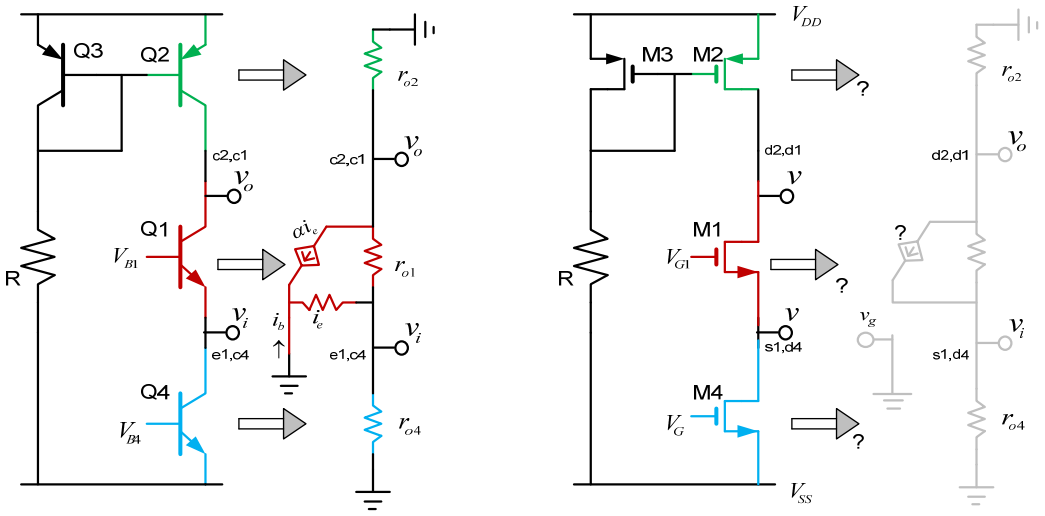
Note that the load transistor is of opposite kind to that of the amplifying device. The amplifying device receives the input ac signal. Since a high voltage gain is required, the current mirror/current source configuration of the active load is employed. This load presents a resistance of $r_o$ for small signal (ac) case. The active load stage has to be biased at the same DC current level as the basic amplifier stage (transistor Q1/M1 in the schematic). This is because the active load is in series connection with the output (collector/drain) terminal of the amplifier stage. If $g_m$ is the transconductance of the amplifier device, the open circuit voltage gain will be given by $-g_m R_L$, where $R_L = r_{o1}||r_{o2}$.

*Numerical calculation practice example:*

Consider an NMOS amplifier stage with a $g_m$ =200 micro mhos and a bias current of 10 µA. We use a PMOS active load for the amplifier. The Early voltages for the NMOS and PMOS devices are 30 V and 50 V respectively. What voltage gain can be realized from this amplifier?

### 2.2.2 B: *CB/CG amplifier*

As the name suggests, the base/gate terminal of the amplifying transistor will be held at a constant (DC) voltage. Consider figures 18(a)-(b).

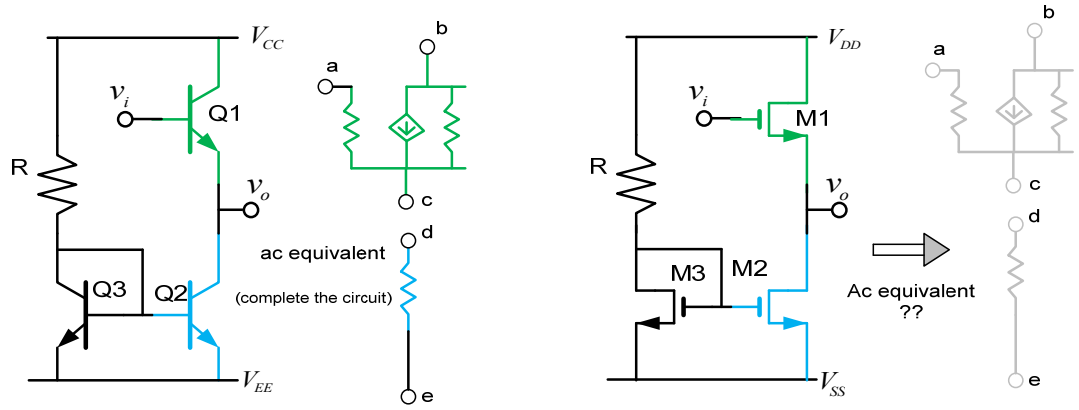



(a) (b)

Figure 18 : (a) CB BJT amplifier with current mirror active load, (b) CG MOS amplifier with current mirror active load.

2.2.2 C: *CC/CD amplifier*

The schematic diagrams are shown below. The collector (of BJT)/drain (of MOS) is connected to a fixed (DC) supply value (i.e., ac ground).




(a) (b)

Figure 18 : (a) CC BJT amplifier with active load (Current mirror), (b) CD MOS amplifier with active load (Current mirror). Which transistors make up the current mirrors ?

2.2.3 Use of active loads in improved current mirrors

2.2.3 A: *Widlar mirror using active load at the emitter*

By using the concept of active loads, we can enhance the output resistance of the Widlar mirror in Fig. 10(a) by replacing $R_E$ with output resistance of a BJT device. The schematic will change to either Fig.19(a) or (b). These are two possible *integrated circuit* implementation of the Widlar mirror. In Fig.19(a), we utilize $r_{o3}$ (why $r_{o3}$ of Q3?) Q3 to replace $R_E$ in Fig.10(a). In Fig.19(b), we utilize $1/g_m$ (why?) of Q3 to replace $R_E$ of Fig.10(a).

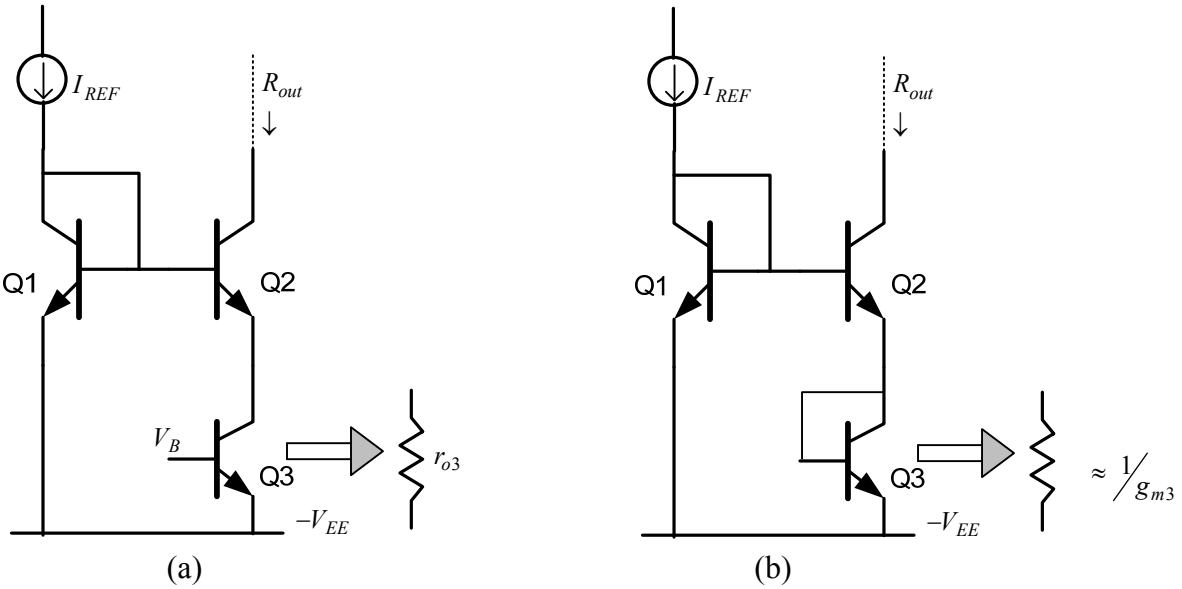
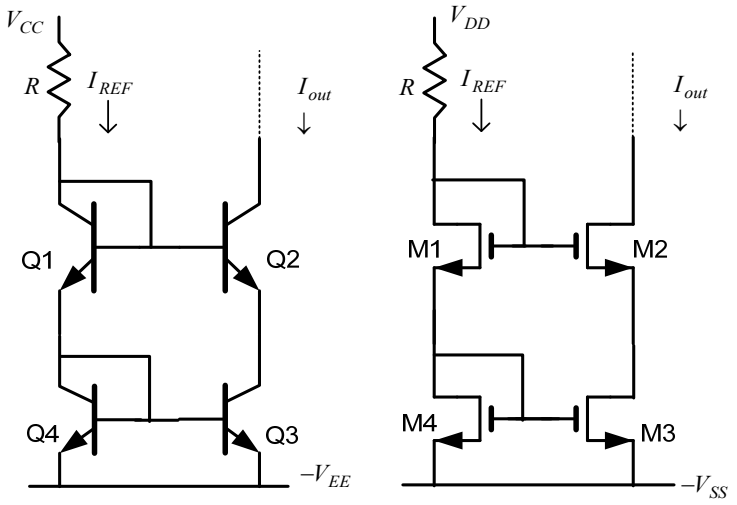



Figure 19: (a) Mirror of Fig.10(a) with $R_E$ replaced by fixed $V_{BE}$ across $Q_3$, (b) $R_E$ replaced by diode connected $Q_3$

In practical integrated circuit implementation of the current mirror, we need to replace the $I_{REF}$ by actual circuit elements providing a bias current. This has already been shown in Fig.9, for example.

Finally, use of too many (more than two) independent DC voltage sources is not practical in an actual integrated circuit substrate floor. Hence the arrangement around $Q_3$ in Fig.15(a) needs a change to reflect $Q_3$ as providing an *ac* output resistance of $r_o$. This can be achieved by including $Q_3$ as part of a current mirror as shown in Fig. 2(a), for example.

2.2.3 B: *Cascode current mirror*



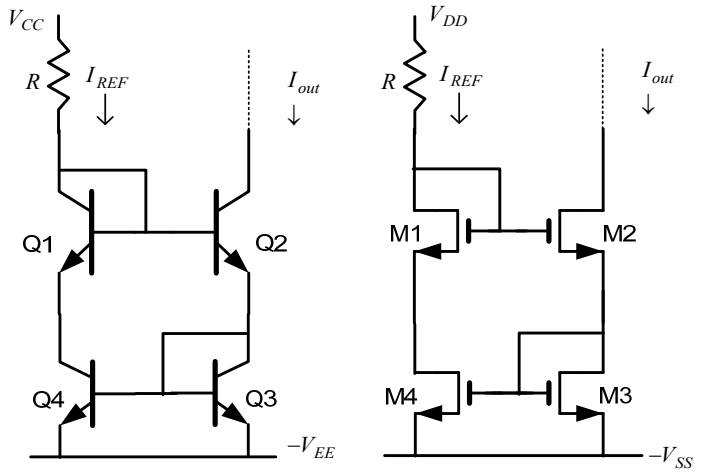

(a) (b)

Figure 20: (a) BJT cascode mirror, (b) MOS cascode mirror.

In Fig.19(a), by making $Q_3$ as part of the output device of a current mirror, we arrive at the circuit of Fig.20(a). Figure 20(b) shows the version with MOS transistors. These configurations are known as *cascode* current mirrors- Fig. 20(a) is the BJT version and Fig.20(b) is the MOS version of cascode current mirrors.

### 2.2.3 C: *Wilson current mirror*

In Fig.19(b), by making $Q_3$ as the diode connected part of a current mirror, we arrive at the circuit of Fig.21(a). Figure 21(b) shows the version with MOS transistors. These configurations are known as *Wilson* current mirrors- Fig. 21(a) is the BJT version and Fig.21(b) is the MOS version of Wilson current mirrors.




(a) (b)

Figure 21: (a) Wilson current mirror with BJT devices, (b) Wilson current mirror with MOS devices.

2.3: Differential amplifiers:

- Differential amplifiers with discrete resistance circuits.
- Differential amplifiers with active loads.

A differential amplifier amplifies difference of two signals. So this amplifier shall have two input nodes. The output can have one or two nodes. In the first case (one output node), the system is simply referred to as a differential-in single-out amplifier. In the second case (output having two nodes), the system will be called as differential-in, differential- out amplifier. Typical schematics of a differential amplifier using BJT and MOS devices are shown below. It can be seen that the emitter terminals of the input devices in a BJT differential amplifier are connected together and a DC current source provides the bias current through this tail-end. For a MOS amplifier, the source terminals of the input devices are connected together. In a discrete component version of the system, the loads are resistances. In an integrated circuit version, the loads will be replaced by active loads.

When the transistors are matched (i.e., identical and of same semiconductor process technology), the output of the differential amplifier will be zero when the two input signal are equal. Thus, a differential amplifier provides good rejection (i.e., produces zero output) for common mode

signals (same signal at the two input nodes). So it is preferably used in a noisy environment (such as the wafer of an IC chip with many systems/subsystems on the same wafer and placed very close to each other). For large signal operation, the differential output system will cancel out the even-order harmonic components of the signal. So this helps in reducing the harmonic distortion at the output. Reducing harmonic distortion and canceling common mode noise are two important features of differential amplifiers.

### 2.3.1 Differential amplifiers (DA) with transistors and resistances

#### 2.3.1.1 BJT device based DA (Large signal operation)

Figure 22 shows a differential amplifier with BJT devices, and resistive loads. For large signal operation, the basic diode equation can be employed at the base-emitter junction. The analysis follows. All the transistors are assumed to be operating in the active region.

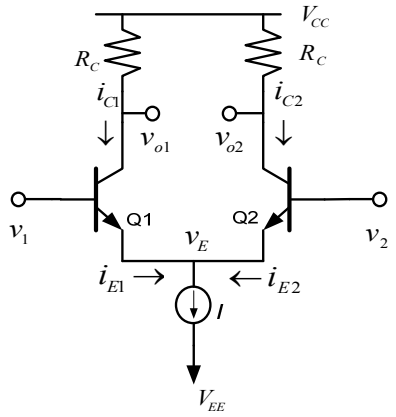



Figure 22: Differential amplifier schematic with BJT and discrete resistances

With identical transistors (i.e., matched transistors) and with zero input signals, $i_{E1} = i_{E2} = I/2$.
With the input signals $v_1$, $v_2$ applied, we use the exponential equation for the BE junctions of $Q_1$ and $Q_2$. Thus:

$i_{E1} = I_S \exp(\frac{v_1 - v_E}{V_T})$, $i_{E2} = I_S \exp(\frac{v_2 - v_E}{V_T})$, where $I_S$ is the scale current, $V_T$ is the thermal voltage (approx. 25 mV unless given otherwise), and $n = 1$ has been assumed.

When the signals are applied, $I = i_{E1} + i_{E2}$ always holds, although $i_{E1}$ may be $\neq i_{E2}$. This is because $I$ is a steady DC current which distributes between $i_{E1}$ and $i_{E2}$ as the signals $v_1$ and $v_2$ changes. On

writing $v_D = v_1 - v_2$= the differential input voltage (ac+DC), and after few algebraic manipulations using the *properties of ratio and proportions*, we can get

$$i_{E1} = I\frac{\exp(v_D/V_T)}{1+\exp(v_D/V_T)}, \quad i_{E2} = I\frac{\exp(-v_D/V_T)}{1+\exp(-v_D/V_T)}. \qquad (2.3.1.1)$$

Now assuming that the transistors have very high $\beta$ , we can set $i_{C1} = \alpha i_{E1} \approx i_{E1}$, $i_{C2} \approx i_{E2}$. Then

$$v_{o1} = V_{CC} - R_C I\frac{\exp(v_D/V_T)}{1+\exp(v_D/V_T)}, \quad v_{o2} = V_{CC} - R_C I\frac{\exp(-v_D/V_T)}{1+\exp(-v_D/V_T)}, \text{ and}$$

$$v_{o1} - v_{o2} = R_C I\left[\frac{\exp(-v_D/V_T)}{1+\exp(-v_D/V_T)} - \frac{\exp(v_D/V_T)}{1+\exp(v_D/V_T)}\right] \qquad (2.3.1.2)$$

The large signal differential voltage gain is: $G_v = \frac{v_{o1}-v_{o2}}{v_1-v_2} = \frac{v_{o1}-v_{o2}}{v_D}$.

Clearly, the gain is dependent upon the input differential voltage. This implies a non-linear system.

If we write $x = e^{v_D/V_T}$, then $1/x = e^{-v_D/V_T}$, and $v_{o1} - v_{o2} = R_C I[\frac{1}{1+x} - \frac{x}{1+x}]$.

The above can be simplified to $v_{o1} - v_{o2} = -R_C I\frac{e^{v_D/2V_T} - e^{-v_D/2V_T}}{e^{v_D/2V_T} + e^{-v_D/2V_T}} = -R_C I[\text{Tanh}(v_D/2V_T)]$.

2.3.1.2 MOS device based DA (Large signal operation)

An MOS based differential amplifier is shown in Figure 23. Compared to BJT based DA, the MOS DA has infinite input resistance. This feature fits well with the requirement of ideal controlled sources (such as VCVS, VCCS). Using the square law equation (i.e., ignoring the channel length modulation), the large signal operation can be derived as follows. The transistors are assumed to be in the saturation region.

In absence of any signal, $i_{S1} = i_{S2} = I/2$. In presence of signals $v_1$, $v_2$, using square-law formula (i.e., ignoring channel length modulation), we can write:

$$i_{D1} = i_{S1} = \mu_n C_{ox}(\frac{W}{2L})_1(v_1 - v_S - V_{THN})^2, \quad i_{D2} = i_{S2} = \mu_n C_{ox}(\frac{W}{2L})_2(v_2 - v_S - V_{THN})^2 \qquad (2.3.1.3)$$

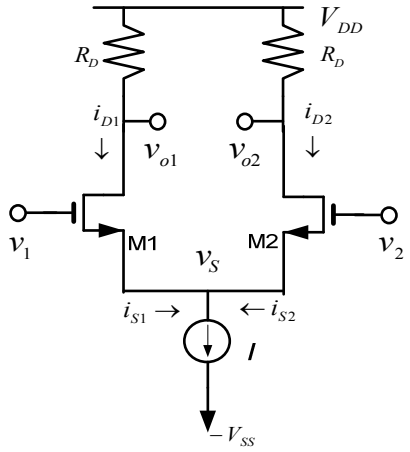



Figure 23: Differential amplifier schematic with NMOS transistors and discrete resistances

The above equations are for NMOS transistors with technological parameters $\mu_n$ (electron mobility), $C_{ox}$ (gate oxide capacitance), and $V_{THN}$ (Threshold voltage). For transistors with identical $W$ and $L$ values (i.e., same physical dimensions) $(W/L)_1 = (W/L)_2 = (W/L)$. The body (substrate) terminal of the MOS transistors have not been shown to improve clarity of the diagram. In reality, the body terminal of each of M1 and M2 will be connected to the most negative DC voltage in the system, i.e., to $-V_{SS}$. We can now write

$$v_1 - v_s - V_{THN} = \sqrt{\frac{2L}{W}\frac{1}{K_n} i_{S1}}, \quad v_2 - v_s - V_{THN} = \sqrt{\frac{2L}{W}\frac{1}{K_n} i_{S2}}, \quad K_n = \mu_n C_{ox} \qquad (2.3.1.4)$$

From the above, we get $v_1 - v_2 = v_D = \sqrt{\frac{2L}{K_n W}}(\sqrt{i_{S1}} - \sqrt{i_{S2}})$ (2.3.1.5)

Since $I$ is the DC bias current, $i_{S1} + i_{S2} = I$ always holds. Replacing $i_{S2}$ in terms of $I$ and $i_{S1}$, and writing $\beta_n = K_n W/2L$; we find $\sqrt{i_{S1}} - \sqrt{I - i_{S1}} = \sqrt{\beta_n}\, v_D$. Squaring both sides we get $I - 2\sqrt{i_{S1}(I - i_{S1})} = \beta_n v_D^2$. Changing sides and squaring again we get, $(I - \beta_n v_D^2)^2 = 4 i_{S!}(I - i_{S1})$.

Then re-arranging as a quadratic equation in $i_{S1}$, we get $i_{S1}^2 - i_{S1} I + \frac{1}{4}(I - \beta_n v_D^2)^2 = 0$. Solving for $i_{S1}$, we get $i_{S1} = \frac{I}{2} \pm \frac{1}{2}\sqrt{2\beta_n v_D^2 I - \beta_n^2 v_D^4}$. Selecting $i_{S1} = \frac{I}{2} + \frac{1}{2}\sqrt{2\beta_n v_D^2 I - \beta_n^2 v_D^4}$, we will get $i_{S2} = I - i_{S1} = \frac{I}{2} - \frac{1}{2}\sqrt{2\beta_n v_D^2 I - \beta_n^2 v_D^4}$. Knowing that $i_{D1} = i_{S1}$, $i_{D2} = i_{S2}$ and with more simplification, we arrive at

$$i_{D1} = \frac{I}{2} + \sqrt{\frac{\beta_n I}{2}}\sqrt{1 - \frac{\beta_n v_D^2}{2I}}v_D \,,\; i_{D2} = \frac{I}{2} - \sqrt{\frac{\beta_n I}{2}}\sqrt{1 - \frac{\beta_n v_D^2}{2I}}v_D \qquad (2.3.1.6)$$

Since, $v_{o1} = V_{DD} - R_D i_{D1}, \quad v_{o2} = V_{DD} - R_D i_{D2}$, we can get to:

$$v_{o1} - v_{o2} = -R_D v_D\left[\sqrt{2\beta_n I}\sqrt{1 - \beta_n v_D^2 \big/ 2I}\right] \qquad (2.3.1.7)$$

The differential voltage gain is $G_v = \frac{v_{o1} - v_{o2}}{v_D} = -R_D\left[\sqrt{2\beta_n I}\sqrt{1 - \beta_n v_D^2 \big/ 2I}\right]$ (2.3.1.8)

Since the gain depends upon the input differential voltage, the gain is not constant. This is the characteristic of a non-linear system. Under the condition $\frac{\beta_n v_D^2}{2I} << 1$, i.e., $v_D << \sqrt{2I \big/ \beta_n}$, we can get the linear approximation which is good for small signal application. The result is:

$G_v\,|_{linear} = \frac{v_{o1} - v_{o2}}{v_D} = -R_D\sqrt{2\beta_n I}$ .

2.3.1.3 Small signal operation (BJT based DA)

The basic schematic and the associated ac equivalent circuit of a BJT-based DA are shown in figures 24(a)-(c). Note that for simplicity of analysis the output resistance $r_o$ has been ignored (assumption $r_o \rightarrow$ infinity).

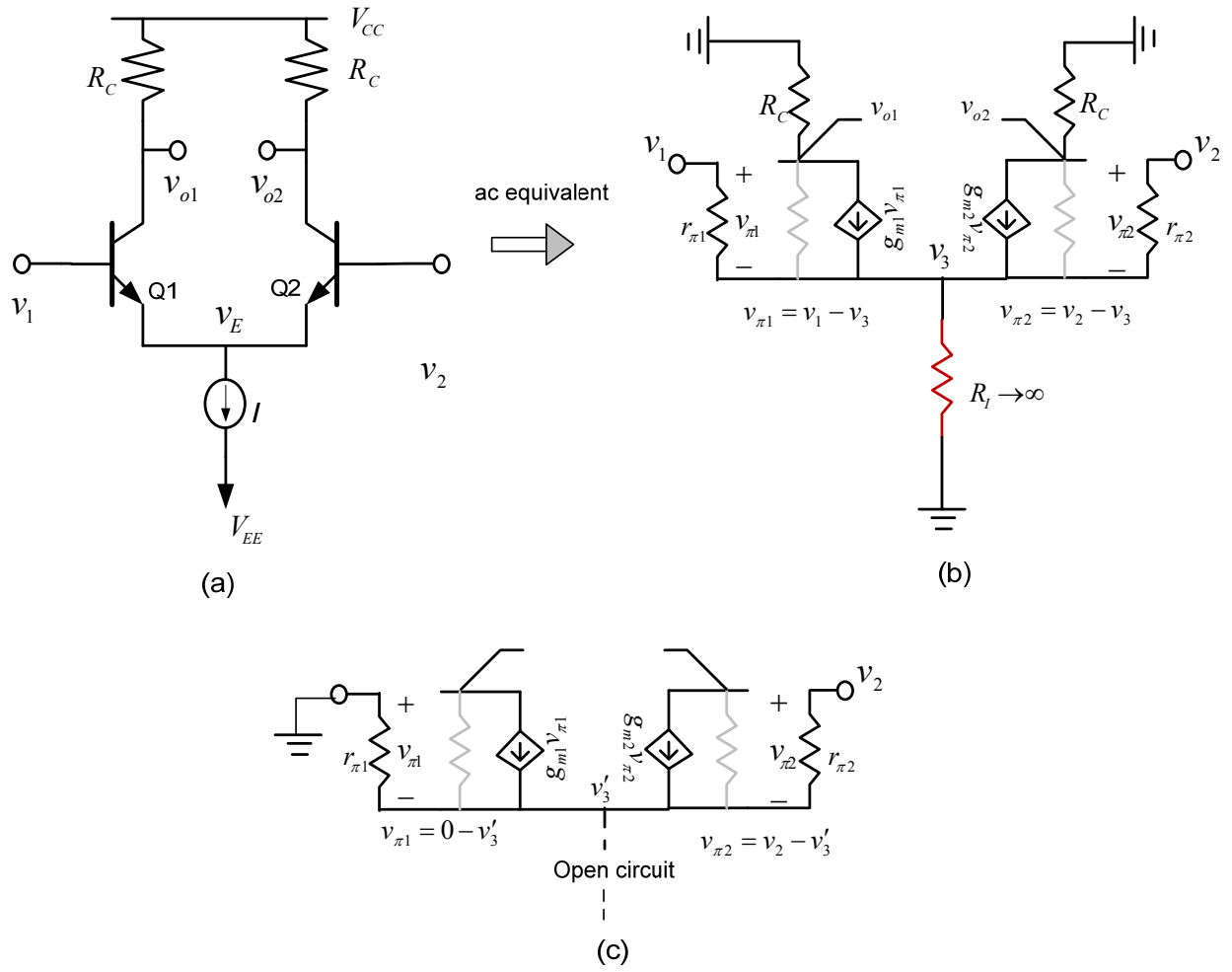



Figure 24: (a) schematic of the differential amplifier, (b) ac equivalent circuit (approximate), (c) equivalent circuit for partial (i.e., with $v_1$ =0, $v_2$ effective) calculations.

2.3.1.3 A: *emitter node voltage*

To calculate $v_3$ we can use principle of superposition (the small signal ac equivalent circuit has linear circuit elements, so superposition principle is applicable). Thus, with $v_1$=0, we get the part $v_3'$ due to $v_2$ alone. From Fig $-\frac{v_2 - v_3'}{r_\pi} - g_m(v_2 - v_3') - g_m(0 - v_3') + \frac{v_3'}{r_\pi} = 0$ .24(c), assuming that the transistors are matched (i.e., $r_{\pi 1} = r_{\pi 2} = r_\pi$ , $g_{m1} = g_{m2} = g_m$), the KCL at the $v_3'$ node leads to

$$-\frac{v_2 - v_3'}{r_\pi} - g_m(v_2 - v_3') - g_m(0 - v_3') + \frac{v_3'}{r_\pi} = 0 \qquad (2.3.1.9)$$

On simplification, we get $v_3' = v_2/2$ . Similarly, keeping $v_2$=0 and applying $v_1$, we can get the part $v_3''$ of $v_3$ as $v_3'' = v_1/2$ .

Thus, $v_3 = v_3' + v_3'' = (v_1 + v_2)/2$ (2.3.1.10)

2.3.1.3 B: *Small signal voltage gain* (balanced differential operation)

For balanced differential (i.e., $v_1$=-$v_2$), $v_3$ =0. Then

$$v_{o1} = -g_m v_1 R_C,\ v_{o2} = -g_m v_2 R_C,\quad v_{o1} - v_{o2} = -g_m R_C (v_1 - v_2) \qquad (2.3.1.11)$$

The voltage gain is thus ($v_{o1}$-$v_{o2}$)/($v_1$-$v_2$) =-$g_m R_C$.

The gain expression derived above is remarkably the same as one would obtain for a CE amplifier with $r_o$ of the device assumed to → infinity. Thus the differential amplifier, with balanced differential input, functions like a simple CE amplifier! The observation can be easily appreciated by recognizing that with balanced differential input signals the voltage $v_3 = v_1$+$v_2$ =0, i.e., the emitter terminals of the two transistors are at (virtually) zero signal potential. Hence each of the left and right halves of the system behaves like a CE amplifier with the emitter returned to signal ground.

The above observation leads to a simplified analysis of differential amplifiers in terms of two single stage half circuits.

2.3.1.3 C: *Differential input resistance* (balanced differential operation)

With the assumption of $r_o$ = infinity for both the transistors, simple observation on Fig.24(c) will lead to the conclusion that $R_{in}|_{\text{bal diff}} = 2r_\pi$ .

2.3.1.3 D: *Single-ended small signal voltage gain*

The associated ac equivalent circuit can be derived from Fig.24(c) and is shown in Fig.25.

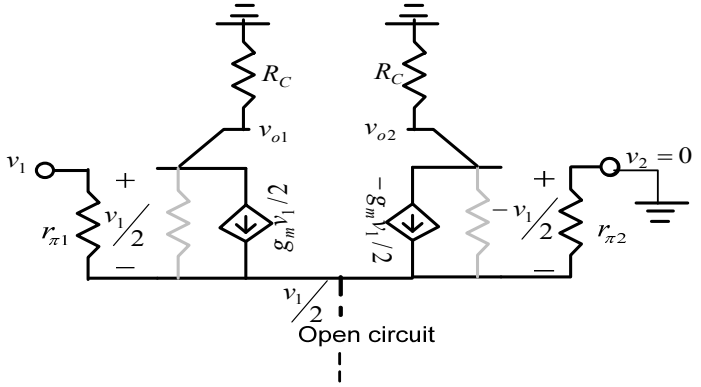



Figure 25: Small signal equivalent circuit for single input operation

Clearly, $v_{o1} = -g_m R_C v1/2$, $v_{o2} = g_m R_C v_1/2$. Then the differential output voltage signal = $v_{o1} - v_{o2}$ $=- g_m R_C v_1$.The voltage gain is then $-g_m R_C$.

2.3.1.3 E: *Common mode voltage gain*

Now we shall consider $v_1=v_2=v_{CM}$. Then $v_3= v_{CM}$ (see eq. 2.3.1.10). In this case, we shall have $v_{o1}$ = $v_{o2}$ = 0. Accordingly, the differential output voltage is zero! Since we are considering identical matched transistors calculating a differential voltage gain with *zero* differential input signal voltage becomes meaningless.

We therefore calculate the single-ended voltage gain, i.e., $v_{o1}/v_{CM}$. We now divide the amplifier into two halves (half circuits) as shown in Fig.26. Each half is like a CE amplifier with un-bypassed resistance in the emitter. The derivation follows. Consider only one half-circuit. KCL at the node of $v_x$ gives

$$-\frac{v_{CM}-v_x}{r_\pi} - g_m(v_{CM}-v_x) + \frac{v_x}{2R_I} = 0 \qquad (2.3.1.12)$$

Solving for $v_x$, we get $$v_x = \frac{2v_{CM}(g_m r_\pi + 1)R_I}{r_\pi + 2R_I(g_m r_\pi + 1)} \qquad (2.3.1.13)$$

The output signal voltage $v_{o1} = -g_m R_C (v_{CM} - v_x) = -\frac{g_m r_\pi R_C v_{CM}}{r_\pi + 2R_I(g_m r_\pi + 1)}$ (2.3.1.14)

Remembering that $g_m r_\pi = \beta, r_\pi = (\beta+1)r_e, (\beta+1)/\beta = 1/\alpha$ , we can finally get the common mode gain $G_{CM} = -v_{o1}/v_{CM} = -\frac{\alpha R_C}{r_e + 2R_I} \approx \frac{\alpha R_C}{2R_I}$. This is approximately same as the voltage gain of a CE BJT amplifier with an un-bypassed emitter resistance of $r_e$ (internal to the transistor) in series with $2R$ (external to the transistor).

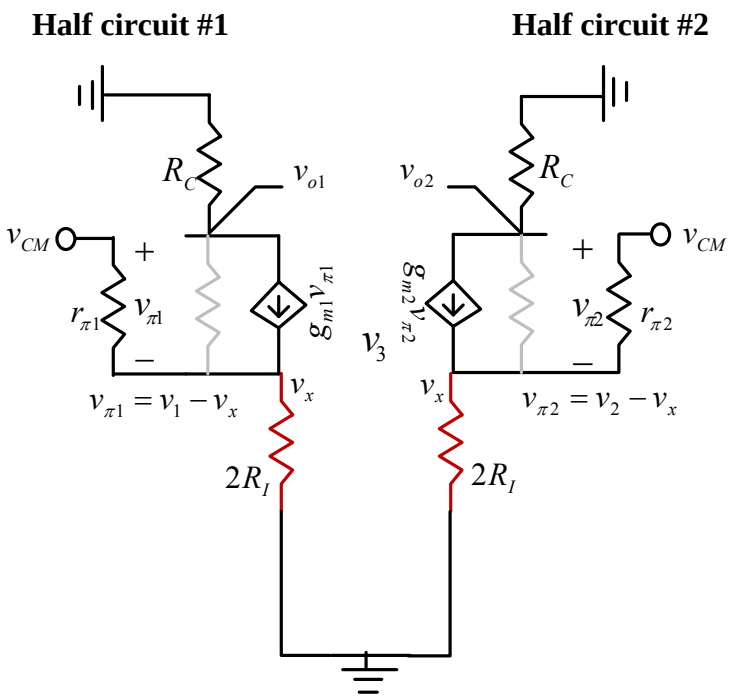



Figure 26: Decomposition of the differential amplifier schematic into two half-circuits.

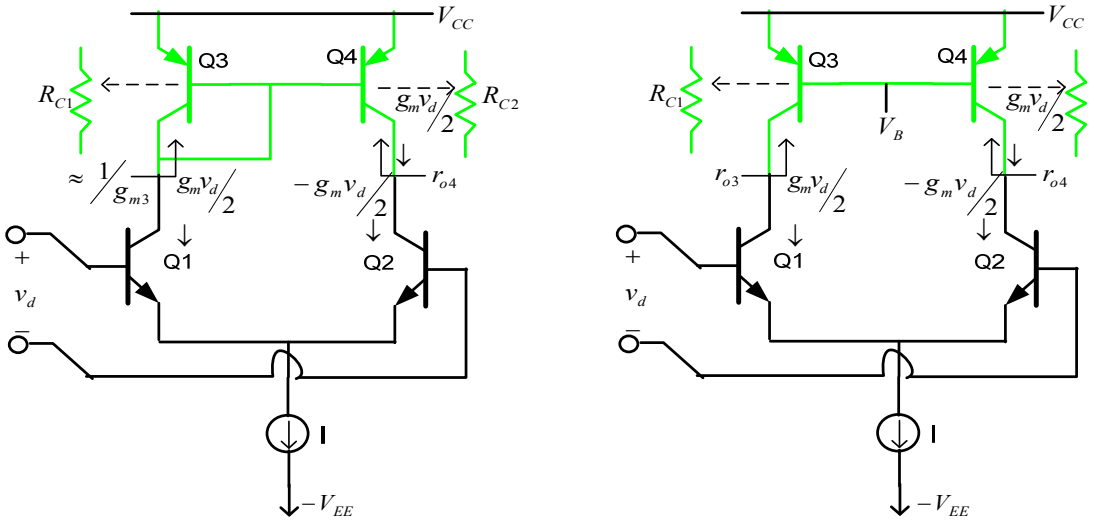
For the balanced differential operation with $v_1=v_d/2$, we would have $v_{o1} = -g_m R_C(v_d/2)$, so that differential voltage gain (for only one input effective) would be $A_d = -g_m R_C/2$.

2.3.1.3 F : *Common mode rejection ratio* (CMRR)

The quality of a differential amplifier is quite often judged by the decibel ratio of the differential gain to the common mode gain. This is referred to as common mode rejection ratio (CMRR). This is then $20\log_{10}(A_d / A_c) = 20\log_{10}(\frac{g_m R_C / 2}{\alpha R_C / 2R}) = 20\log_{10}(\frac{g_m R}{\alpha})$, where $R=R_I$ is the small signal resistance of the bias current source. Typical values of CMRR are between 60 dB to 90 dB.

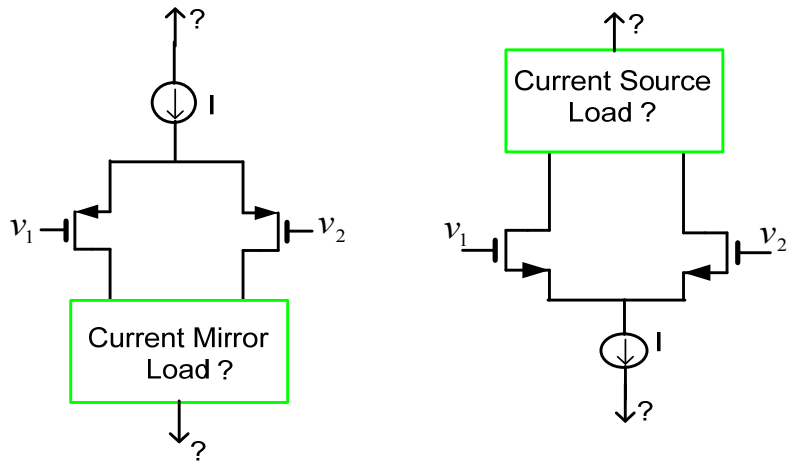
2.3.2 Differential amplifier with active loads

In an integrated circuit environment, discrete resistors are not preferred. Active loads are used instead of the resistors. Depending upon the nature of the output signal, either current mirror load or current source load is used. The two possibilities for BJT based differential amplifiers are shown in figures 27(a)-(b).




(a) (b)

Figure 27: BJT based differential amplifier with active loads; (a) current mirror load, (b) current source load




(a) (b)

Figure 28: MOST-based DA with active loads; (a) current mirror load, (b) current source load.

The student is asked to fill up the details. The body (bulk) terminals of the MOSTs are not shown

Figures 28(a)-(b) depict the MOS transistor (MOST) based differential amplifiers (DA) with current mirror and current source active loads respectively. The student may try to fill up the details using his/her understanding of the active loads.

The MOS or CMOS technology is primarily used now- a- days for integrated circuits and systems. So we can work with a MOST-based DA for signal related analysis or calculations.

For a current mirror based DA, consider figures 29(a) and (b) for the schematic and the associated small signal equivalent circuit respectively. The amplifying devices are NMOS while the active loads are comprised of PMOS transistors.

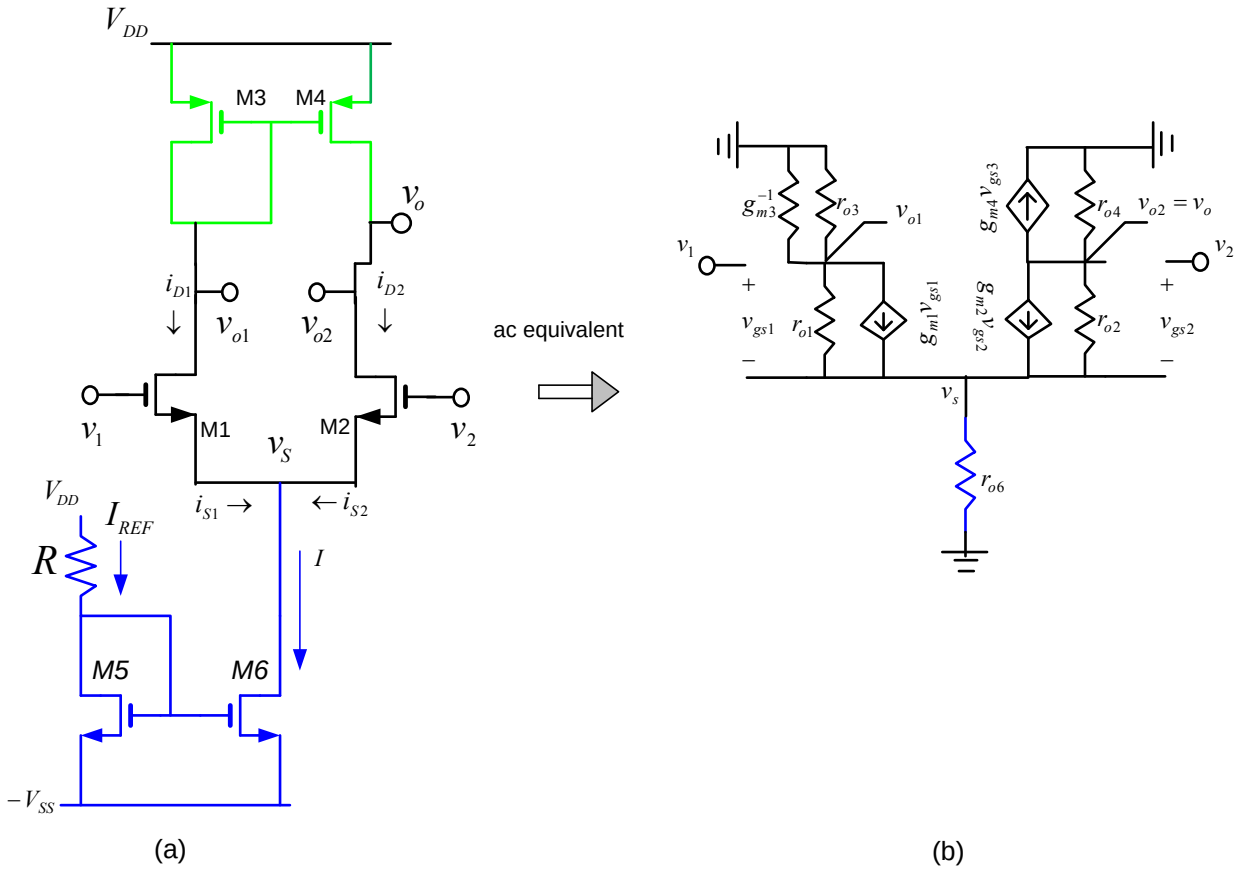



Figure 29: (a) A CMOS DA with current mirror load and current mirror bias current source, (b) ac equivalent circuit at low frequency (i.e., ignoring any parasitic capacitances).

*Analysis*: To begin an approximate analysis, we will introduce several simplifying assumptions. Thus the NMOS transistors M1,M2 are considered matched pair of transistors. So $g_{m1}=g_{m2}=g_{mn}$, $r_{o1}=r_{o2}=r_{dn}$ . Similarly, the PMOS pair M3,M4 are considered matched. So $g_{m3}=g_{m4}=g_{mp}$, and $r_{o3}=r_{04}=r_{dp}$. Let us introduce the conductance parameter $g_{xy}=1/r_{xy}$.

We will then carry out the analysis for *balanced* differential input signals, i.e., $v_1=v_d/2$, $v_2=-v_d/2$. Consequently, $v_s=0$, $v_{gs1}=v_d/2$, $v_{gs2}=-v_d/2$. Further the circuit configuration of the current mirror dictates $v_{gs3}=v_{o1}$

The KCL at $v_{o2}$ node is: $g_{dp}v_{o2} + g_{mp}v_{o1} - g_{mn}\frac{v_d}{2} + g_{dn}v_{o2} = 0$ (2.3.2.1)

The KCL at $v_{o1}$ node is: $g_{dp}v_{o1} + g_{mp}v_{o1} + g_{mn}\frac{v_d}{2} + g_{dn}v_{o1} = 0$ (2.3.2.2)

From (2.3.2.2) $$v_{o1} = \frac{-g_{mn}(v_d/2)}{g_{dp} + g_{mp} + g_{dn}} \quad (2.3.2.3)$$

Substituting for $v_{o1}$ from (2.3.2.3) in (2.3.2.1), we will get

$$v_{o2} = \frac{1}{2}\frac{g_{mn}(2g_{mp} + g_{dp} + g_{dn})}{(g_{dp} + g_{dn})(g_{dp} + g_{dn} + g_{mp})}v_d \quad (2.3.2.4)$$

Considering that in a practical case $g_{mp}$ is >> $g_{dp}$ or $g_{dn}$, and hence ignoring $g_{dn}$+$g_{dp}$ in comparison with $g_{mn}$, (2.3.2.4) simplifies to: $v_{o2} = \frac{g_{mn}}{g_{dp} + g_{dn}}v_d$ (2.3.2.5)

The *differential-in* , *single- out* voltage gain is therefore: $\frac{g_{mn}}{g_{dp} + g_{dn}} = g_{mn} \times r_{on} \,||\, r_{op}$ (2.3.2.6)

In (2.3.2.6), $r_{on}$ =1/$g_{dn}$, $r_{op}$ =1/$g_{dp}$. The expression in (2.3.2.6) is surprisingly similar to the voltage gain expression of a CS- MOST amplifier circuit! So it should be easy to remember. Note that $v_{o2}$ is in phase with $v_d$ with +$v_d$/2 applied at the $v_1$ terminal of the differential amplifier in Fig. 29(a). Similarly, $v_{o2}$ will be 180$^o$ out of phase with $v_2$ (i.e., -$v_d$/2).

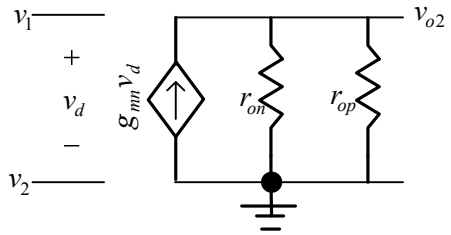



Figure 30: Simple ac equivalent circuit for the differential amplifier in Fig.29(a).

The expression in (2.3.2.6) can be modeled by an ac equivalent circuit as in figure 30. Note that the *input is differential* (i.e., both the terminals are floating, none is grounded), the output is *single-ended* (one of the output terminals is grounded). This is the characteristic of a DA using current mirror as active load, i.e., a *differential input* signal is amplified and delivered as a *single-ended* voltage at the output.

Viewed in another way, we need to *employ a DA with current mirror active load* if conversion *from a differential input* signal *to a single-ended output* signal is desired. For *fully differential* (i.e., differential-in, differential out) operation, the amplifying transistors (such as M1, M2 in Fig.29(a)) are to be used with *current source/sink active load* devices.

The student is suggested to draw up the schematics of

(i) A differential-in, single-out amplifier where PMOS transistors are used as the amplifying devices. That is to say, the PMOS devices receive the input signal.

(ii) A fully differential (i.e., differential-in, differential-out) amplifier with NMOS transistors as the signal amplifiers (i.e., NMOS devices receiving the input signal).

(iii) Repeat (ii) for PMPS transistors as the amplifying devices.

2.3.3 Multi-stage amplifier (MOST and BJT based Operational Amplifier examples)

The student is now fairly familiar with all the basic circuit modules employed in an integrated circuit. It is interesting to see how several such modules are interconnected to produce a versatile integrated circuit amplifier, such as an operational amplifier (OP-AMP).

2.3.3.1: A two-stage MOS operational amplifier (OP-AMP)

Figure 31 depicts the schematic of a two-stage CMOS operational amplifier[1]. Let us calculate the voltage gain that can be afforded by this circuit.

Toward this, we need to know about the bias currents and the characteristics of the devices, such as width ($W$), length ($L$), transconductance factor ($\mu_n C_{ox}$, $\mu_p C_{ox}$), threshold voltages ($V_{THN}$, $V_{THP}$), and the *Early* voltages ($V_{AN}$, $V_{AP}$). Consider the following given information.

*W/L values (Table)*

| Transistor | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | $Q_8$ |
|---|---|---|---|---|---|---|---|---|
| $W/L$ (in $\mu m$) | 20/0.5 | 20/0.5 | 5/0.5 | 5/0.5 | 40/0.5 | 10/0.5 | 40/0.5 | 40/0.5 |

[1] Figure 8.41, *Microelectronic Circuits* by Sedra and Smith, 6th edn., ©2010 , Oxford University Press Inc, ch.8.

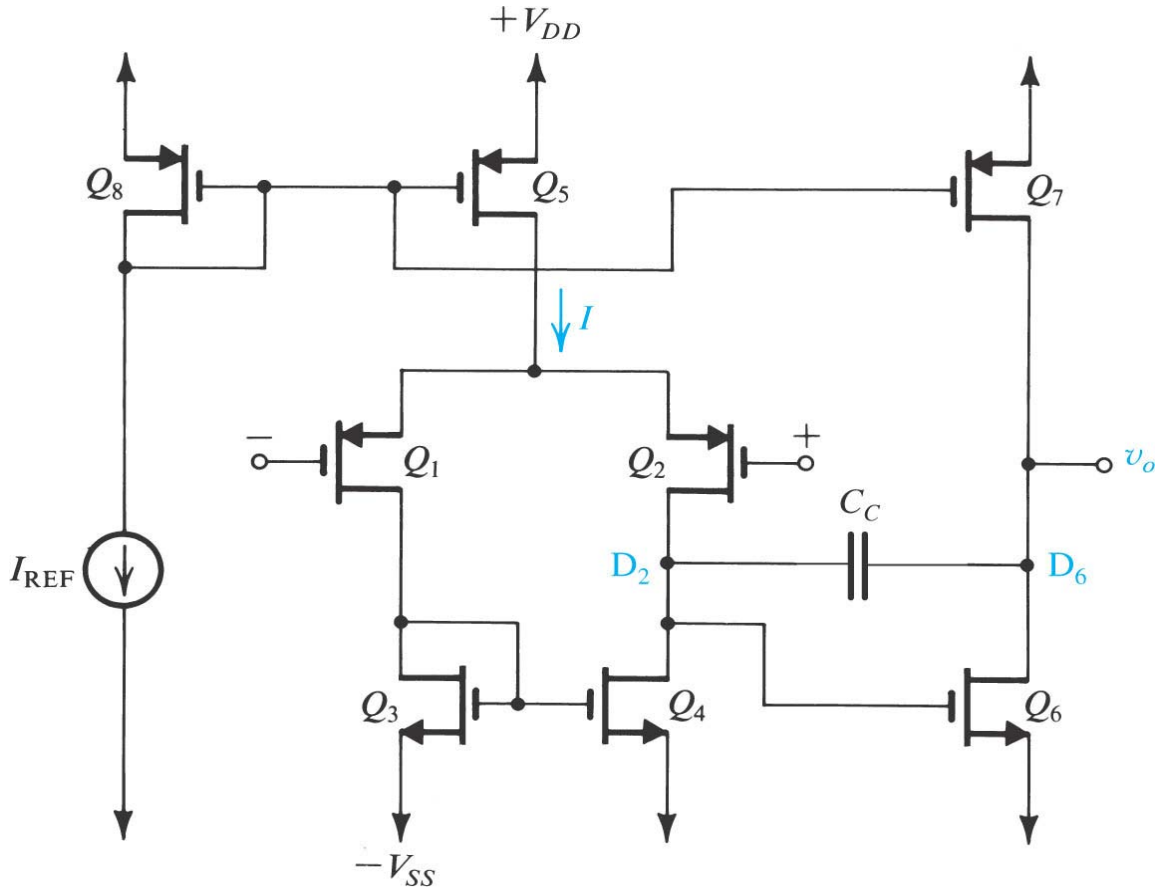



Figure 31: Schematic of a two-stage CMOS operational amplifier

Further, $\mu_n C_{ox}$=200 $\mu A/V^2$, $\mu_p C_{ox}$ =60 $\mu A/V^2$, $V_{THN}$=0.7 V, $V_{THP}$=-0.8 V, $V_{AN}$ =10 V, $V_{AP}$ =12 V, $V_{DD}$ =$V_{SS}$ =1.8 V, and $I_{REF}$ = 120 $\mu A$.

Inspection of Fig.31 reveals that the OP-AMP has a DA as the signal input stage ($Q_1$, $Q_2$). The devices are PMOS transistors. A PMOS current mirror system ($Q_5$, $Q_7$, $Q_8$) *supplies the DC bias* current to the amplifying stages.

The DA has an NMOS current mirror as active load. The stage that follows the DA is an NMOS-CS amplifier ($Q_6$) with a PMOS ($Q_7$) current mirror as *active load.*

The capacitor $C_C$ provides *frequency compensation* to ensure stable operation of the OP-AMP when connected in a negative-feedback for signal processing. The concept of frequency compensation will be discussed in chapter 3 of this note-pack.

Since the voltage gain depends upon $g_m$ of the signal-driven transistor(s) and the output resistances of the signal-driven transistor and of the transistor forming the active load (i.e., $r_{op}$, $r_{on}$), we need to find the pertinent $g_m$ values (i.e., of $Q_1$,$Q_2$,$Q_6$ –these are driven by the signal),and the output resistances of $Q_2$, $Q_4$, $Q_6$, and $Q_7$. The $g_m$ and output resistance values depend upon the

DC bias current. So we need to find the bias currents through the different stages (a stage is a column of transistors in the schematic).

Thus, considering that $Q_8$, $Q_5$ and $Q_7$ form current mirrors and that the *W/L* values for these are identical ( see the Table) we conclude that $I_5=I_7=I_{REF}=120\ \mu A$.

Since $I_5$ divides equally between $Q_1$ and $Q_2$, we can determine $I_1=I_2=I_{REF}/2=60\ \mu A$. Since $Q_3$ is in series with $Q_1$, and likewise $Q_4$ is with $Q_2$, we know $I_3=I_4=I_1=I_2=60\ \mu A$. Similarly, $I_6=I_7=120\ \mu A$.

Using the square-law equation for the drain current in the MOST, i.e., $I_D=(1/2)\mu C_{ox}(W/L)V_{ov}^2$, where $V_{ov}=|V_{GS}|-|V_{TH}|$, we can determine the following quantities

For $Q_1$, $Q_2$ :

$I_D$=120/2 μA, $\mu_n C_{ox}$=200 $\mu A/V^2$ (for NMOS), *W*/L = 20/0.5, $V_{OV}$ =0.122 V.

Further, since the transconductance $g_m=\partial I_D/\partial V_{OV}=2I_D/V_{OV}$, we get $g_{mQ1}=g_{mQ2}=9.836\times10^{-4}$ mho.

For $Q_2$,$Q_4$ :

The output resistances are dependent upon the *Early* voltage and DC bias current. Thus, $r_{o2}=V_{AN}/I_{DQ2}$ =166.67 *k*Ω. Similarly, $r_{o4}=V_{AP}/I_{DQ4}$ =200 *k*Ω.

Then signal voltage gain of stage#1 (i.e., $Q_2$, $Q_4$ pair) is $-g_{mQ2}\times r_{o2}\,||\,r_{o4}$ = -89.42 V/V

For $Q_6$, $Q_7$ :

$I_{DQ7}$= 120 $\mu A$ (by current mirroring principle, and since $(W/L)_{Q7}=(W/L)_{Q8}$ ).

Also, $I_{DQ6}$ = 120 $\mu A$ (since $Q_6$, $Q_7$ are in series).

For $Q_6$ , $V_{OV}$ =0.245 V, $g_{mQ6}=9.796\times10^{-4}$ , $r_{o6}$ =83.33 *k*Ω.

For $Q_7$ , $r_{07}$ =100 *k*Ω.

The signal voltage gain of stage#2 (i.e., $Q_6$ , $Q_7$ pair) is $-g_{mQ6}\times r_{o6}\,||\,r_{o7}$ = -44.53 V/V

Overall voltage gain of the two stage OP-AMP= $-89.42\times(-44.53)$=3989.92 V/V.

The above serves as an example to calculate the voltage gains in a cascade of multi-stage MOS amplifiers. The above gain is the gain of the two- stage OP-AMP as depicted in Figure 31.

The voltage gain is not the only parameter of interest for an OP-AMP. Several other performance characteristics, such as: (i) offset voltage, offset current, -3dB bandwidth, unity-gain bandwidth, CMRR, slew rate, settling time, power supply rejection ratio (PSRR), input common mode range (CMR), total DC power consumption, harmonic distortion, noise figure etc., are important. Interested students are

encouraged to read more advanced books[2] and or take a course on, for example, *introduction to analog VLSI*.

2.3.3.2: MOS based Operational Amplifier ( a second example)[3]

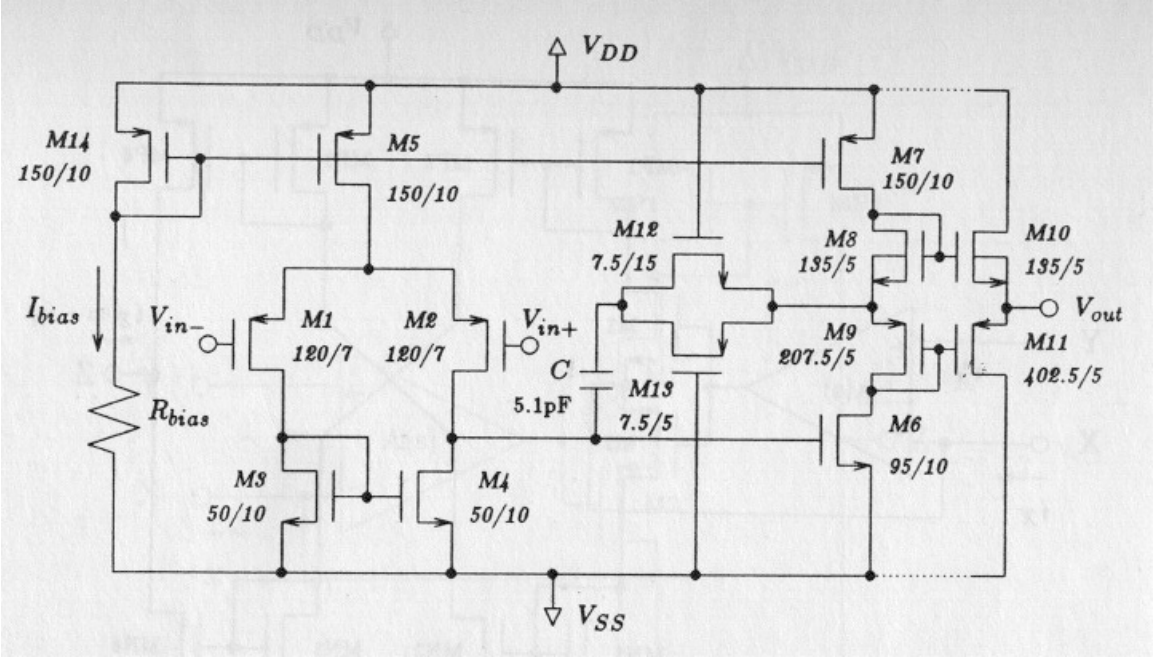



Figure 32: A CMOS OP-AMP with a class AB output stage.

*Discussion:* Figure 32 presents a three-stage OP-AMP including a class AB output stage. The output stage offers a low output impedance – an important criterion for a voltage amplifier (i.e., VCVS).

The input DA is comprised of two PMOS transistors (M1,M2), with PMOS current mirror (M14,M5) bias source and NMOS (M3,M4) current mirror (active) load.

The capacitor C together with transistors M12, M13 form a series C,R frequency compensation circuit.

[2] See the list at the end of this chapter

[3] *Analog IC design: the current-mode approach,* Edited by C. Toumazou, F.J. Lidgey & D.G. Haigh © April 1990: Peter Peregrinus Ltd., London, United Kingdom, ISBN 0 86341 215 7

The second stage of amplification comes from the NMOS transistor M6 which has an active load comprised of the diode connected transistors (M8,M9) in series with the current mirror load (M7).

Transistors M10 (NMOS), M11 (PMOS) together with the diode connected transistors (M8,M9) from a class AB output stage. Since the output is taken from the source terminals of M10, M11, the output resistance will be small.

The *W*/*L* data shown are in microns.

2.3.3.3: BJT based OP-AMP

Please refer to *Microelectronic Circuits* by Sedra and Smith, 6th edn., ©2010 , Oxford University Press Inc, ch.8, p.657-663.

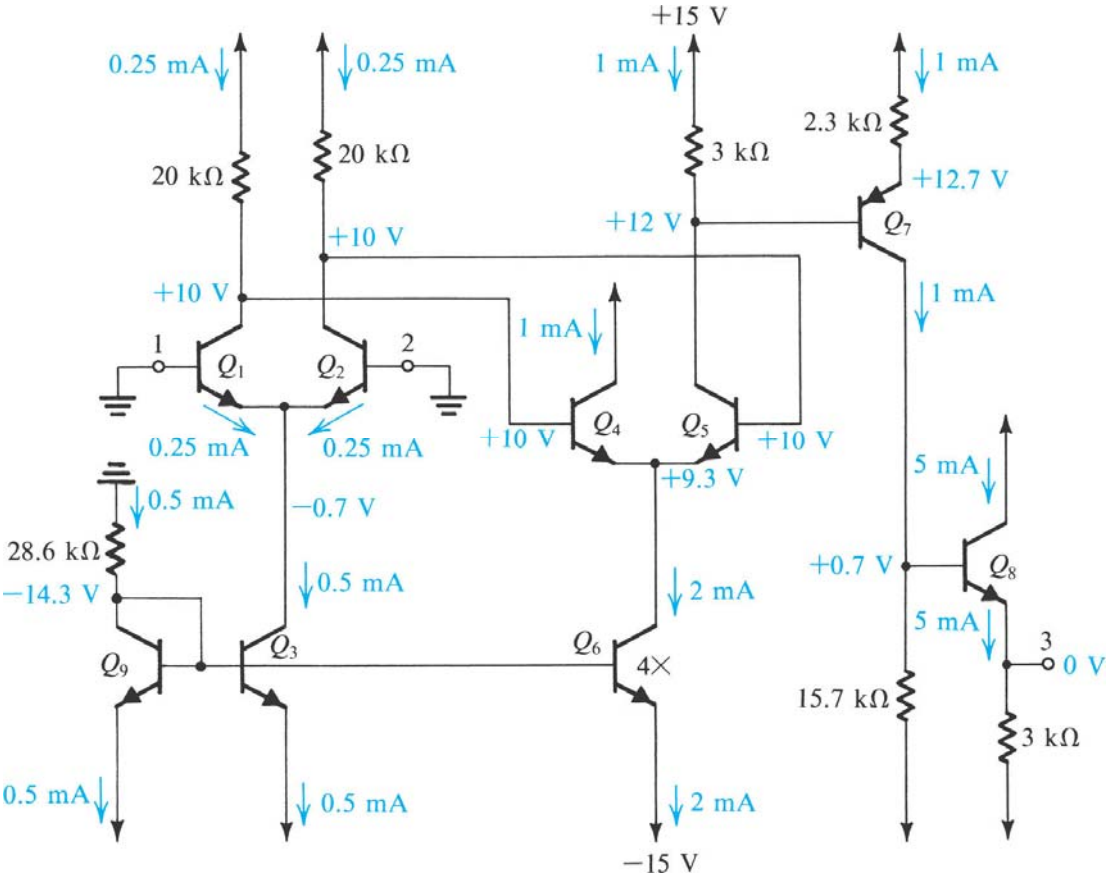
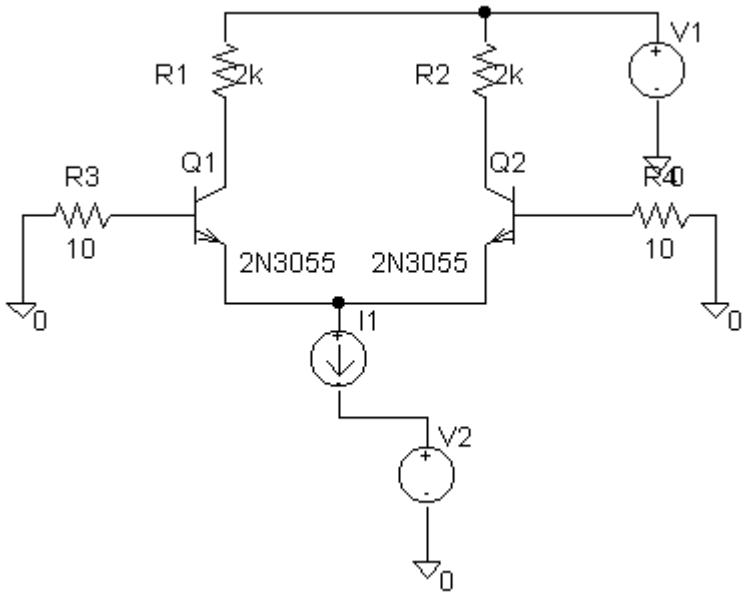



Figure 33: A four-stage BJT OP-AMP

For analyzing the circuit operation, and calculating the voltage gain and input/output resistances, please read ref#1, p.657-663.

## 2.4 : Practice Exercises

Q.1: Consider the schematic of a differential amplifier below. The output listing for the network in pSPICE format is appended. Using this listing do the following:




- Draw an ac equivalent circuit model for the amplifier.
- Using necessary theoretical formula and the relevant component values from the output listing, find the (a) voltage gain, and (b) input resistance for small signal operation.

* Schematics Netlist *

R_R1 $N_0002 $N_0001 2k
R_R2 $N_0003 $N_0001 2k
V_V1 $N_0001 0 DC 5
V_V2 $N_0004 0 DC -5

Q_Q1 $N_0002 $N_0005 $N_0006 Q2N3055

R_R4 $N_0007 0 10

R_R3 0 $N_0005 10

Q_Q2 $N_0003 $N_0007 $N_0006 Q2N3055

I_I1 $N_0006 $N_0004 DC 5m

SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

**********

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) 5.0000 ($N_0002) .1730

($N_0003) .1730 ($N_0004) -5.0000

($N_0005)-864.9E-06 ($N_0006) -.5602

($N_0007)-864.9E-06

VOLTAGE SOURCE CURRENTS

NAME CURRENT

V_V1 -4.827E-03

V_V2 5.000E-03

TOTAL POWER DISSIPATION 4.91E-02 WATTS

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**** 12/31/103 11:09:01 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\pe_el312lect_ch2.sch

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

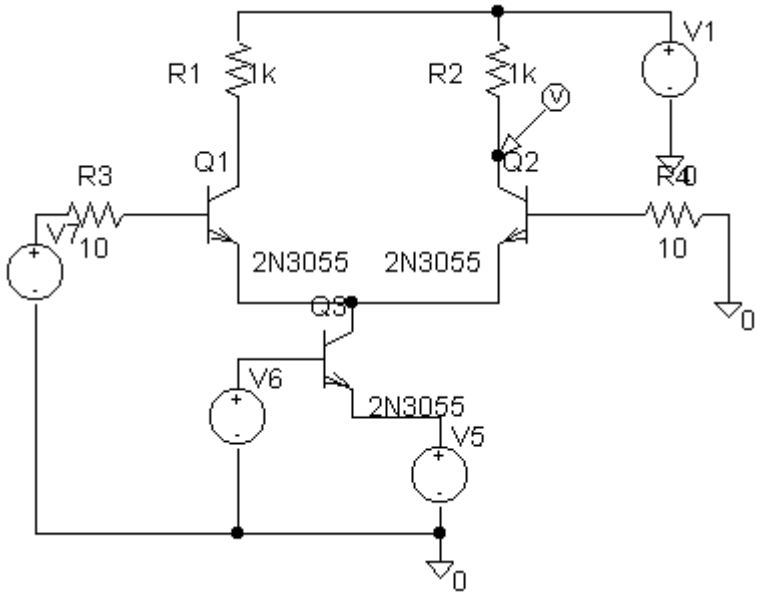
**********

**** BIPOLAR JUNCTION TRANSISTORS

| NAME | Q_Q1 | Q_Q2 |
|---|---|---|
| MODEL | Q2N3055 | Q2N3055 |
| IB | 8.65E-05 | 8.65E-05 |
| IC | 2.41E-03 | 2.41E-03 |
| VBE | 5.59E-01 | 5.59E-01 |
| VBC | -1.74E-01 | -1.74E-01 |
| VCE | 7.33E-01 | 7.33E-01 |
| BETADC | 2.79E+01 | 2.79E+01 |
| GM | 9.32E-02 | 9.32E-02 |
| RPI | 4.59E+02 | 4.59E+02 |
| RX | 1.00E-01 | 1.00E-01 |
| RO | 2.08E+04 | 2.08E+04 |
| CBE | 4.48E-09 | 4.48E-09 |

| | | |
|---|---|---|
| CBC | 2.58E-10 | 2.58E-10 |
| CJS | 0.00E+00 | 0.00E+00 |
| BETAAC | 4.28E+01 | 4.28E+01 |
| CBX | 0.00E+00 | 0.00E+00 |
| FT | 3.13E+06 | 3.13E+06 |

Q.2: For the network below, the output listing is appended. Repeat the work done in Q.1 above.




* Schematics Netlist *

| | |
|---|---|
| Q_Q1 | $N_0002 $N_0001 $N_0003 Q2N3055 |
| R_R4 | $N_0004 0 10 |
| Q_Q3 | $N_0003 $N_0005 $N_0006 Q2N3055 |
| R_R1 | $N_0002 $N_0007 1k |
| V_V1 | $N_0007 0 DC 5 |

R_R3 $N_0008 $N_0001 10

R_R2 $N_0009 $N_0007 1k

V_V5 $N_0006 0 DC -5

V_V6 $N_0005 0 DC -4.4295

V_V7 $N_0008 0 DC 0 AC 1

Q_Q2 $N_0009 $N_0004 $N_0003 Q2N3055

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

**********

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001)-719.5E-06 ($N_0002) 3.0812

($N_0003) -.5527 ($N_0004)-719.5E-06

($N_0005) -4.4295 ($N_0006) -5.0000

($N_0007) 5.0000 ($N_0008) 0.0000

($N_0009) 3.0812

VOLTAGE SOURCE CURRENTS

NAME CURRENT

V_V1 -3.838E-03

V_V5 4.096E-03

V_V6 -1.149E-04

V_V7 -7.195E-05

TOTAL POWER DISSIPATION 3.92E-02 WATTS

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**** 12/31/103 11:42:49 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\pe_el312lect_ch2_2.sch

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**********

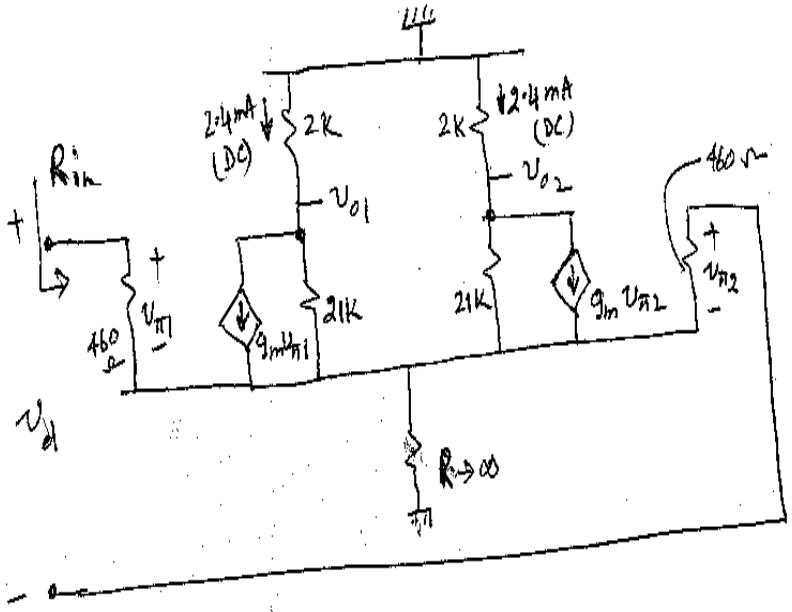
**** BIPOLAR JUNCTION TRANSISTORS

NAME Q_Q1 Q_Q3 Q_Q2

MODEL Q2N3055 Q2N3055 Q2N3055

| | | | |
|---|---|---|---|
| IB | 7.19E-05 | 1.15E-04 | 7.19E-05 |
| IC | 1.92E-03 | 3.98E-03 | 1.92E-03 |
| VBE | 5.52E-01 | 5.71E-01 | 5.52E-01 |
| VBC | -3.08E+00 | -3.88E+00 | -3.08E+00 |
| VCE | 3.63E+00 | 4.45E+00 | 3.63E+00 |
| BETADC | 2.67E+01 | 3.46E+01 | 2.67E+01 |
| GM | 7.41E-02 | 1.54E-01 | 7.41E-02 |
| RPI | 5.64E+02 | 3.35E+02 | 5.64E+02 |
| RX | 1.00E-01 | 1.00E-01 | 1.00E-01 |
| RO | 2.77E+04 | 1.35E+04 | 2.77E+04 |
| CBE | 3.73E-09 | 6.86E-09 | 3.73E-09 |
| CBC | 1.60E-10 | 1.51E-10 | 1.60E-10 |
| CJS | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| BETAAC | 4.18E+01 | 5.15E+01 | 4.18E+01 |
| CBX | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| FT | 3.03E+06 | 3.49E+06 | 3.03E+06 |

* Q3: The ac equivalent circuit of a BJT differential amplifier is shown below. Determine the input impedance and differential voltage gain $(v_{o1}-v_{o2})/v_d$




Given

$h_{fe} = 43$

$g_m = \frac{I_{DC}}{V_T}$

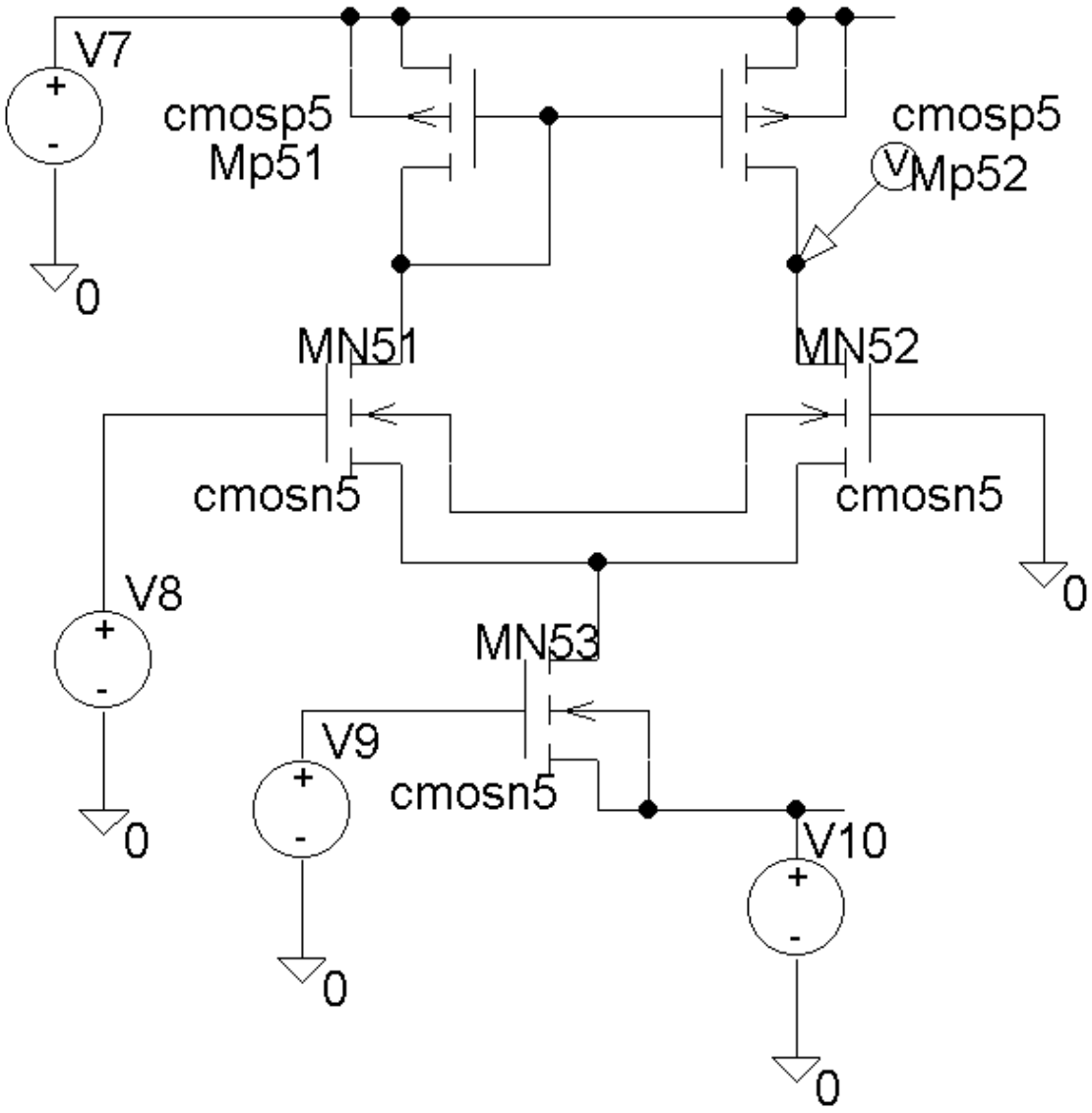
$V_T = \frac{kT}{q} \simeq 25mV$ at room temperature.

Q4 Repeat Q3 when R = 14KΩ

Q.5: Deleted

Q.6: Consider the schematic and the output file listing for the differential amplifier shown below.

- Draw the ac equivalent circuit for the amplifier using standard symbols (i.e., $g_m$, $r_{ds}$ ..)
- Estimate the voltage gain of the amplifier using the data form the output listing and relevant formula learned in your lecture class. The output node is where the voltage probe is attached.




**** INCLUDING CMR_study.net ****

* Schematics Netlist *

M_Mp51 $N_0001 $N_0001 $N_0002 $N_0002 cmosp5

+ L=2u

+ W=18u

M_Mp52 $N_0003 $N_0001 $N_0002 $N_0002 cmosp5

+ L=2u

+ W=18u

```
M_MN51        $N_0001 $N_0005 $N_0004 $N_0006 cmosn5
+ L=2u
+ W=5u
M_MN52        $N_0003 0 $N_0004 $N_0006 cmosn5
+ L=2u
+ W=5u
M_MN53        $N_0004 $N_0008 $N_0007 $N_0007 cmosn5
+ L=2u
+ W=10u
V_V10         $N_0007 0 DC -1.5
V_V9        $N_0008 0 DC -.5
V_V7        $N_0002 0 DC 1.5
V_V8        $N_0005 0 DC 0 AC 1


****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C
********************************************************************************
 NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE    NODE   VOLTAGE
($N_0001)     .2325              ($N_0002)    1.5000

($N_0003)     .2325              ($N_0004)    -.9651

($N_0005)    0.0000              ($N_0006)    -.8457

($N_0007)   -1.5000              ($N_0008)    -.5000

    VOLTAGE SOURCE CURRENTS
    NAME        CURRENT

    V_V10       4.951E-05
    V_V9        0.000E+00
```

V_V7 -4.951E-05

V_V8 0.000E+00

TOTAL POWER DISSIPATION 1.49E-04 WATTS

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**** 01/02/104 09:58:50 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

* F:\Msim_8\Projects\Teaching\CMR_study.sch

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

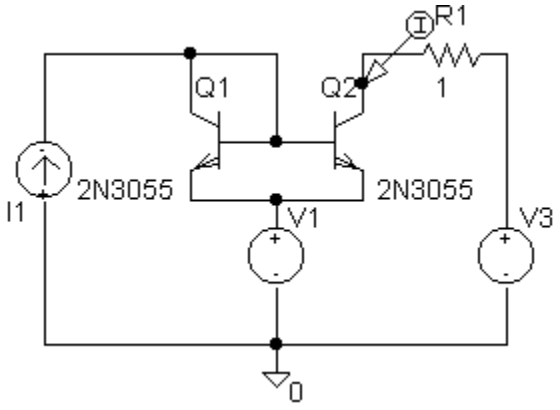
**********

**** MOSFETS

| NAME | M_Mp51 | M_Mp52 | M_MN51 | M_MN52 | M_MN53 |
|---|---|---|---|---|---|
| MODEL | cmosp5 | cmosp5 | cmosn5 | cmosn5 | cmosn5 |
| ID | -2.48E-05 | -2.48E-05 | 2.48E-05 | 2.48E-05 | 4.95E-05 |
| VGS | -1.27E+00 | -1.27E+00 | 9.65E-01 | 9.65E-01 | 1.00E+00 |
| VDS | -1.27E+00 | -1.27E+00 | 1.20E+00 | 1.20E+00 | 5.35E-01 |
| VBS | 0.00E+00 | 0.00E+00 | 1.19E-01 | 1.19E-01 | 0.00E+00 |
| VTH | -9.43E-01 | -9.43E-01 | 6.46E-01 | 6.46E-01 | 6.82E-01 |
| VDSAT | -3.20E-01 | -3.20E-01 | 2.96E-01 | 2.96E-01 | 2.99E-01 |
| GM | 1.31E-04 | 1.31E-04 | 1.29E-04 | 1.29E-04 | 2.59E-04 |
| GDS | 1.10E-07 | 1.10E-07 | 2.46E-07 | 2.46E-07 | 5.42E-07 |
| GMB | 3.28E-05 | 3.28E-05 | 3.68E-05 | 3.68E-05 | 8.62E-05 |
| CBD | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| CBS | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| CGSOV | 4.31E-15 | 4.31E-15 | 1.53E-15 | 1.53E-15 | 3.05E-15 |

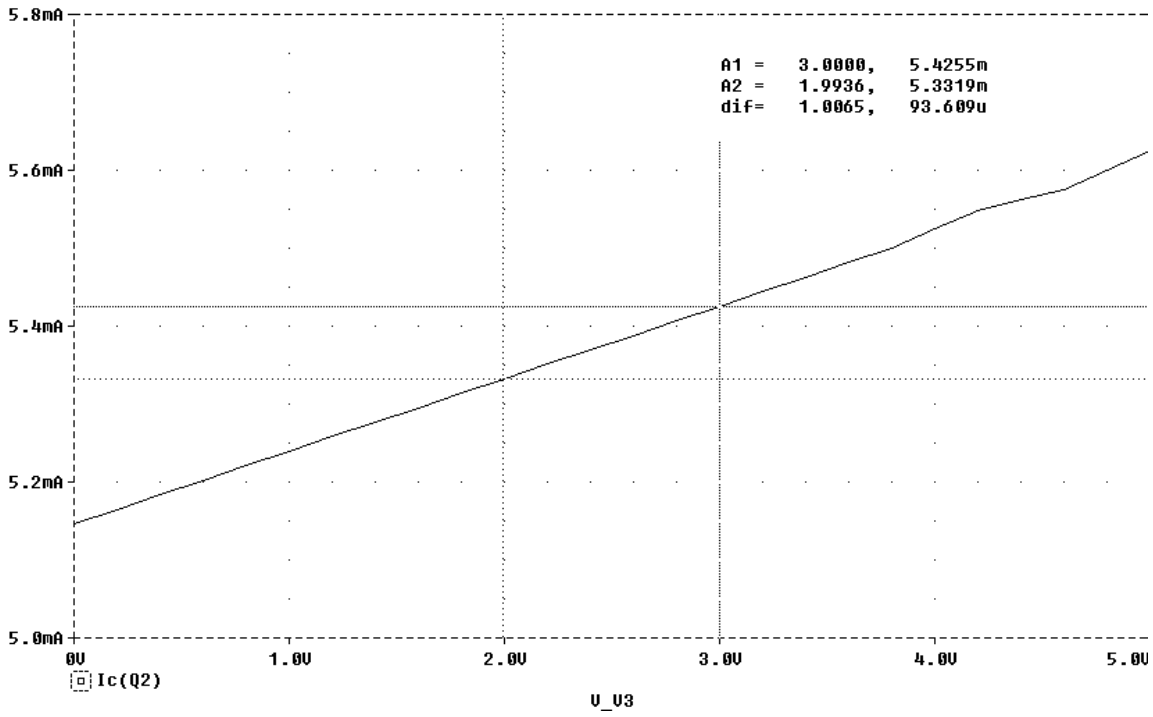
| | | | | | |
|---|---|---|---|---|---|
| CGDOV | 4.31E-15 | 4.31E-15 | 1.53E-15 | 1.53E-15 | 3.05E-15 |
| CGBOV | 7.25E-16 | 7.25E-16 | 7.67E-16 | 7.67E-16 | 7.67E-16 |
| CGS | 8.33E-14 | 8.33E-14 | 2.28E-14 | 2.28E-14 | 4.57E-14 |
| CGD | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| CGB | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 | 0.00E+00 |

Q.7: The figure below shows a BJT-based simple current mirror. The DC bias current in Q1 is 5 mA. The schematic represents a test set up to measure the output impedance of




Basic current mirror

the current mirror. The relevant graphical behavior is shown below. The Y-axis is the current into the collector pin of Q2 (the output transistor). What is the output resistance of this mirror?




Q.8: The simulation result for the above current mirror is appended below. What is the expected output resistance for the mirror? Use the pertinent data for the transistors to determine the output resistance. Compare this with the value you get from the above graph.

* Schematics Netlist *

I_I1 0 $N_0001 DC 5m
Q_Q1 $N_0001 $N_0001 $N_0002 Q2N3055
V_V1 $N_0002 0 DC -5
Q_Q2 $N_0003 $N_0001 $N_0002 Q2N3055
V_V3 $N_0004 0 DC 5
R_R1 $N_0003 $N_0004 1

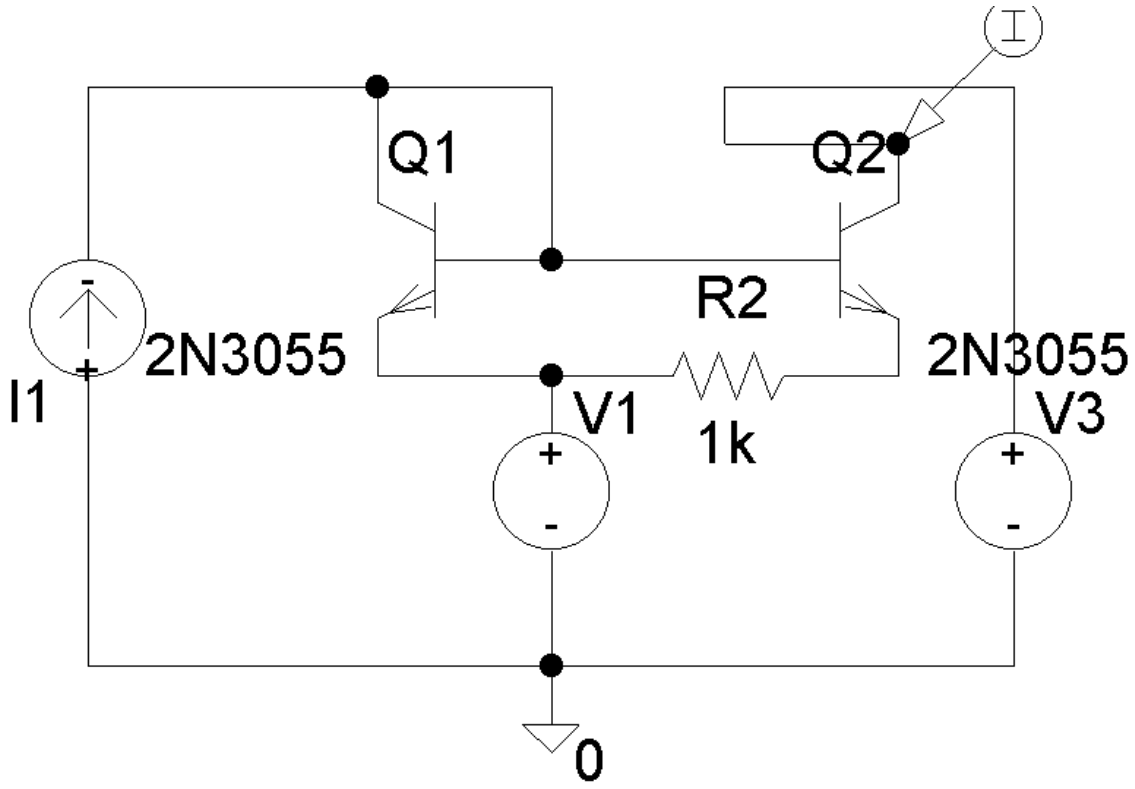
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

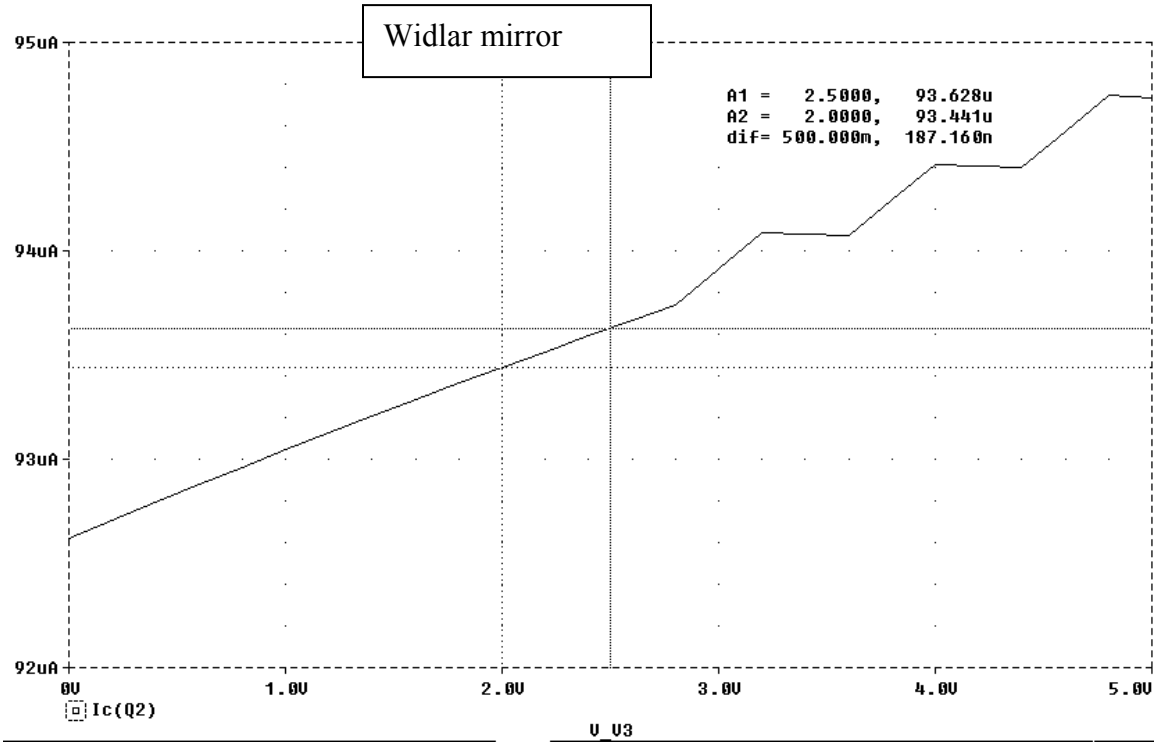
**********

**** BIPOLAR JUNCTION TRANSISTORS

| NAME | Q_Q1 | Q_Q2 |
|---|---|---|
| MODEL | Q2N3055 | Q2N3055 |
| IB | 1.36E-04 | 1.36E-04 |
| IC | 4.73E-03 | 5.62E-03 |
| VBE | 5.77E-01 | 5.77E-01 |
| VBC | 0.00E+00 | -9.42E+00 |
| VCE | 5.77E-01 | 9.99E+00 |
| BETADC | 3.48E+01 | 4.14E+01 |
| GM | 1.83E-01 | 2.17E-01 |
| RPI | 2.78E+02 | 2.78E+02 |
| RX | 1.00E-01 | 1.00E-01 |
| RO | 1.06E+04 | 1.06E+04 |
| CBE | 7.99E-09 | 9.33E-09 |
| CBC | 2.76E-10 | 1.16E-10 |
| CJS | 0.00E+00 | 0.00E+00 |
| BETAAC | 5.07E+01 | 6.03E+01 |
| CBX | 0.00E+00 | 0.00E+00 |
| FT | 3.52E+06 | 3.65E+06 |

Q.9: For the Widlar mirror below, the output current voltage characteristic is shown in the accompanying graph. Determine the output resistance.


Q1
Q2
R2
2N3055
2N3055
I1
V1
1k
V3
0


Widlar mirror
95uA
94uA
93uA
92uA
A1 = 2.5000, 93.628u
A2 = 2.0000, 93.441u
dif= 500.000m, 187.160n
0V
1.0V
2.0V
3.0V
4.0V
5.0V
Ic(Q2)
V_V3

Q.10: The simulated output listing for the above mirror is attached below. Use necessary formula and the relevant data to calculate the $R_{out}$. Compare with the value obtained from the graph.

Schematics Netlist *

```
Q_Q1        $N_0001 $N_0001 $N_0002 Q2N3055
V_V3        $N_0003 0 DC 5
V_V1        $N_0002 0 DC -5
R_R2        $N_0002 $N_0004  1k
Q_Q2        $N_0003 $N_0001 $N_0004 Q2N3055
I_I1        0 $N_0001 DC 5m
```

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

**********

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) -4.4225 ($N_0002) -5.0000

($N_0003) 5.0000 ($N_0004) -4.8937

VOLTAGE SOURCE CURRENTS

NAME CURRENT

V_V3 -9.473E-05

V_V1 5.095E-03

TOTAL POWER DISSIPATION 2.59E-02 WATTS

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**** 01/03/104 10:06:09 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

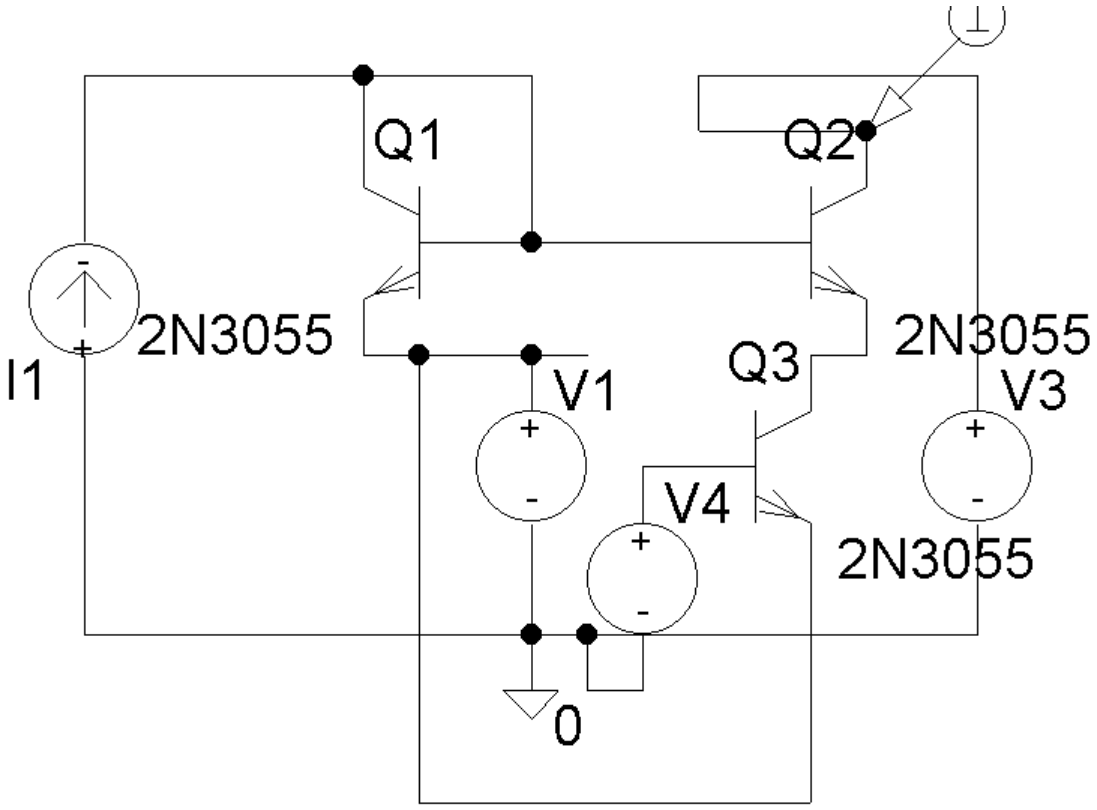
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**********

**** BIPOLAR JUNCTION TRANSISTORS

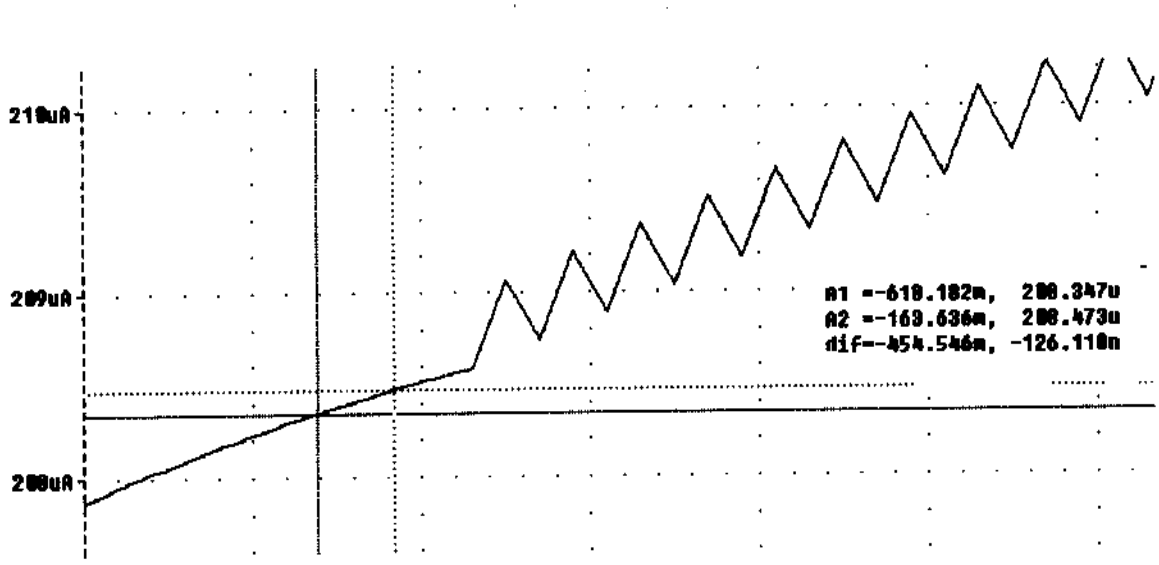
| NAME | Q_Q1 | Q_Q2 |
|---|---|---|
| MODEL | Q2N3055 | Q2N3055 |
| IB | 1.38E-04 | 1.16E-05 |
| IC | 4.85E-03 | 9.47E-05 |
| VBE | 5.78E-01 | 4.71E-01 |
| VBC | 0.00E+00 | -9.42E+00 |
| VCE | 5.78E-01 | 9.89E+00 |
| BETADC | 3.51E+01 | 8.19E+00 |
| GM | 1.87E-01 | 3.66E-03 |
| RPI | 2.73E+02 | 4.07E+03 |
| RX | 1.00E-01 | 1.00E-01 |
| RO | 1.03E+04 | 6.27E+05 |
| CBE | 8.17E-09 | 9.22E-10 |
| CBC | 2.76E-10 | 1.16E-10 |
| CJS | 0.00E+00 | 0.00E+00 |
| BETAAC | 5.10E+01 | 1.49E+01 |
| CBX | 0.00E+00 | 0.00E+00 |
| FT | 3.53E+06 | 5.62E+05 |

Q.11 In order to enhance the output resistance of the Widlar mirror, the resistance R2 is replaced by a BJT device as shown below. Draw the ac equivalent circuit for the modifier current mirror. Label the circuit components clearly.




The output I-V characteristic is shown below. Determine the output resistance and compare with the value predicted by the theoretical formula.

You have to use the component values given in the output listing.



* Schematics Netlist *

```
Q_Q1        $N_0001 $N_0001 $N_0002 Q2N3055
V_V3        $N_0003 0 DC 5
V_V1        $N_0002 0 DC -5
I_I1        0 $N_0001 DC 5m
Q_Q2        $N_0003 $N_0001 $N_0004 Q2N3055
Q_Q3        $N_0004 $N_0005 $N_0002 Q2N3055
V_V4        $N_0005 0 DC -4.5
```

SMALL SIGNAL BIAS SOLUTION  TEMPERATURE =  27.000 DEG C

**********

| NODE | VOLTAGE | NODE | VOLTAGE | NODE | VOLTAGE | NODE | VOLTAGE |
|---|---|---|---|---|---|---|---|
| ($N_0001) | -4.4225 | ($N_0002) | -5.0000 | | | | |
| ($N_0003) | 5.0000 | ($N_0004) | -4.9144 | | | | |
| ($N_0005) | -4.5000 | | | | | | |

VOLTAGE SOURCE CURRENTS

| NAME | CURRENT |
|---|---|
| V_V3 | -2.105E-04 |
| V_V1 | 5.235E-03 |
| V_V4 | -2.453E-05 |

TOTAL POWER DISSIPATION  2.71E-02  WATTS

_**** 01/03/104 10:33:30 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**********

**** BIPOLAR JUNCTION TRANSISTORS

| NAME | Q_Q1 | Q_Q2 | Q_Q3 |
|---|---|---|---|
| MODEL | Q2N3055 | Q2N3055 | Q2N3055 |
| IB | 1.38E-04 | 1.80E-05 | 2.45E-05 |
| IC | 4.84E-03 | 2.10E-04 | 2.29E-04 |
| VBE | 5.78E-01 | 4.92E-01 | 5.00E-01 |
| VBC | 0.00E+00 | -9.42E+00 | 4.14E-01 |
| VCE | 5.78E-01 | 9.91E+00 | 8.56E-02 |
| BETADC | 3.51E+01 | 1.17E+01 | 9.32E+00 |
| GM | 1.87E-01 | 8.13E-03 | 8.95E-03 |
| RPI | 2.73E+02 | 2.55E+03 | 2.11E+03 |
| RX | 1.00E-01 | 1.00E-01 | 1.00E-01 |
| RO | 1.03E+04 | 2.82E+05 | 2.91E+03 |
| CBE | 8.16E-09 | 1.11E-09 | 1.16E-09 |
| CBC | 2.76E-10 | 1.16E-10 | 6.93E-10 |
| CJS | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| BETAAC | 5.10E+01 | 2.07E+01 | 1.89E+01 |
| CBX | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| FT | 3.53E+06 | 1.06E+06 | 7.69E+05 |

Q.12: By a mistake the bias voltage at the base of Q3 was altered from –4.5 V to –4.4 V. What effect will this have in the output resistance of the current mirror? The simulation output listing is attached below. Calculate the output resistance and compare it with the value found in Q.11 above. Discuss your results.

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

**********

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

($N_0001) -4.4229 ($N_0002) -5.0000

($N_0003) 5.0000 ($N_0004) -4.9837

($N_0005) -4.4000

VOLTAGE SOURCE CURRENTS
NAME CURRENT

V_V3 -3.024E-03
V_V1 1.038E-02
V_V4 -2.352E-03

TOTAL POWER DISSIPATION 5.67E-02 WATTS

**** 01/03/104 10:51:17 **** Win95 PSpice 8.0 (July 1997) ***** ID# 95827 ****

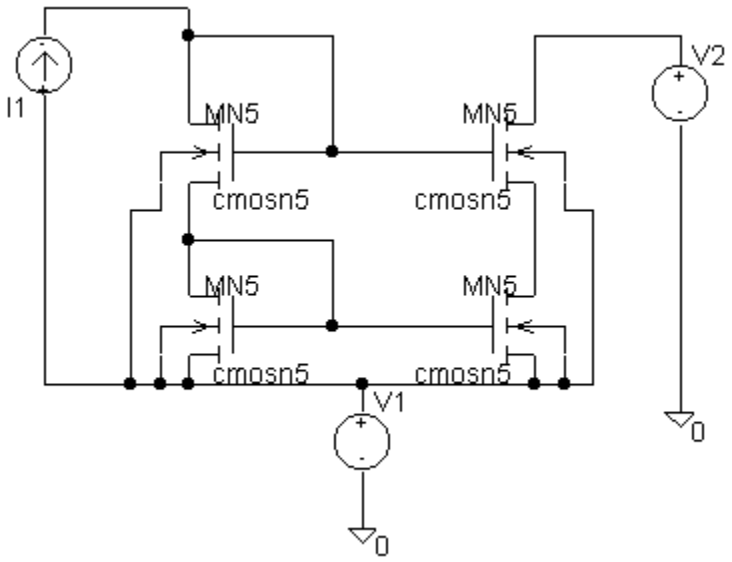
**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

**********

**** BIPOLAR JUNCTION TRANSISTORS

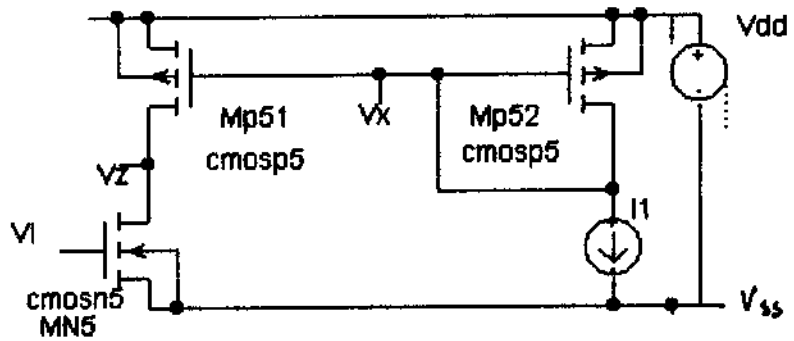
| NAME | Q_Q1 | Q_Q2 | Q_Q3 |
|---|---|---|---|
| MODEL | Q2N3055 | Q2N3055 | Q2N3055 |
| IB | 1.37E-04 | 8.97E-05 | 2.35E-03 |
| IC | 4.77E-03 | 3.02E-03 | 3.11E-03 |
| VBE | 5.77E-01 | 5.61E-01 | 6.00E-01 |
| VBC | 0.00E+00 | -9.42E+00 | 5.84E-01 |
| VCE | 5.77E-01 | 9.98E+00 | 1.63E-02 |
| BETADC | 3.49E+01 | 3.37E+01 | 1.32E+00 |
| GM | 1.84E-01 | 1.17E-01 | 2.01E-01 |
| RPI | 2.76E+02 | 4.41E+02 | 1.38E+02 |
| RX | 1.00E-01 | 1.00E-01 | 1.00E-01 |
| RO | 1.05E+04 | 1.97E+04 | 4.24E+00 |
| CBE | 8.06E-09 | 5.41E-09 | 1.79E-08 |
| CBC | 2.76E-10 | 1.16E-10 | 2.33E-07 |
| CJS | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| BETAAC | 5.08E+01 | 5.15E+01 | 2.78E+01 |
| CBX | 0.00E+00 | 0.00E+00 | 0.00E+00 |
| FT | 3.52E+06 | 3.37E+06 | 1.28E+05 |

Q.13: The schematic below presents a cascode current mirror using NMOS transistors.




Draw the ac equivalent circuit for the system and indicate in the circuit how you could determine the output resistance of the current mirror.

Q.14: Consider the NMOS amplifier with PMOS active load as shown below. Assume that the I-V equation is of the form $I(NMOS)= K_n(V_{GS}-V_{TN})^2(1+\lambda_n V_{DS})$ and $I(PMOS)=K_p(V_{SG}-|V_{TP}|)^2(1+\lambda_p V_{SD})$. Given $K_n=90\ \mu A/V^2$, $K_p=30\ \mu A/V^2$, $V_{TN}=1$ V, VTP= -1 V, $\lambda_n=0.01\ V^{-1}$, $\lambda_p=0.02\ V^{-1}$, $V_{dd}=10$ V, $V_{SS}=-3$V, and I1=200 μA, find the DC voltages at various nodes (i.e., $V_x$, $V_z$ ) of the system. Assume $V_i$ =0 V. The PMS transistors are identical.



Q.15,16 : deleted

Q.17. In a MOS differential amplifier using current mirror load, the voltage gain is given by $g_m/(g_{dp}+g_{dn})$ where $g_m = \sqrt{2\mu C_{ox}\frac{W}{L} I_{DC}}$ for the amplifying device and $g_{dp} = \frac{1}{r_{op}}$, $g_{dn} = \frac{1}{r_{on}}$. The suffixes 'p', 'n' standing for PMOS and NMOS transistors.

Given $\mu C_{ox} = 100\ \mu A/V^2$, $I_{DC} = 100\ \mu A$, $V_{TN} = 1V$, $V_{AP} = 20V$, $V_{An} = 30V$.

Design the aspect ratio W/L of the amplifying transistors for a gain of 40.

Soln:

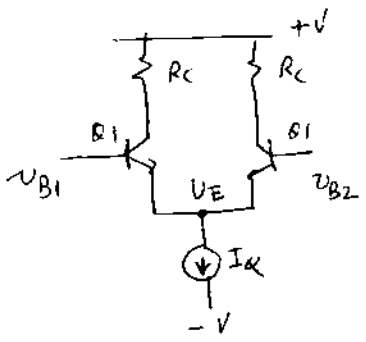
$$40 = \frac{g_m}{g_{dp}+g_{dn}}$$

$g = \frac{1}{r}$ ; $r = \frac{V_A}{I_{DC}}$

$$40 = \frac{\sqrt{2 \times 100 \times 10^{-6} \frac{W}{L} \times 100 \times 10^{-6}}}{100 \times 10^{-6}\left(\frac{1}{20}+\frac{1}{30}\right)}$$

Solving $\sqrt{\frac{2W}{L}} = \frac{10}{3}$ ; $\frac{W}{L} = \frac{50}{9}$

Q.18: For the BJT DA, find an expression for the common emitters node voltage $v_E$ when the DA has two large signal (, input voltages $v_{B1}$, $v_{B2}$.




Ans: For large signal operation you use the exponential equation for the BE junctions of each transistor.

For $Q_1$, $i_{E1} = I_S e^{(v_{B1}-v_E)/nV_T} \simeq I_S e^{(v_{B1}-v_E)/V_T}$ assuming $n=1$

For $Q_2$, $i_{E2} = I_S e^{(v_{B2}-v_E)/V_T}$.

$V_T \rightarrow$ thermal voltage $= \frac{kT}{q}$

But by KCL at $v_E$ node, $i_{E1} + i_{E2} = I_Q$

So $I_Q = I_S \cdot e^{\frac{v_{B1}-v_E}{V_T}} + I_S e^{\frac{v_{B2}-v_E}{V_T}}$, assuming identical transistors.

$$= I_S e^{-\frac{v_E}{V_T}} \cdot \left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)$$

So $$e^{-v_E/V_T} = \frac{I_Q}{I_S} \cdot \frac{1}{\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)}$$

Taking natural log on both sides

$$-\frac{v_E}{V_T} = \ln\left(\frac{I_Q}{I_S}\right) - \ln\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right)$$

$$\text{or } v_E = V_T \left[\ln\left(e^{\frac{v_{B1}}{V_T}} + e^{\frac{v_{B2}}{V_T}}\right) - \ln\left(\frac{I_Q}{I_S}\right)\right].$$

Q: What if $v_{B1} = \frac{v_d}{2}$; $v_{B2} = -\frac{v_d}{2}$ ? and $v_d$ is very small } TRY YOURSELF!

## 2.5 Additional references

2.5.1: *Analog Integrated Circuit Design*, David A. Johns, and Ken Martin, John Wiley & Sons Inc., © 1997, ISBN 0-471-14448-7.

2.5.2: *CMOS Circuit Design, Layout, and Simulation*, R. Jacob Baker, Wiley- Interscience, IEEE Press, © 2005, ISBN 0-471-70055-X.

2.5.3: Design of Aanlog Integrated Circuits and Systems, Kenneth R. Laker, and Willy M.C. Sansen, McGraw-Hill, Inc., © 1994, ISBN 0-07-036060-X.

# CHAPTER 3

## Frequency Response of Basic BJT and MOSFET Amplifiers

(*Review materials in Appendices III and V*)

In this chapter you will learn about the general form of the frequency domain transfer function of an amplifier. You will learn to analyze the amplifier equivalent circuit and determine the critical frequencies that limit the response at low and high frequencies. You will learn some special techniques to determine these frequencies. BJT and MOSFET amplifiers will be considered. You will also learn the concepts that are pursued to design a wide band width amplifier. Following topics will be considered.

- Review of Bode plot technique.
- Ways to write the transfer (i.e., gain) functions to show frequency dependence.
- Band-width limiting at low frequencies (i.e., DC to $f_L$). Determination of lower band cut-off frequency for a single-stage amplifier – short circuit time constant technique.
- Band-width limiting at high frequencies for a single-stage amplifier. Determination of upper band cut-off frequency- several alternative techniques.
- Frequency response of a single device (BJT, MOSFET).
- Concepts related to wide-band amplifier design – BJT and MOSFET examples.

### 3.1 A short review on Bode plot technique

*Example:* Produce the Bode plots for the magnitude and phase of the transfer function $T(s) = \dfrac{10s}{(1+s/10^2)(1+s/10^5)}$, for frequencies between 1 rad/sec to $10^6$ rad/sec.

We first observe that the function has zeros and poles in the numerical sequence 0 (zero), $10^2$ (pole), and $10^5$ (pole). Further at ω=1 rad/sec i.e., lot less than the first pole (at $\omega=10^2$ rad/sec), $T(s) \cong 10s$. Hence the first portion of the plot will follow the asymptotic line rising at 6 dB/octave, or 20 dB/decade, in the neighborhood of ω=1 rad/sec. The magnitude of *T(s)* in decibels will be approximately 20 dB at ω= 1 rad/sec.

The second asymptotic line will commence at the pole of $\omega=10^2$ rad/sec, running at -6 dB/octave slope relative to the previous asymptote. Thus the overall asymptote will be a line of slope zero, i.e., a line parallel to the ω- axis.

The third asymptote will commence at the pole $\omega=10^5$ rad/sec, running at -6 dB/Octave slope relative to the previous asymptote. The overall asymptote will be a line dropping off at -6 dB/octave beginning from $\omega=10^5$ rad/sec.

Since we have covered all the poles and zeros, we need not work on sketching any further asymptotes. The three asymptotic lines are now sketched as shown in figure 3.1.

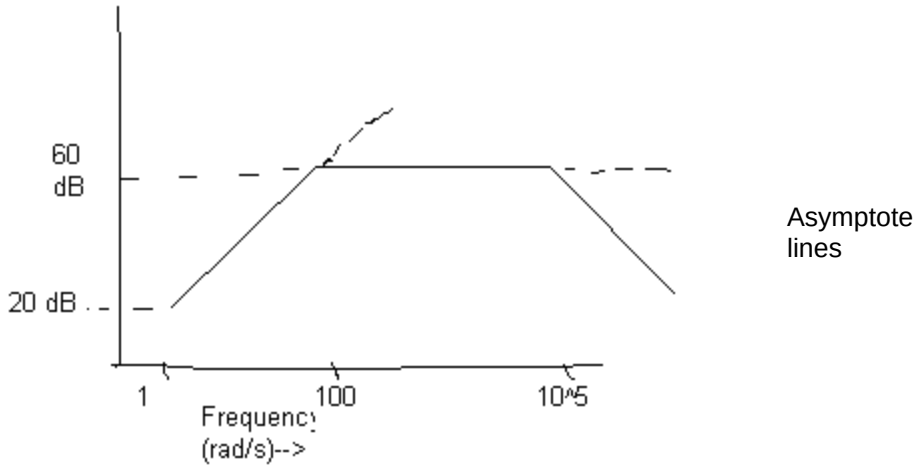



Figure 3.1: The asymptotic line plots for the *T(s)*.

The actual plot will follow the asymptotic lines being 3 dB below the first corner point (i.e.,at ω=100)i.e., 57 dB ,and 3 dB below the second corner point (i.e., ω=10^5), i.e. 57 dB. In between the two corner point the plot will approach the asymptotic line of constant value 60 dB. The magnitude plot is shown in figure 3.2.

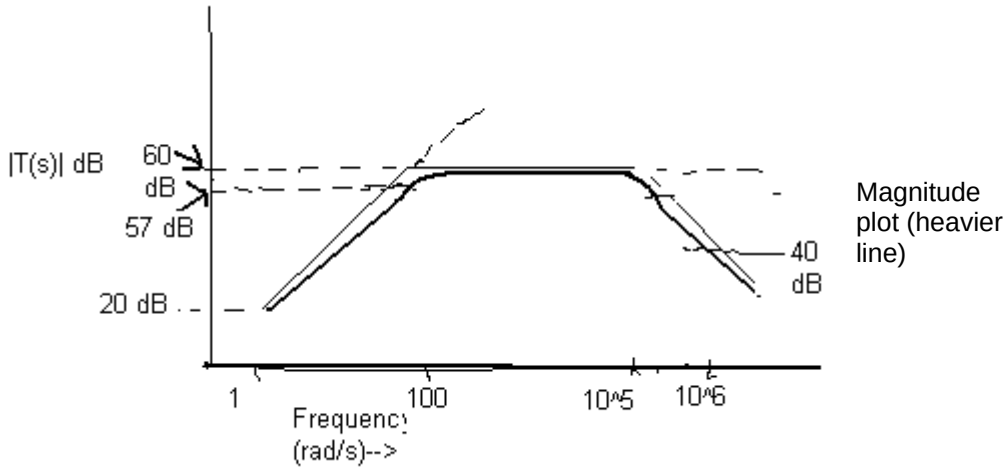



Figure 3.2:Bode magnitude plot for *T(s)*

For phase plot, we note that the 's' in the numerator will give a constant phase shift of +90$^o$ degrees (since $s \to j\omega \to 0 + j\omega$, angle: $\tan^{-1}(\omega/0) \to \tan^{-1}(\infty) \to 90^o$), while the terms in the denominator will produce angles of $-\tan^{-1}(\omega/10^2)$, and $-\tan^{-1}(\omega/10^5)$ respectively. The total phase angle will then be:

$$\phi(\omega) = 90^o - \tan^{-1}(\omega/10^2) - \tan^{-1}(\omega/10^5) \qquad (3.1)$$

Thus at low frequency (<< 100 rad/sec), the phase angle will be close to 90$^o$. Near the pole frequency ω=100, a -45$^o$ will be added due to the ploe at making the phase angle to be close to +45$^o$. The phase angle will progressively decrease, because of the first two terms in φ(ω). Near the second pole ω=$10^5$, the phase angle will approach

$\phi(\omega) = 90^o - \tan^{-1}(10^5/10^2) - \tan^{-1}(10^5/10^5) \cong 90^o - 90^o - 45^o$ i.e., -45$^o$ degrees.

(The student in encouraged to draw the curve)

3.2 Simplified form of the gain function of an amplifier revealing the frequency response limitation

3.2.1 Gain function at low frequencies

Electronic amplifiers are limited in frequency response in that the response magnitude falls off from a constant mid-band value to lower values both at frequencies below and above an intermediate range (the mid-band) of frequencies. A typical frequency response curve of an amplifier system appears as in figure3.3.

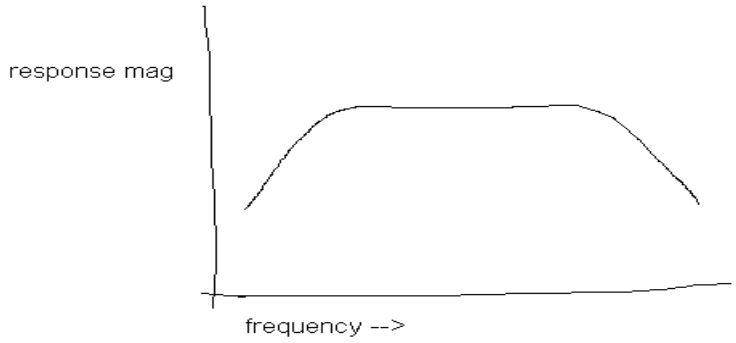



Figure 3.3: Typical frequency response function magnitude plot for an electronic amplifier

Using the concepts of Bode magnitude plot technique, we can approximate the low-frequency portion of the sketch above by an expression of the form $T_L(s) = \frac{Ks}{s+a}$, or $T_L(s) = \frac{K}{1+a/s}$. In this $K$ and $a$ are constants and $s=j\omega$, where $\omega$ is the (physical, i.e., measurable) angular frequency (in rad/sec). In either case, when the signal frequency is very much smaller than the pole frequency 'a', the response $T_L(s)$ takes the form $Ks/a$. This function increases progressively with the frequency $s = j\omega$, following the asymptotic line with a slope of +6 dB per octave. At the pole frequency 'a', the response will be 3 dB below the previous asymptotic line, and henceforth follow an asymptotic line of slope (-6+6=0) of zero dB/ octave. Thus $T_L(s)$ will remain constant with frequency, assuming the mid-band value. Note that $T_L(s)$ is a first order function in 's' (a single time-constant function).

The *frequency* at which the magnitude plot reaches *3 dB below the mid-band* (i.e., the flat portion of the magnitude response curve) gain value is known as the *-3 dB frequency* of the gain function. For the low-frequency segment (i.e., $T_L$(s)) of the magnitude plot this will be designated by $f_L$ (or $\omega_L = 2\pi f_L$).

In a practical case the function $T_L(s)$ may have several poles and zeros at low frequencies. The pole which is *closest* to the flat mid-band value is known as the *low frequency dominant pole* of the system. Thus it is the pole of *highest* magnitude among all the poles and zeros at low frequencies. Numerically the *dominant* pole differs from the -3 dB frequency. But for simplicity, one can approximate dominant pole to be of same value as the -3dB frequency. The -3dB frequency at low frequencies is also sometimes referred to as the *lower* cut-off frequency of the amplifier system.

The frequency response limitation at low frequency occurs because of coupling and by-pass capacitors used in the amplifier circuit. For single-stage amplifiers, i.e., CE, CB..CS,CG amplifiers these capacitors come in series with the signal path (i.e., they form a loop in the signal path), and hence impedes the flow of signal coupled to the internal nodes ( i.e., BE nodes of the BJT, GS nodes of the MOSFET) of the active device. The students can convince themselves by considering the simple illustration presented in figure 3.4.

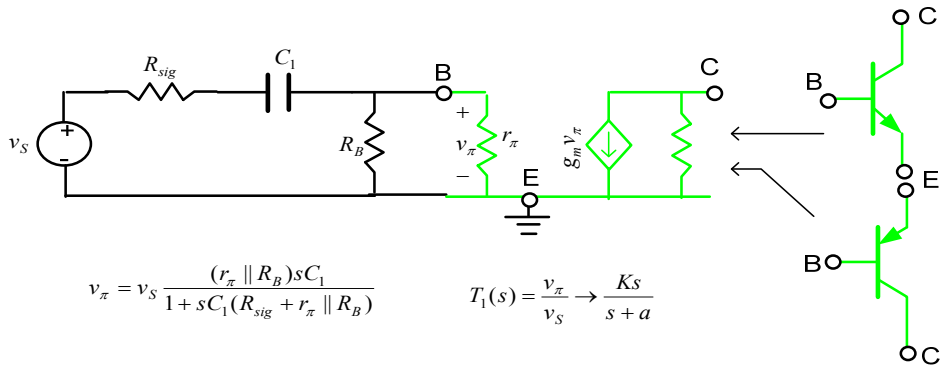



Figure 3.4: Illustrating the formation of s *zero* in the voltage transfer function because of a capacitor in the signal loop. The controlling voltage $v_\pi$ for the VCCS has a *zero* because of the presence of $C_1$.

3.2.2 Gain function at high frequencies

A similar scenario exists for the response at high frequencies. By considering the graph in Fig.3.3 at frequencies beyond (i.e., higher than) the mid-band segment, we can propose the form of the response function as: $T_H(s) = \frac{K}{s+b}$. $K$ and $b$ are constants. Other alternative forms are: $T_H(s) = \frac{K_o b}{s+b}$, or $T_H(s) = \frac{K_o}{1+s/b}$. Note that in all cases, for frequencies << the pole frequency 'b', the response function assumes a constant value (i.e., the mid-band response). For $T_H(s)$, which is a *first-order* function, the frequency $b$ becomes the *-3db frequency* for high frequency response, or the *upper* cut-off frequency. When there are several poles and zeros in the high frequency range, the pole with the *smallest* magnitude and hence closest to the mid-band response zone is referred to as the *high frequency dominant* pole. Again, numerically the high frequency dominant pole will be different from the upper cut-off frequency. But in most practical cases, the difference is small. In case the high frequency response has several poles and zeros, one can formulate the function as

$$T_H(s) = \frac{(1+s/\omega_{z1})(1+s/\omega_{z2})..}{(1+s/\omega_{p1})(1+s/\omega_{p2})..} \qquad (3.2)$$

In an integrated circuit scenario coupling or by-pass capacitors are absent. The frequency dependent gain function (i.e., *transfer function*) is produced because of the intrinsic capacitances (*parasitic* capacitances) of the devices. As a consequence the zeros occur at very high frequencies and only one of the poles fall in the signal frequency range of interest, with the other poles at substantially higher frequencies. Thus if $\omega_{p1}$ is the pole of smallest magnitude, the amplifier will have $\omega_{p1}$ as the dominant pole. In such case $T_H(s) \cong \frac{\omega_{p1}}{s+\omega_{p1}}$, and $\omega_{p1}$ will also be the -3 dB or upper cut-off frequency of the system. Otherwise, the -3 dB frequency $\omega_H$ can be calculated using the formula[1]

[1] Sedra and Smith, "Microelectronic Circuits", 6th edn., ch.9, p.722, Oxford University Press, ©2010.

$$\omega_H \cong \frac{1}{[(\frac{1}{\omega_{p1}^{\ 2}} + \frac{1}{\omega_{p2}^{\ 2}} + ...) - 2(\frac{1}{\omega_{z1}^{\ 2}} + \frac{1}{\omega_{z2}^{\ 2}} + ..)]^{1/2}} \qquad (3.3)$$

3.2.3 Simplified (first order) form of the amplifier gain function

Considering the discussions in sections 3.2.1-2 we can formulate the simplified form of the amplifier gain function can then be considered as :

$$A(s)=A_M F_L(s) F_H(s) \qquad (3.4)$$

In (3.4), $A_M$ is independent of frequency, $F_L$ has a frequency dependence of the form $s/(s+w_L)$, while $F_H$ has a frequency dependence of the form $w_H/(s+w_H)$. Thus for frequencies higher than $w_L$ and for frequencies lower than $w_H$ the gain is close to $A_M$. This is a constant gain and the frequency band $w_H$ - $w_L$ is called the mid-band frequencies. So in the mid-band frequencies the gain is constant i.e., $A_M$. At frequencies $<< w_L$, $F_L(s)$ increases with frequency (re: Bode plot) by virtue of the '*s*' in the numerator, at 6dB/octave. As the frequency increases, the rate of increase slows down and the Bode plot merges with the constant value $A_M$ shortly after $w=w_L$. At $w=w_L$ the response falls 3 dB below the initial asymptotic line of slope 6dB/octave. Similarly, as frequency increases past $w_H$ , the response A(s) tends to fall off, passing through 3dB below $A_M$ (in dB) at $w=w_H$ and then following the asymptotic line with slope *minus* 6dB/octave drawn at $w=w_H$ . It is of interest to be able to find out these two critical frequencies for basic single stage amplifiers implemented using BJT or MOSFET.

3.3 Simplified high-frequency *ac* equivalent circuits for BJT and MOSFET devices

It can be noted that for amplifiers implemented in integrated circuit technology only the upper cut-off frequency $w_H$ is of interest. To investigate this we must be familiar with the ac equivalent circuit of the transistor at high frequencies. The elements that affect the high frequency behavior are the parasitic capacitors that exist in a transistor. These arise because a transistor is made by laying down several semiconductor layers of different conductivity (i.e., p-type and n-type materials). At the junction of each pair of dissimilar layers, a capacitance is generated. We will consider the simplified high-frequency equivalent circuits for the BJT and MOSFET as shown in Figs.3.5-3.6. In these models

each transistor is assigned with only two parasitic capacitance associated with its internal nodes. These arise out of the semiconductor junctions that are involved in building the transistor. For the BJT, the base material produces a small resistance $r_x$, which assumes importance for high (signal) frequency applications (signal processing). The models for N-type (i.e., NPN, NMOSFET) and P-type (i.e., PNP, PMOSFET) transistors are considered same. In more advanced models (used in industries) more number of parasitic capacitances and resistances are employed.

### 3.3.1 High frequency response characteristics of a BJT

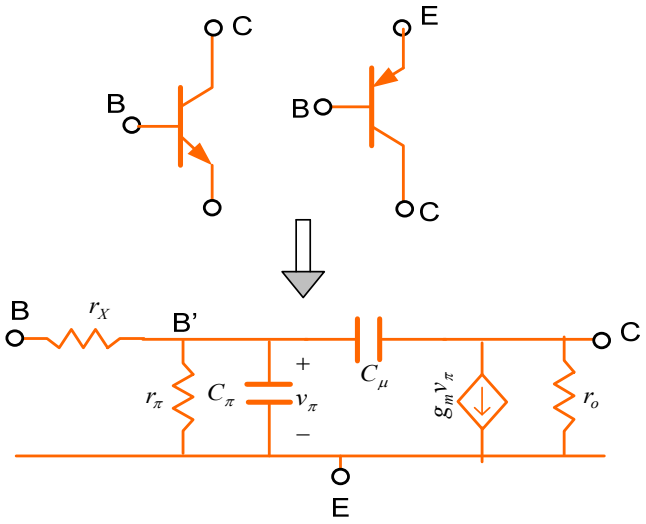



Figure 3.5: Simplified ac equivalent circuit for a BJT device for high signal frequency situation.

An important performance parameter of a BJT device is the small signal short circuit current gain of the device under CE mode of operation. Thus in Fig.3.5, if we insert an ac current source at terminal **B** and seek the ac short-circuit output current at node C, we can construct the CE ac equivalent circuit as in Fig.3.6. The short-circuit current gain $i_o/i_i$ of the device can be derived from the KCL equations (returning terminal C to *ac* ground) at the nodes B and B'. Writing $g_i = 1/r_i$ in general, we get

$$i_i = g_x(v_B - v_\pi), \quad 0 = -g_x v_B + (g_x + g_\pi + sC_\pi + sC_\mu)v_\pi \qquad (3.5)$$

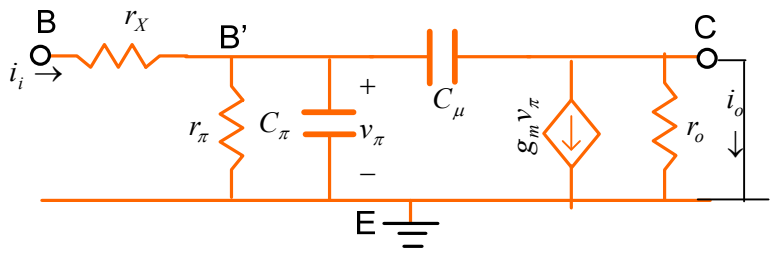



Figure 3.6: Configuring the BJT device for CS short-circuit current gain calculation.

Solving for $v_\pi$ and noting that at C node (which is short circuited for *ac*) $i_o = -g_m v_\pi + sC_\mu$, we can finally derive the *short-circuit* current gain of the BJT under CE mode of operation as:

$$h_{fe}(s) = \frac{i_o}{i_i} = -\frac{-(g_m - sC_\mu)g_x}{g_x(g_\pi + s(C_\pi + C_\mu))} = -\frac{g_m - sC_\mu}{C_\pi + C_\mu}\frac{1}{s + \dfrac{1}{r_\pi(C_\pi + C_\mu)}} \qquad (3.6)$$

Eq.(3.6) represents a transfer function with a low-frequency (i.e., $\omega \approx 0$) value of $h_{fe}|_{\text{low-frequency}} = h_{fe}(s)|_{s=j\omega=0} = -g_m r_\pi = -\beta$, the familiar symbol for the current gain of a BJT in CE operation. Because $C_\mu$ is very small, the *zero* of $h_{fe}(j\omega)$ i.e., $g_m/C_\mu$ lies at very high frequencies. Using the symbol $h_{fe}$ (0) for low-frequency ($\omega \approx 0$) value of $h_{fe}$, and for frequencies << $\omega_z = g_m / C_\mu$, the Bode magnitude plot of $h_{fe}$ appears as in Fig. 3.7.

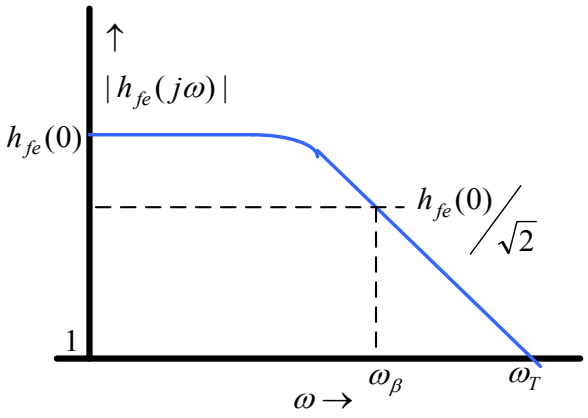



Figure 3.7: The Bode magnitude plot of $|h_{fe}(j\omega)|$.

It is observed that at the frequency $\omega_\beta = 1/r_\pi(C_\pi + C_\mu)$, $|h_{fe}|$ drops to $h_{fe}(0)/\sqrt{2}$, i.e., -3db below $h_{fe}(0)$. This frequency is known as the $\beta$ cut-off frequency for the BJT under CE mode of operation.

At frequencies much higher than $\omega_\beta$, $h_{fe}(j\omega)$ changes as (see eq.(3.6)) $\approx -\frac{g_m}{j\omega(C_\pi + C_\mu)}$.

This reaches a magnitude of *unity* (i.e. =1), at a frequency

$$\omega_T = g_m/(C_\pi + C_\mu) \qquad (3.7)$$

This is known as the *transition frequency* of the BJT for operation as CE amplifier. The *transition frequency* $\omega_T = 2\pi f_T$ is a very *important* parameter of the BJT for high-frequency applications. For a given BJT, the high-frequency operational limit of the device can be increased by increasing $\omega_T$ via an increase in $g_m$, the *ac* transconductance of the BJT. This, however, implies an increase in the DC bias current (since $g_m = I/V_T$) and hence an increase in the DC power consumption of the system. Recalling the relation $g_m r_\pi = \beta + 1$, we can deduce that

$$\omega_T = (1+\beta)\omega_\beta = (1 + h_{fe}(0))\omega_\beta \qquad (3.8)$$

In real BJT devices $C_\pi >> C_\mu$, and $C_\pi + C_\mu >> C_\mu$. Hence, the *zero* frequency $\omega_z = g_m/C_\mu$ will be >> the *transition* frequency $\omega_T$. Since $|h_{fe}(j\omega)|$ becomes <1 beyond $\omega_T$, the *zero* frequency bears no practical interest.

### 3.3.2 High frequency response characteristics of a MOSFET

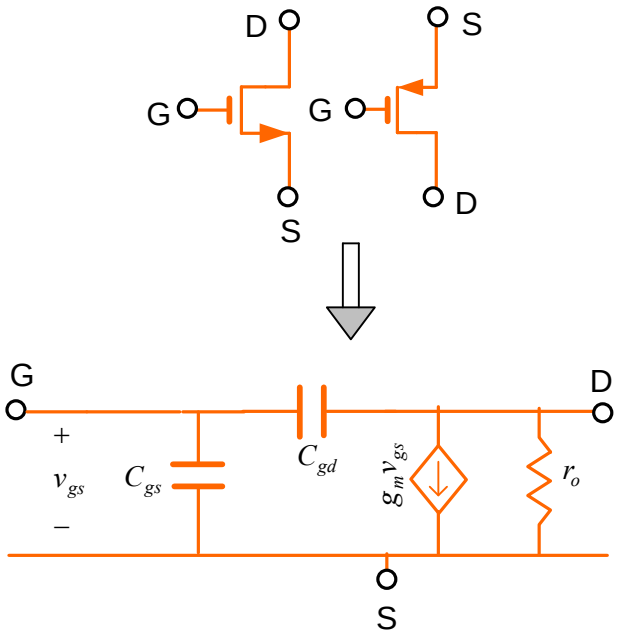



Figure 3.8: Simplified ac equivalent circuit for a MOSFET device for high signal frequency situation.

A simplified ac equivalent circuit for the MOSFET is shown in figure 3.8. The body terminal (B) for the MOSFET , and the associated parasitic capacitances as well as the body transconductance ($g_{mb}$) have not been shown. By following a procedure similar to that of a BJT, it can be shown that the *short circuit current gain* of the MOSFET configured as a CS amplifier is given by $i_o/i_i = -\dfrac{g_m - sC_{gd}}{s(C_{gs}+C_{gd})}$ which can be approximated as $\dfrac{i_o}{i_i} = -\dfrac{g_m}{s(C_{gs}+C_{gd})}$ for frequencies well below the *zero* frequency $g_m/sC_{gd}$.

Under the above assumption the frequency at which the magnitude of the current gain becomes *unity* i.e., the *transition frequency*, becomes:

$$\omega_T = \frac{g_m}{(C_{gs}+C_{gd})} \qquad (3.9)$$

The *transition frequency* of a MOSFET is a very important parameter for high frequency operation. This can be increased via an increase in $g_m$ with the attendant increase in the DC bias current and hence increase in DC power dissipation.

## 3.4 Calculation of $\omega_L$ – the lower cut-off frequency (*Short Circuit Time Constant method*)

Figure 3.9(a) depicts a typical CE-BJT amplifier with coupling capacitors $C_1$, $C_3$, and the by-pass capacitor $C_E$. Each of these capacitors fall in the *signal path* for the operation of the amplifier and hence influences the voltage gain function in terms of introducing several poles and zeros in the gain transfer function.

A simplified method to determine *the poles* is to consider *only one of the capacitors* effective at a time and assume that the other capacitors behave approximately as *short circuits*. Because only one capacitor is present in the system, it is easy to determine the *time constant* parameter of the *associated ac equivalent* circuit. Hence the method is known as *short circuit time constant* method (SCTC). Figures 3.9(b)-(d) show the three *ac* equivalent circuits under the assumption of only one of $C_1$, $C_2$, or $C_E$ present in the circuit. The location(s) to be used for the calculation of the equivalent *Thevenin* resistance for each of the capacitors ($C_1$, $C_E$, $C_3$) are shown in blue lines on the diagrams. The internal capacitances of the BJT offer very high impedance at low frequencies and hence they are considered as open circuits (so these are not shown).

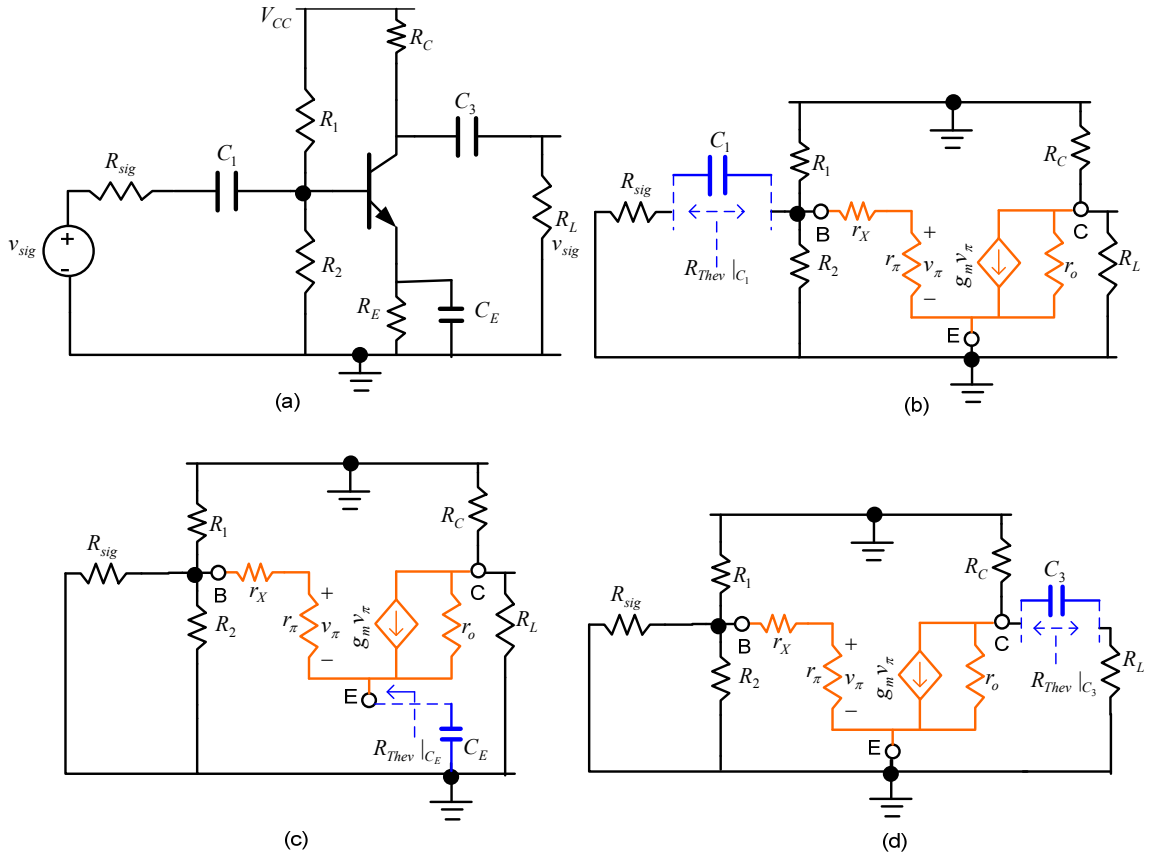


Figure 3.9: (a) Schematic of a CE amplifier with four resistor biasing; (b) the *ac* equivalent circuit with $C_E$ ,$C_3$ as *short circuits*; (c) the *ac* equivalent circuit with $C_1$ ,$C_3$ as *short circuits*, and (d) the *ac* equivalent circuit with $C_E$ ,$C_1$ as *short circuits*.

Analysis of the equivalent circuit in Fig.3.9(b) is straightforward. By inspection, the *Thevenin* resistance associated with $C_1$ is $R_{Th1} = R_{sig} + R_1 \,||\, R_2 \,||\, (r_x + r_\pi)$, where the notation || implies *in parallel with*. The associated time-constant is $C_1R_{Th1}$, and the corresponding *pole-frequency* is $\omega_{L1} = 1/(C_1R_{Th1})$. Similarly, the *Thevenin* resistance for $C_3$ is $R_{Th3} = R_C \,||\, r_o + R_L$ (see Fig.3.9(d)). The corresponding *pole-frequency* is $\omega_{L3} = 1/(C_3R_{Th3})$. The calculation of the *Thevenin* resistance associated with $C_E$ can be simplified considerably by assuming $r_o$ as *inifinity*. Then by inspection (see Fig.3.9(c)), $R_{ThE} = R_E \,||\, (\dfrac{r_\pi + r_x + R_1 \,||\, R_2 \,||\, R_{sig}}{1 + h_{fe}})$. The corresponding *pole-frequency* is $\omega_{LE} = 1/(C_ER_{ThE})$.

---

A more adventurous student may discard the assumption of $r_o \rightarrow$ *infinity* and proceed to set up a 3 by 3 nodal admittance matrix (NAM) (see *Appendix III*) by using the substitutions $r_{\pi p} = r_\pi + r_x$, $R_{sp} = R_{sig} \,||\, R_1 \,||\, R_2$, $R_{cp} = R_c \,||\, R_L$, and by inserting a *dummy* current source $i_x$ at the node labeled as E in Fig. 3.9(c). The NAM will appear as

$$\begin{bmatrix} g_E + g_{\pi p} + g_o & -g_{\pi p} & -g_o \\ -g_{\pi p} & g_{\pi p} + g_{sp} & 0 \\ -g_o & 0 & g_o + g_{cp} \end{bmatrix} \begin{bmatrix} V_E \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} i_x + g_m v_\pi \\ 0 \\ -g_m v_\pi \end{bmatrix} \qquad (3.10)$$

In the above $g_E = 1/R_E$,, $g_{\pi p} = 1/r_{\pi p}$, $g_o = 1/r_o$, and so on, have been used. With the further assumption (it is very good if $r_x$ is << $r_\pi$) of $v_\pi = V_B - V_E$, the matrix equation (3.10), becomes, after rearrangement (i.e., changing sides):

$$\begin{bmatrix} g_E + g_{\pi p} + g_o + g_m & -g_{\pi p} - g_m & -g_o \\ -g_{\pi p} & g_{\pi p} + g_{sp} & 0 \\ -g_o - g_m & 0 + g_m & g_o + g_{cp} \end{bmatrix} \begin{bmatrix} V_E \\ V_B \\ V_C \end{bmatrix} = \begin{bmatrix} i_x \\ 0 \\ 0 \end{bmatrix} \qquad (3.11)$$

Then $R_{ThE}$ is given by $V_E/i_x$. The result is (using *Maple* program code):

$$R_{ThE} = \frac{(g_{\pi p} + g_{sp})(g_o + g_{cp})}{g_E g_{\pi p} g_o + g_E g_{\pi p} g_{cp} + g_E g_{sp} g_o + g_E g_{sp} g_{cp} + g_{\pi p} g_{sp} g_o + g_{\pi p} g_{sp} g_{cp} + g_o g_{\pi p} g_{cp} + g_o g_{sp} g_{cp} + g_m g_{sp} g_{cp}}$$

Now introducing the assumption $g_o \rightarrow 0$ (i.e., $r_o \rightarrow$ *infinity*), one will get

$$R_{ThE} = \frac{(g_{\pi p} + g_{sp})g_{cp}}{g_E g_{\pi p} g_{cp} + g_E g_{sp} g_{cp} + g_{\pi p} g_{sp} g_{cp} + g_m g_{sp} g_{cp}} \qquad (3.12)$$

Substituting back in terms of the resistance notations, i.e., $g_E = 1/R_E$,, $g_{\pi p} = 1/r_{\pi p}$, $g_o = 1/r_o$, and so on, one can get

$$R_{ThE} = \frac{(R_{sp} + r_{\pi p})R_E}{R_{sp} + r_{\pi p} + R_E + g_m r_{\pi p} R_E} \qquad (3.13)$$

Using $g_m r_{\pi p} = h_{fe}$, and simplifying, one arrives at $R_{ThE} = \frac{(R_{sp} + r_{\pi p})R_E/(1+h_{fe})}{(R_{sp} + r_{\pi p})/(1+h_{fe}) + R_E}$, i.e.,

$$R_{ThE} = R_E \,||\, (\frac{R_{sp} + r_{\pi p}}{1 + h_{fe}}) = R_E \,||\, (\frac{r_\pi + r_x + R_1 \,||\, R_2 \,||\, R_{sig}}{1 + h_{fe}}) .$$

********

The overall lower -3 dB frequency is calculated approximately by the formula $\omega_L = \omega_{L1} + \omega_{L3} + \omega_{LE}$. If out of the several poles of the low-frequency transfer function $F_L(s)$, one is very large compared to all other poles and zeros, the overall lower -3 dB frequency $\omega_L$ becomes $\cong$ dominant pole (i.e., largest of $\omega_{L1}$ or $\omega_{LE}$ or $\omega_{L3}$).

If the numerical values of the various pole frequencies are known (by exact circuit analysis followed by numerical computation), the lower 3-dB frequency can be calculated approximately by a formula of the form $\omega_L = \sqrt{\omega_1^2 + \omega_2^2 + \omega_3^2 + ...}$ where, $\omega_1$, $\omega_2$ , .. are the individual pole frequencies and the zero-frequencies are very small compared with the pole frequencies.

*Example 3.4.1*: Consider the following values in a BJT amplifier.

$R_{sig}$ =50Ω, $R_B = R_1 || R_2$ = 10 kΩ, $r_\pi$ =2500, $r_x$ =25Ω, $h_{fe}$ =100 and $R_E$ =1kΩ, $R_C$ =1.5kΩ, $R_L$ =3.3 kΩ, $V_A$ =20 volts, $I_C \approx$ 1 mA. Further, $C_1$ =1uF and $C_E$= 10uF and $C_3$ = 1uF. What is $\omega_L$ ?

According to above formulas, $R_{Th1}$ = 2.05kΩ , $R_{ThE}$ =25.25Ω and $R_{Th3}$ =1.39kΩ+3.3kΩ = 4.69kΩ. Then $\omega_{L1}$ = 487.8 rad/s, $\omega_{LE}$ = 3.96E3 rad/sec and $\omega_{L3}$ = 213.2 rad/sec. Then , $\omega_L \approx \omega_{L1} + \omega_{LE} + \omega_{L3} = 4.661E3$ rad/s, which is pretty close to $\omega_{LE}$.

*Example 3.4.2*: What if , $\omega_L$= 1800 rad/sec is to be designed? We can assume, for example, $\omega_{L1} = 0.8\omega_L$, , $\omega_{LE}$= $\omega_{L2}$= $0.1\omega_L$ and $\omega_{L3}$=$0.1\omega_L$. Then, design the values of the capacitors $C_1$, $C_E$ and $C_3$. The student can try other relative allocations too.

3.5: Calculation of $\omega_H$ – the higher cut-off frequency

Several alternative methods exist in the literature. The following are presented.

3.5.1: Open circuit time-constant (OCTC) method

This is similar to the case as with low frequency response. For high frequency operation, we are interested in the capacitor which will have lower reactance value since this capacitance will start to degrade the high frequency response sooner than the other. Thus, we can consider one capacitor at a time and assume that the other capacitors are too small and have reasonably high reactance values (for a C, the reactance is $\propto$ 1/C) so that they could be considered as open circuits. We then calculate the associated time constant. Thus the method is named as *open circuit time constant* (OCTC) method. We shall illustrate the method using the case of a CE BJT amplifier.

Consider figure 3.10(a) which shows the *ac* equivalent circuit of the CE-BJT amplifier of Fig.3.9(a). The *high frequency* equivalent circuit for the BJT has been included. The coupling and by-pass capacitors are assumed as *short circuits* for *high frequency* situation.

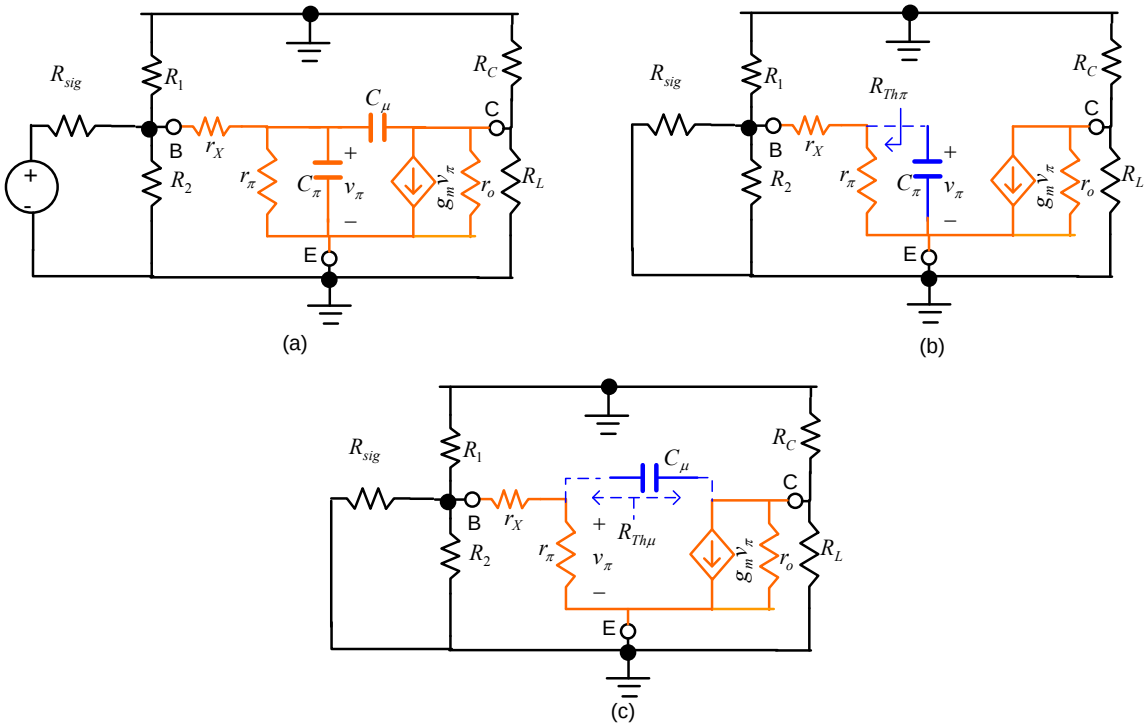



Figure 3.10: (a) high frequency equivalent circuit of the amplifier in Fig.3.9(a); (b) the equivalent circuit with $C_\mu$ open; (c) the equivalent circuit with $C_\pi$ open.

*Case 1: Cμ open*

The ac equivalent circuit to determine the *Thevenin* equivalent resistance $R_{Th\pi}$ across $C_\pi$ is shown in Fig.3.10(b). By simple inspection $R_{Th\pi} = r_\pi \,\|\, (r_x + R_{sig} \,\|\, R_1 \,\|\, R_2)$

The high frequency pole due to this situation is $\omega_{H1} = 1/(C_\pi R_{Th\pi})$.

*Case 2: $C_\pi$ open*

We now need to determine the Thevenin equivalent resistance $R_{Th\mu}$ across $C_\mu$. The associated equivalent circuit is shown in Fig.3.10(c). We can use a dummy signal current source $i_x$ and carry out few steps of basic circuit analysis (see Fig.3.11).

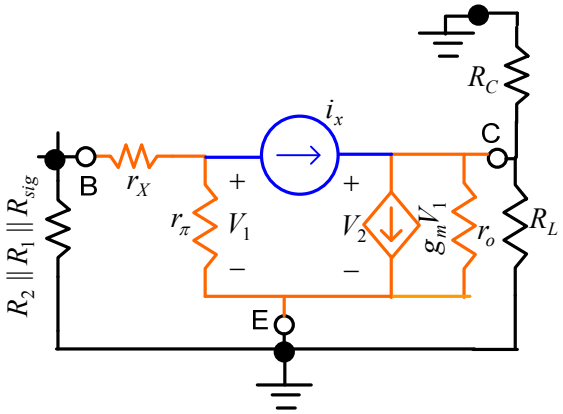



Figure 3.11: Equivalent circuit for calculating $R_{Th\mu}$

KCL at $V_1$ node gives: $V_1 G_S' + i_x = 0, \quad G_S' = \dfrac{1}{r_\pi \| (r_x + R_{sig} \| R_1 \| R_2)} = 1/R_S'$ (3.13a)

KCL at $V_2$ node gives: $-i_x + g_m V_1 + V_2 G_L' = 0, \quad G_L' = \dfrac{1}{r_o \| R_C \| R_L} = 1/R_L'$ (3.13b)

Solving (3.13(a),(b)) for $V_1$ and $V_2$ we can find $R_{Th\mu} = (V_2 - V_1)/i_x = R_s' + (1 + g_m R_s') R_L'$

The high frequency pole for $C_\mu$ is $\omega_{H2} = 1/ C_\mu R_{Th\mu}$.

When the two pole frequencies are comparable in values, the upper -3 dB frequency is given approximately by $\omega_H = 1/(C_\pi R_{Th\pi} + C_\mu R_{Th\mu}) = 1/(\tau_1 + \tau_2)$ (3.14)

If, however, the two values are widely apart (say, by a factor of 5 or more), the upper -3 dB frequency will be called as the *dominant high frequency pole* and will be equal to the lesser of $\omega_{H1}$ and $\omega_{H2}$.

3.5.2: Application of Miller's theorem

This theorem helps simplifying the ac equivalent circuit of the BJT CE amplifier by removing the $C_\mu$ capacitor, which runs between two floating nodes (i.e., between the base side to the collector side). In principle, if an admittance $Y_3$ runs between nodes 1 and 2 with $Y_1$ at node 1 (to ground) and $Y_2$ at node 2 (and ground) and if K is the voltage gain $(V_2/V_1)$ between nodes 1 and 2, then $Y_3$ can be split into two parts – one being in parallel

with $Y_1$ with a value $Y_3$ (1-K) and another becoming in parallel with $Y_2$ with a value (1-1/K)$Y_3$. The theorem can be applied to all cases of floating elements connected between two nodes in a system.

As a result of this principle, the high frequency equivalent circuit of the CE BJT amplifier (see Fig.3.5) simplifies to figure 3.12.

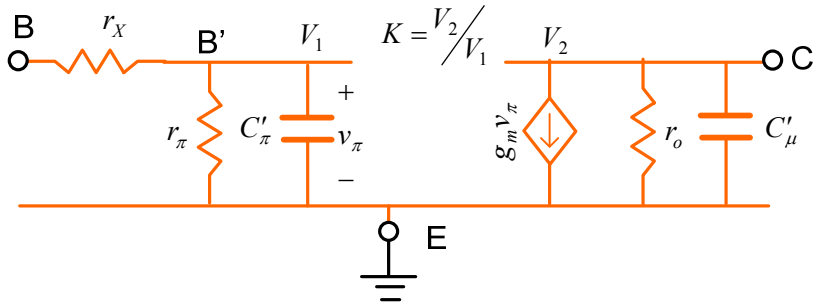


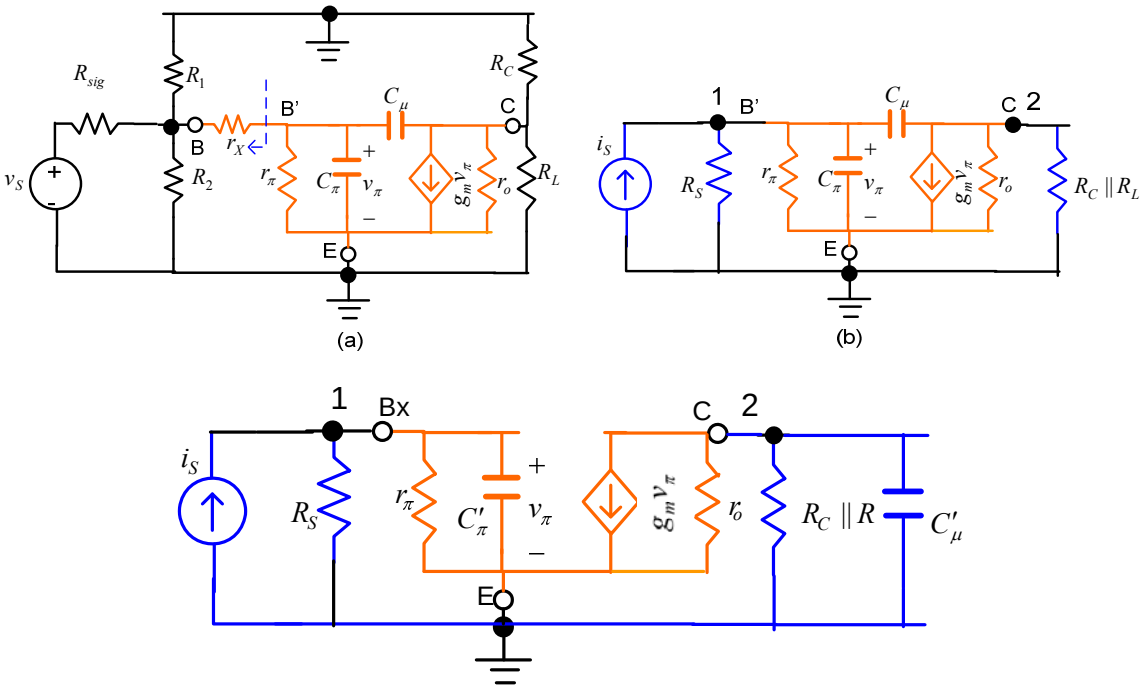

Figure 3.12: High frequency equivalent circuit of a CE-BJT device after application of Miller's theorem

In the above $C'_\pi = C_\pi + C_\mu(1-K)$, $C'_\mu = C_\mu(1-1/K)$. Figure 3.12 is a simple two node circuit and can be conveniently analyzed. Miller's theorem is very effective when the admittances $Y_1$ and $Y_2$ have one of their ends grounded for ac signals. After the equivalent circuit is simplified as above, one can apply the OCTC method to determine the high frequency poles.

*Example 3.5.2.1*: Consider Fig.3.13(a) which shows the high frequency equivalent circuit for the amplifier in Fig.3.9(a). Figure 3.13(b) is a reduced form of Fig.3.13(a), suitable for analysis by nodal matrix formulation. In Fig.3.13(b), the following expressions hold:

$$R_S = r_X + R_{sig} \,||\, R_1 \,||\, R_2, \quad i_S = v'_S / R_S, \quad v'_S = v_S \frac{R_B}{R_{sig} + R_B}, R_B = R_1 \,||\, R_2$$

(a) Calculate the *low frequency* voltage gain between nodes labeled 1 and 2 in Fig.3.13(b). This amounts to ignoring the presence of $C_\pi$ and $C_\mu$ for this calculation. Let this gain be K.




(c)

Figure 3.13: (a) high frequency equivalent circuit of the amplifier in Fig.3.9(a), (b) the equivalent circuit adjusted for nodal admittance matrix (NAM) analysis, (c) Transformed ac equivalent circuit after application of Miller's theorem.

(b) Use Miller's theorem to find the new circuit configuration in the form of Fig.3.12.

(c) Apply OCTC method to derive the pole frequencies for high frequency response of the amplifier.

(d) Given that $R_{sig}$ =50Ω, $R_1$=82 kΩ, $R_2$=47 kΩ, $r_X$ =10Ω, $g_m$ =40 m mhos, $r_o$=50 kΩ, $R_C$ =2.7 kΩ, $R_L$=4.7 kΩ, $R_E$=270 Ω, $h_{fe}$ (0)=$h_{FE}$= 49, $C_\pi$ =1.2 pF, $C_\mu$ =0.1 pF, find the high frequency poles by using

(i) The OCTC method discussed in section 3.5.1.

(ii) The OCTC method after applying Miller's theorem (introduced in section 3.5.2).

*Solution* :

By inspection of Fig.3.13(b), the voltage gain K=$v_2/v_1$=$v_2/v_\pi = -g_m r_o \| R_C \| R_L$ =-66.14

Further, recalling $g_m r_\pi = h_{fe}(0)$ =49, we get $r_\pi$ =1225 Ω.

**Part (c)** : $R_{Th\pi} = r_\pi \,||\, (r_x + R_{sig} \,||\, R_1 \,||\, R_2)$ =57.1 Ω. $\omega_{H1}$ =1/($C_\pi\, R_{Th\pi}$) =$14.59\times10^9$ rad/s

$R_{Th\mu}$ = $R_s$'+(1+$g_m R_s$')$R_L$' (see derivations in 3.5.1)=5503.5 Ω, $\omega_{H2}$ = 1/ $C_\mu R_{Th\mu}$ =1.817 $\times10^9$ rad/sec. The above is the result by OCTC method *without taking recourse to Miller's theorem.*

**Part (b):** Using Miller's theorem the equivalent circuit of Fig.3.13(b) transform to figure 3.13(c). Using K=-66.14, the new capacitance values become:

$$C'_\pi = C_\pi + C_\mu(1-K) = 7.93\times10^{-12}, \quad C'_\mu = C_\mu(1-{}^1\!/_K) = 1.01\times10^{-13}$$

Now, we need to recalculate the Thevenin resistances $R'_{Th\pi} = r_\pi \,||\, R_S = 59.9\,||1225 = 57\,\Omega$,

$R'_{Th\mu} = R_C \,||\, R_L \,||\, r_o = 1658\,\Omega$.

Then, $\omega'_{H1} = {}^1\!/_{C'_\pi R'_{Th\pi}} = 2.21\times10^9$ rad/sec, and $\omega'_{H2} = {}^1\!/_{C'_\mu R'_{Th\mu}} = 5.94\times10^9$ rad/sec.

**Part d(i):** Since $\omega_{H2}$ is << $\omega_{H1}$, $\omega_{H2}$ is the *dominant* high-frequency pole for the amplifier. Hence the -3dB frequency is approximately $1.817\times10^9$ rad/sec, i.e., the *dominant* high frequency pole of the system.

**Part d(ii):** Since the $\omega'_{H1}$, $\omega'_{H2}$ values are not widely apart (i.e., differ by a factor of 5 or more), we will estimate the higher -3dB frequency by adopting the formula

$$\omega'_H = \frac{1}{C'_\pi R'_{Th\pi} + C'_\mu R'_{Th\mu}} = 1.6118\times10^9 \text{ rad/sec.}$$

**Part d(i) revised**: If we had used the same formula with the values found in **part (c),** we would get $\omega_H = \dfrac{1}{C_\pi R_{Th\pi} + C_\mu R_{Th\mu}} = 1.6157\times10^9$ rad/sec.

*Conclusion:* In practice the more conservative value should be chosen, i.e., the upper -3 dB frequency will be $1.6118\times10^9$ rad/sec.

### 3.5.3 Transfer function analysis method

The time-constant methods discussed above lead to determination of the poles (and zeros) of the transfer function. We need yet to determine the mid-band gain function and combine this with the poles (and zeros) to form the overall transfer function for high (or low) frequency response of the amplifier. This involves a two-step process. Alternatively,

we can apply nodal matrix analysis (see *Appendix III*) technique to determine the overall transfer function as the first operation. Since the high frequency equivalent circuit of the transistor has two capacitors, the transfer function will be of order two in 's' (i.e., second degree in 's'). For such a transfer function there exists a simple rule to determine the *dominant* pole of the transfer function. Further, by ignoring the frequency dependent terms (i.e., coefficients of $s$ ) in the transfer function, we can derive the mid-band gain of the system. Hence the transfer function analysis opens up avenues for deriving several important network functions for the amplifier on hand. Following examples illustrate several cases.

*Example 3.5.3.1: Derivation of the voltage gain transfer function of a CE-BJT amplifier*

Consider the ac equivalent circuit of the BJT CE amplifier of Fig.3.9(a) which is re-drawn in Fig.3.14(a) for convenience. Applying Thevenin-Norton equivalence principle to the left of the arrow-head (in blue), we can convert the circuit in Fig.3.14(a) to

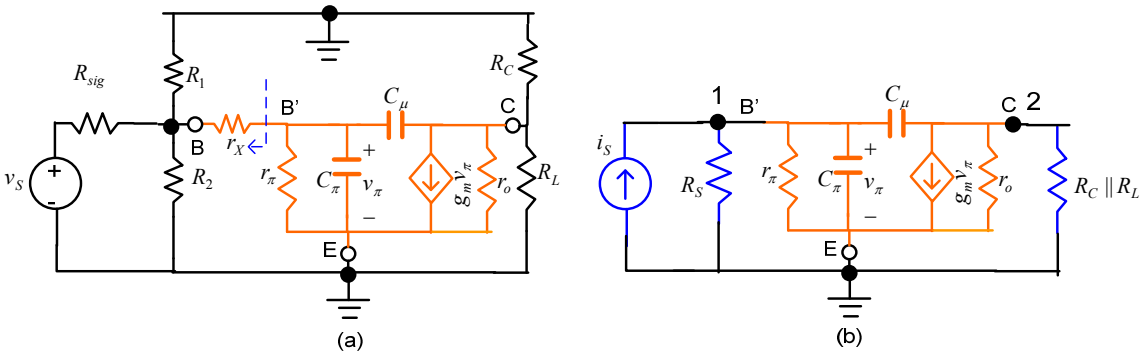



Figure 3.14: (a) high frequency equivalent circuit of the complete amplifier, (b) the equivalent circuit adjusted for nodal admittance matrix (NAM) analysis.

Fig.3.14(b), which is convenient for nodal analysis (i.e., it has fewer number of nodes and is driven by a current source. In Fig. 3.13(b) note that

$$R_S = r_X + R_{sig} \| R_1 \| R_2, \quad i_S = v_S' / R_S, \quad v_S' = v_S \frac{R_B}{R_{sig} + R_B}, R_B = R_1 \| R_2 \qquad (3.15)$$

Using the notations $g_S = 1/R_S$, $g_\pi = 1/r_\pi$, $R_C' = R_C \| R_L$, $g_C' = 1/R_C'$, and so on, we can formulate the admittance matrix for the two nodes (labeled as 1,2) system in Fig.3.13(b). Thus,

$$\begin{bmatrix} g_S + g_\pi + s(C_\pi + C_\mu) & -sC_\mu \\ -sC_\mu & g_o + g_C' + sC_\mu \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} i_S \\ -g_m v_\pi \end{bmatrix} \qquad (3.16)$$

Noting that $v_\pi = V_1$, and bringing $-g_m v_\pi$ ($=g_m V_1$) on the left side inside the matrix,

$$\begin{bmatrix} g_S + g_\pi + s(C_\pi + C_\mu) & -sC_\mu \\ g_m - sC_\mu & g_o + g'_C + sC_\mu \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} i_S \\ 0 \end{bmatrix} \qquad (3.17)$$

The output signal voltage of the system is $v_o = V_2$, given by

$$v_o = V_2 = \frac{\begin{vmatrix} g_S + g_\pi + s(C_\pi + C_\mu) & i_S \\ g_m - sC_\mu & 0 \end{vmatrix}}{\begin{vmatrix} g_S + g_\pi + s(C_\pi + C_\mu) & -sC_\mu \\ g_m - sC_\mu & g_o + g'_C + sC_\mu \end{vmatrix}} \qquad (3.18)$$

On carrying out the tasks of evaluation of the determinants, one can find

$$v_o = \frac{-i_S(g_m - sC_\mu)}{s^2 C_p C_\mu + s(g_S C_\mu + g_\pi C_\mu + g_o C_\mu + g'_C C_\mu + g_m C_\mu + g_o C_\pi + g'_C C_\pi) + g_S g_o + g_S g'_C + g_\pi g_o + g_\pi g'_C}$$

Writing $D(s)$ =

$s^2 C_p C_\mu + s(g_S C_\mu + g_\pi C_\mu + g_o C_\mu + g'_C C_\mu + g_m C_\mu + g_o C_\pi + g'_C C_\pi) + g_S g_o + g_S g'_C + g_\pi g_o + g_\pi g'_C$,

and substituting for $i_S$ we find $v_o = -\frac{g_m - sC_\mu}{D(s)} \frac{1}{r_X + R_{sig} \| R_B} \frac{R_B}{R_B + R_{sig}} v_S \qquad (3.19)$

The voltage gain transfer function is: $T(s) = \frac{v_o}{v_S} = -\frac{g_m - sC_\mu}{D(s)} \frac{1}{r_X + R_{sig} \| R_B} \frac{R_B}{R_B + R_{sig}}$ (3.20)

We can make two important derivations from the result in (3.20)

- *Low-frequency voltage gain* $A_M$ : This is obtained from (3.20) on approximating $\omega \rightarrow 0$, i.e., $s \rightarrow 0$.

  Thus $A_M = -\frac{g_m}{g_S g_o + g_S g'_C + g_\pi g_o + g_\pi g'_C} \frac{R_B}{(r_X + R_{sig} \| R_B)(R_B + R_{sig})} \qquad (3.21)$

Assuming the component and device parameter values as in *Example 3.5.2.1*, we get $A_M$ =-63.12

- High frequency dominant pole $\omega_{HD}$

When the denominator *D(s)* of the transfer function is of second order, one can estimate the dominant pole from the least valued root of the denominator polynomial. The technique is explained as follows.

We can write *D(s)* in the form : $s^2 + bs + c$. Then the high frequency dominant pole (i.e., the pole with the least magnitude of all the high frequency poles) is given by $\omega_{pD} = c/b$

i.e., the *ratio of the constant term* in *D(s)* to the *coefficient of the s term* in *D(s)*. This follows easily by writing $s^2+bs+c=(s+\alpha)(s+\beta)=s^2+(\alpha+\beta)s+\alpha\beta$. Then, $\alpha+\beta=b\cong\beta$, if α<< β. Further, from $\alpha\beta=c$, we deduce $\alpha=c/\beta\cong c/b$, as the dominant pole of the voltage gain transfer function. Hence,

$$\omega_{HD} = (g_S g_o + g_S g'_C + g_\pi g_o + g_\pi g'_C)/(g_S C_\mu + g_\pi C_\mu + g_o C_\mu + g'_C C_\mu + g_m C_\mu + g_o C_\pi + g'_C C_\pi) \quad (3.22)$$

Consider the voltage gain function of the CE BJT amplifier in *Example 3.5.2.1* as an illustration. We can find $\omega_{HD}$ approximate the by substituting the values for the pertinent parameters $g_S$, $g_o$, and so on. Thus, the upper cut-off frequency (i.e., upper -3dB frequency) is calculated as $1.6158\times10^9$ rad/sec. The student may compare this value with the values obtained previously, i.e., $1.6157\times10^9$ rad/sec (using OCTC method), and $1.6118\times10^9$ rad/sec (using Miller's theorem followed by OCTC method), respectively.

*Example 3.5.3.2: Derivation of the voltage gain transfer function* (VTF) *of a* CB-BJT *amplifier*

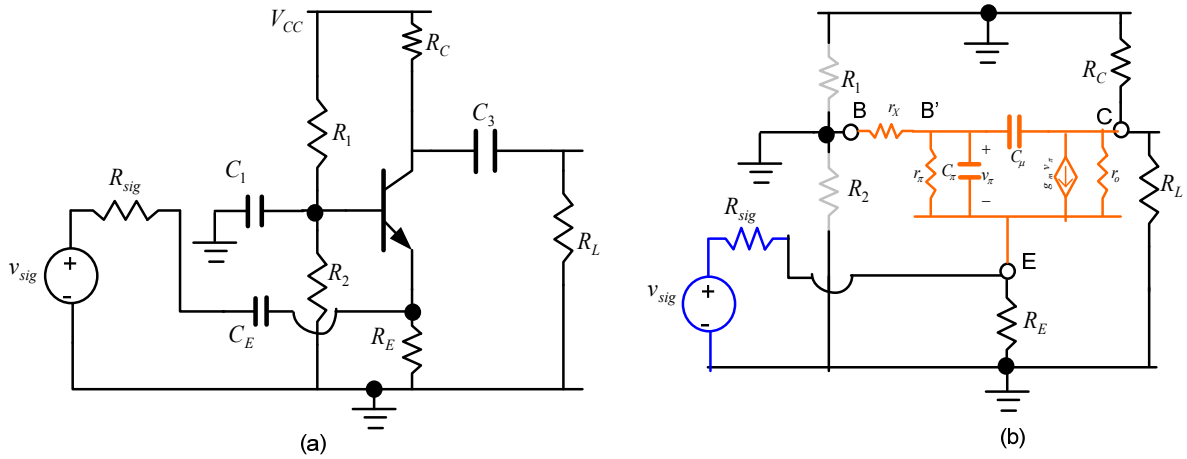



Figure 3.15: (a) Schematic of the CB-BJT amplifier stage, (b) the high-frequency equivalent circuit.

Figures 3.15(a)-(b) depict respectively the schematic and high frequency equivalent circuits of the CB amplifier stage. All coupling and by-pass capacitors behave as short circuits and hence they do not appear in Fig.3.15(b).

For nodal admittance matrix (NAM) formulation we need to transform the voltage source with its internal resistance to its Norton equivalent, i.e., a signal current source $i_S = v_{sig}/R_{sig}$ in parallel with $R_{sig}$ (the student is encouraged to complete this part to modify Fig.3.15(b)). The NAM by inspection will be:

$$\begin{bmatrix} g_{sig}+g_E+g_\pi+g_o+sC_\pi & -g_\pi-sC_\pi & -g_o \\ -g_\pi-sC_\pi & g_x+g_\pi+sC_\pi+sC_\mu & -sC_\mu \\ -g_o & -sC_\mu & g_o+g'_C \end{bmatrix} \begin{bmatrix} v_E \\ v_{B'} \\ v_C \end{bmatrix} = \begin{bmatrix} i_S \\ 0 \\ -g_m v_\pi \end{bmatrix} \quad (3.23)$$

But $v_\pi = v_{B'} - v_E$. Hence (3.23) reduces to

$$\begin{bmatrix} g_{sig}+g_E+g_\pi+g_o+sC_\pi & -g_\pi-sC_\pi & -g_o \\ -g_\pi-sC_\pi & g_x+g_\pi+sC_\pi+sC_\mu & -sC_\mu \\ -g_m-g_o & g_m-sC_\mu & g_o+g'_C+sC_\mu \end{bmatrix} \begin{bmatrix} v_E \\ v_{B'} \\ v_C \end{bmatrix} = \begin{bmatrix} i_S \\ 0 \\ 0 \end{bmatrix} \quad (3.24)$$

In order to compare the performance of the CB and CE BJT amplifiers, it will be convenient to assume $r_X$ as negligible. Then node *B'* will be at *zero* ac potential and (3.24) will approximate to (by discarding the *row* and *column* associated with the ***B'*** node)

$$\begin{bmatrix} g_{sig}+g_E+g_\pi+g_o+sC_\pi & -g_o \\ -g_m-g_o & g_o+g'_C+sC_\mu \end{bmatrix} \begin{bmatrix} v_E \\ v_C \end{bmatrix} = \begin{bmatrix} i_S \\ 0 \end{bmatrix} \quad (3.25)$$

The VTF is given by

$$v_o/v_{sig} = v_C/v_{sig} = \frac{g_{sig}(g_m+g_o)}{s^2C_\pi C_\mu + s[C_\pi(g_o+g'_C)+C_\mu(g_\pi+g_E+g_{sig}+g_o)]+g_o(g_{sig}+g_\pi+g_E+g'_C-g_m)+g'_C(g_{sig}+g_E+g_o+g_\pi)}$$

Using the VTF we can deduce

- The mid-band gain (i.e., $s \rightarrow j\omega$, $\omega \rightarrow 0$) for CB mode of operation is:

$$A_M|_{CB} = \frac{g_{sig}(g_m+g_o)}{g_o(g_{sig}+g_\pi+g_E+g'_C-g_m)+g'_C(g_{sig}+g_E+g_o+g_\pi)} \quad (3.26)$$

- The dominant high frequency pole for CB mode of operation is

$$\omega_{HD}|_{CB} = \frac{g_o(g_{sig}+g_\pi+g_E+g'_C-g_m)+g'_C(g_{sig}+g_E+g_o+g_\pi)}{C_\pi(g_o+g'_C)+C_\mu(g_\pi+g_E+g_{sig}+g_o)} \quad (3.27)$$

*Example 3.5.3.3: Determine the mid-band gains and dominant high frequency poles of the BJT amplifier operated as CE (see Fig.3.9a) and CB (see Fig.3.15a) modes of operation. The devices, the DC biasing conditions, and the circuit components are assumed identical for both the configurations.*

[Given $R_{sig}$ =50Ω, $R_1$=82 kΩ, $R_2$=47 kΩ, $R_E$=270 Ω, $R_C$ =2.7 kΩ, $R_L$=4.7 kΩ

$g_m$ =40 m mhos, $r_o$=50 kΩ, $r_X$ =10Ω ,$h_{fe}(0)=h_{FE}$ = 49

$C_\pi$ =1.2 pF, $C_\mu$ =0.1 pF]

On substitution into the expressions (3.26) and (3.27), we get: $A_M$ =57.17 v/v, $\omega_{HD}|_{CB}=4.5796\times10^9$ rad/sec.

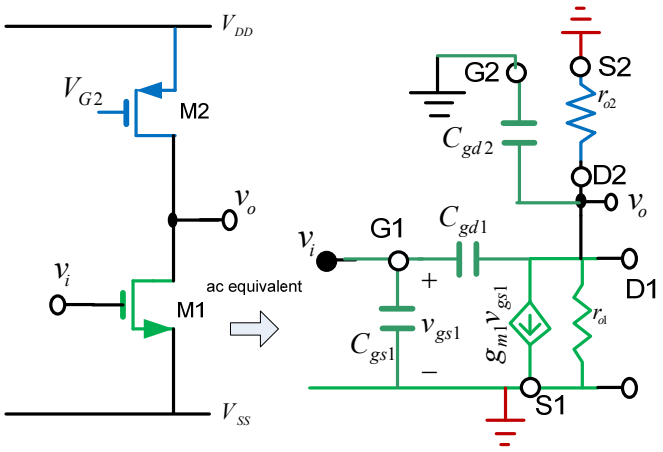
***Note I****:* We observed that the CB-BJT amplifier has somewhat *lower voltage gain* (i.e., 57.17) compared with that of CE-BJT (i.e., 63.12 in magnitude) amplifier, but has a *higher high-frequency bandwidth* (~ dominant high-frequency pole=$4.5796\times10^9$ rad/sec) compared with that of CE-BJT (i.e., $1.6158\times10^9$ rad/sec) amplifier.

***Note II****:* It is known that the CE-BJT amplifier as moderate to high (kΩ to tens of kΩ) input resistance, as well as moderately high (kΩ) output resistance. In comparison, a CB-BJT amplifier has low (Ω to tens of Ω) input resistance while a moderately high (kΩ) output resistance.

***Note III:*** A CB-BJT is preferred over a CE-BJT amplifier for most *radio-frequency* (MHz and above) applications because it has a *higher* high-frequency bandwidth (for identical device and biasing conditions), and affords to provide better impedance matching at the input with the *radio-frequency* (RF) source ($R_{sig}$ in the range of 50Ω to 75Ω).

*Example 3.5.3.4: Derivation of the voltage gain transfer function* (VTF) *of a* CS-MOSFET *amplifier with active load*

Consider figures 3.16(a)-(b) which depict respectively the schematic of a CS-MOSFET amplifier and the associated high frequency equivalent circuit.




(a) (b)

Figure 3.16: (a) Schematic of a CS-MOSFET amplifier with active load, (b) associated high-frequency equivalent circuit.

Using a dummy input current source $i_x$ (when not shown explicitly, the student should adopt this principle), the admittance matrix is

$$\begin{bmatrix} s(C_{gs1}+C_{gd1}) & -sC_{gd1} \\ -sC_{gd1} & g_{o1}+g_{o2}+s(C_{gd1}+C_{gd2}) \end{bmatrix}\begin{bmatrix} v_i \\ v_o \end{bmatrix}=\begin{bmatrix} i_x \\ -g_{m1}v_{gs1} \end{bmatrix} \qquad (3.28)$$

After re-arranging (the student is suggested to work out the details), we can find the VTF given by

$$\frac{v_o}{v_i}=\frac{\begin{vmatrix} s(C_{gs1}+C_{gd1}) & i_x \\ g_m-sC_{gd1} & 0 \end{vmatrix}}{\begin{vmatrix} i_x & -sC_{gd1} \\ 0 & g_{o1}+g_{o2}+s(C_{gd1}+C_{gd2}) \end{vmatrix}} \qquad (3.29)$$

*Exercise* 3.5.3.4*:* Can you sketch the Bode magnitude plot for the above VTF? Assume, $g_m$=250 µA/V, $r_{o1}$, $r_{o2}$ =1 MΩ (each), $C_{gd1}$, $C_{gd2}$= 20 fF (each f→ femto i.e., $10^{-15}$), $C_{gs1}$= 100 fF.

*Example 3.5.3.5: Derivation of the voltage gain transfer function* (VTF) *of a* CG-MOSFET *amplifier.*

Figures 3.17(a)-(b) show the schematic diagrams of a CG-MOSFET amplifier (M1) under *ideal* loading and *practical* loading conditions respectively. Figure 3.17(c) depict the high frequency equivalent circuit. Note that now we need to include the body-

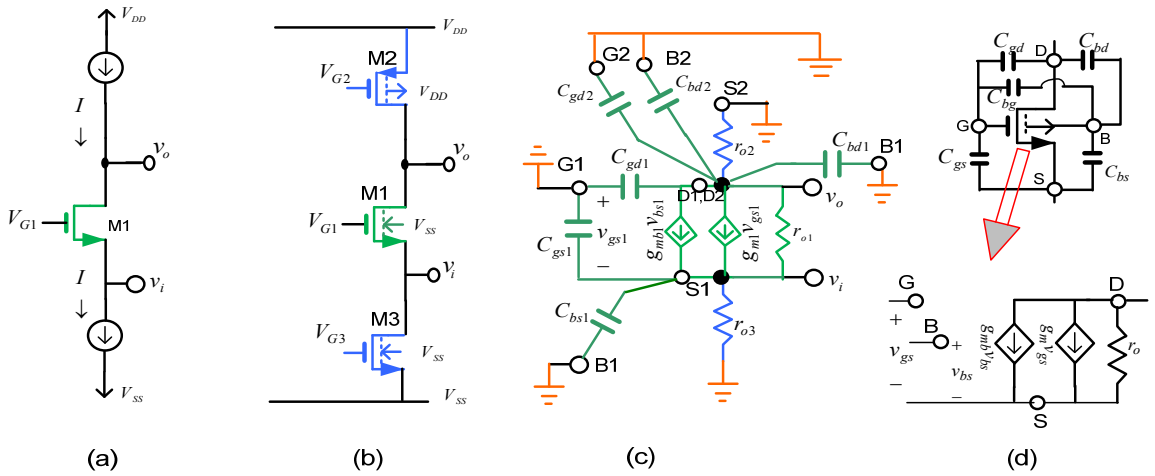



Figure 3.17: (a) Schematic of the CG-MOSFET amplifier with ideal load and bias source, (b) practical biasing and active load arrangement, (c) high-frequency equivalent circuit model for the CG-MOSFET stage, (d) more complete high-frequency model for a MOSFET.

transconductance $g_{mb}$ of the MOSFET, since the topology is such (i.e., the amplifying device is in a *totem pole* connection) that the source and body terminals of the amplifying transistor M1 cannot be connected together!

It may be noted that despite the complicated look of Fig.3.17(c), there are only two signal nodes in the equivalent circuit. Thus the nodal admittance matrix will appear as:

$$\begin{bmatrix} g_{o3}+g_{o1}+s(C_{gs1}+C_{bs1}) & -g_{o1} \\ -g_{o1} & g_{o1}+g_{o2}+s(C_{bd1}+C_{gd1}+C_{bd2}+C_{gd2}) \end{bmatrix}\begin{bmatrix} v_i \\ v_o \end{bmatrix}=\begin{bmatrix} i_x+g_{m1}v_{gs1}+g_{mb1}v_{bs1} \\ -g_{m1}v_{gs1}-g_{mb1}v_{bs1} \end{bmatrix}$$

Writing $C_1=C_{gs1}+C_{bs1}$, $C_2=C_{gd1}+C_{bd1}+C_{gd2}+C_{bd2}$, and observing that the gate and body terminals of the MOSFETs are at *zero* ac potentials so that $v_{gs1}=-v_{s1}=-v_i$, $v_{bs1}=-v_{s1}=-v_i$, we can re-write the admittance matrix equation as

$$\begin{bmatrix} g_{o3}+g_{o1}+sC_1 & -g_{o1} \\ -g_{o1} & g_{o1}+g_{o2}+sC_2 \end{bmatrix}\begin{bmatrix} v_i \\ v_o \end{bmatrix}=\begin{bmatrix} i_x-g_{m1}v_i-g_{mb1}v_i \\ g_{m1}v_i+g_{mb1}v_i \end{bmatrix} \qquad (3.30)$$

Re-arranging, we get

$$\begin{bmatrix} g_{o3}+g_{o1}+g_{m1}+g_{mb1}+sC_1 & -g_{o1} \\ -g_{m1}-g_{mb1}-g_{o1} & g_{o1}+g_{o2}+sC_2 \end{bmatrix}\begin{bmatrix} v_i \\ v_o \end{bmatrix}=\begin{bmatrix} i_x \\ 0 \end{bmatrix} \qquad (3.31)$$

The VTF is given by:

$$\frac{v_o}{v_i} = \frac{\begin{vmatrix} g_{o3}+g_{o1}+g_{m1}+g_{mb1}+sC_1 & i_x \\ -g_{m1}-g_{mb1}-g_{o1} & 0 \end{vmatrix}}{\begin{vmatrix} i_x & -g_{o1} \\ 0 & g_{o1}+g_{o2}+sC_2 \end{vmatrix}} \qquad (3.32)$$

*Exercise* 3.5.3.5-I: *Find the explicit expression for the* VTF *using* (3.32).

*Exercise* 3.5.3.5-II: *Using* (3.31), *and the knowledge that the driving point impedance* (DPI) *at the input is given by* $Z_{dpi} = v_i / i_x$, *find the expression for the* $Z_{dpi}$.

*Exercise* 3.5.3.5-III: *Given that* $r_{o1} = r_{o3} = 1M\Omega$, $r_{o2} = 2M\Omega$, $g_{m1} = 200\mu mho$, $g_{mb1} = 0.2g_{m1}$, $C_{gs1} = 100\,fF$, $C_{bs1} = 20\,fF$, $C_{gd1} = 5\,fF$, $C_{bd1} = 20\,fF$, $C_{gd2} = 10\,fF$, $C_{bd2} = 15\,fF$ *find the expressions for the* VTF *and the* $Z_{dpi}$

*Exercise* 3.5.3.5-IV: *Find the expression for the trans-impedance function* TIF $(= v_o / i_x)$ *for the amplifier stage*.

*Example 3.5.3.6*: *Derivation of the voltage gain transfer functions* (VTF) *for a CC-BJT and CD-MOSFET amplifiers*

Figures 3.18(a)-(d) show respectively the schematic and high frequency equivalent circuits of a CC-BJT and CD-MOSFET amplifiers. The biasing/loading is arranged by

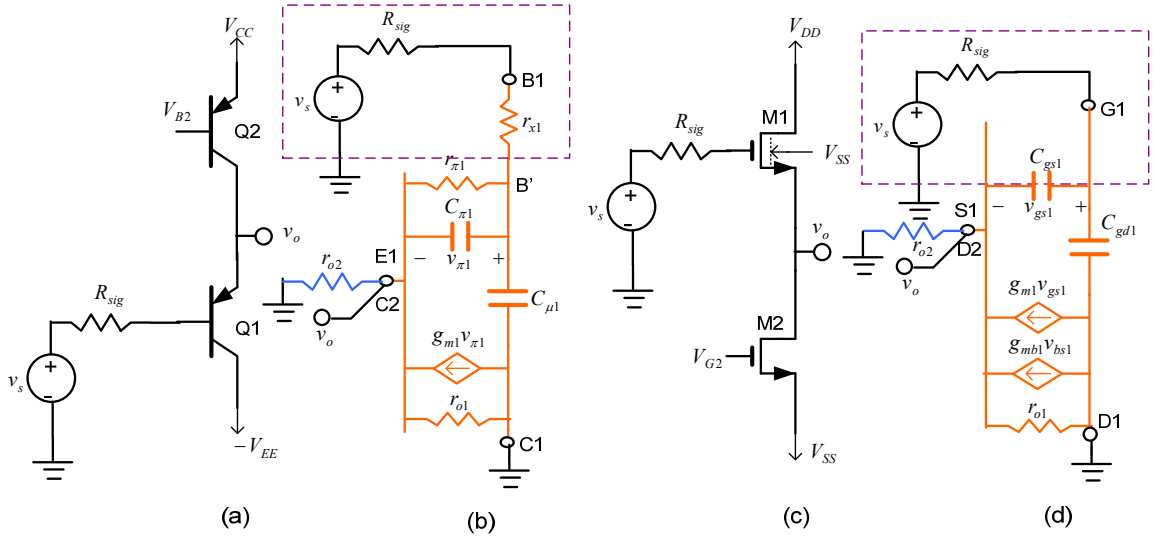


Figure 3.18: (a) Schematic of a CC-BJT amplifier, (b) high frequency equivalent circuit of the CC amplifier, (c) Schematic of a CD-MOSFET amplifier, (d) high frequency equivalent circuit of the CD amplifier

employing active resistors (Q2 in Fig.3.18(a), and M2 in Fig.3.18(c)). It may be noted that since one terminal of the capacitor $C_{\mu 1}$ (and of $C_{gd1}$) is grounded for *ac*, neither of these capacitors are subjected to the *Miller* effect magnification, as are in the cases with CE (BJT and CS (MOSFET) amplifiers.

*The student is encouraged to complete the analysis and derive the expressions for the VTF $v_o/v_s$ of the CC and the CD amplifiers.Remember that for the MOSFET the body terminal is connected to a DC voltage.*

## 3.6: Wide band multi-stage amplifiers

### 3.6.1: CE-CB Cascode BJT amplifier

It has been known that a CE stage has high voltage gain and high input resistance while a CB stage has high voltage gain with low input resistance. For high frequency operation CE amplifier will have a smaller band width than the CB amplifier since in the former the capacitance $C_\mu$ is magnified due to Miller effect. This has a corresponding effect on reducing the band width. In the CB stage, since the base is at ac ground, the capacitance $C_\mu$ has already one terminal to ground and is not subjected to Miller effect magnification. So the CB stage affords to higher operating band width.

It is interesting to consider a composite amplifier containing the CE and CB stages so that advantages of both the configurations could be shared. That is what happens in a cascode amplifier where the CE stage receives the input signal, while the CB stage acts as a low

resistance load for the CE stage. Because of the low resistance load, the Miller effect magnification of the $C_\mu$ capacitor in the CE stage is drastically reduced. Because of the low resistance load, however, the voltage gain in the CE stage drops. But it is adequately compensated by the large voltage gain of the CB stage which works from a low input resistance to a high output resistance.

*3.6.1.1: Analysis for the bandwidth and mid-band gain*

The schematic connection of a cascode amplifier and the associated ac equivalent circuit are in Figures 3.19(a)-(b). The equivalent circuit has *six* nodes. Converting the signal source in series with $R_{sig}$ and $r_{X1}$ to its Norton equivalent will bring the number of nodes to *four*. For the *common base* transistor Q2 we can ignore $r_{X2}$ as very small (~ zero). Thus the number of nodes reduce to *three*. These are labeled as nodes 1,2,3 in Fig.3.19(b). For quick hand analysis we can adopt the following simplification procedure.

We can now introduce the assumption that $r_{o2}$ is very large (→infinity), and remove it. This separates node#2 and #3 with the controlled current source $g_{m2}v_{\pi 2}$ split into two parts- one running from node#3 to ground, and the other from ground to node#2.

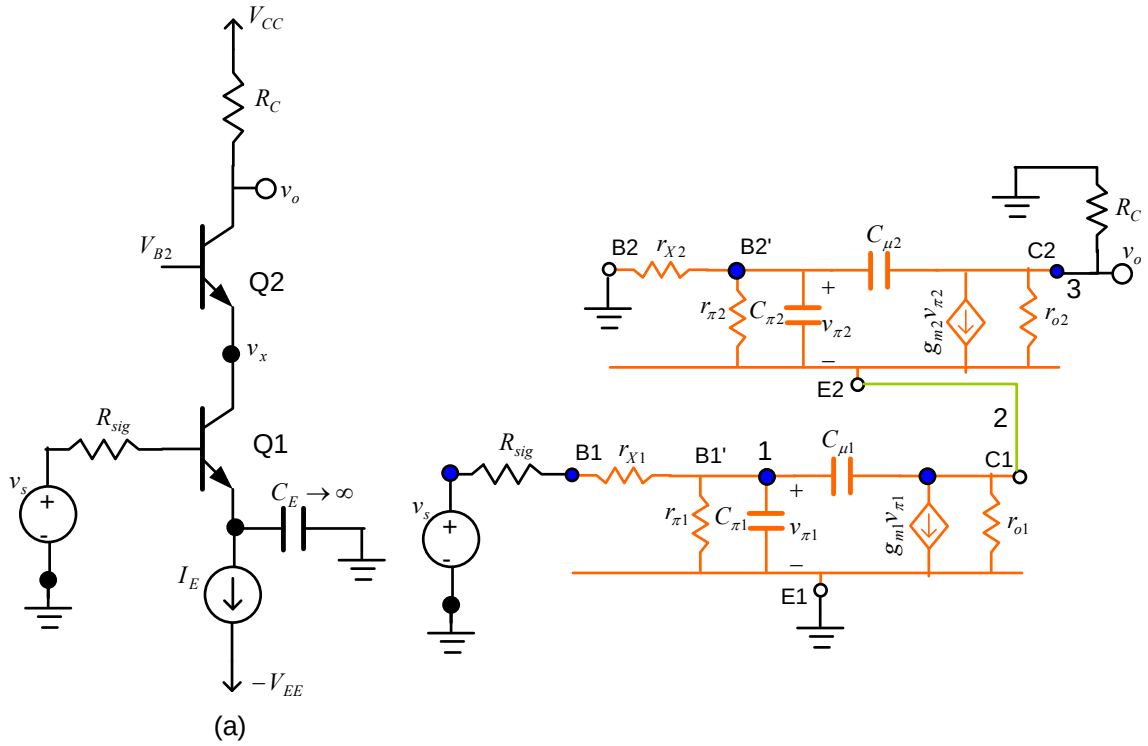


Figure 3.19: (a) Schematic of a CE-CB cascode amplifier, (b) high frequency equivalent circuit.

The simplified equivalent circuit appears in figure 3.20.

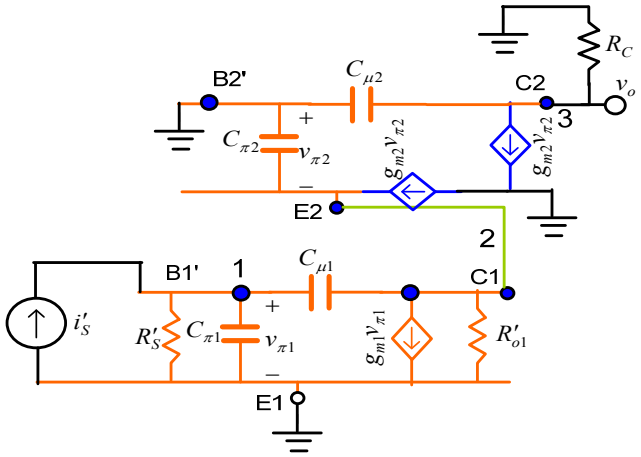



Figure 3.20: Simplified high frequency equivalent circuit for the CE-CB cascode amplifier.

In Fig.3.20 we have used $R'_S = (R_{sig} + r_{X1}) \| r_{\pi 1}$, $R'_{o1} = r_{o1} \| r_{\pi 2}$.

A careful scrutiny of the controlled current source $g_{m2}v_{\pi 2}$ between ground to node #2 and the fact that the controlling voltage $v_{\pi 2}$ is also effective across the same pair of nodes with the positive terminal at ground (node labeled $B'_2$) reveals that the controlled current source $g_{m2}v_{\pi 2}$ can be equivalently replaced by a conductance of $g_{m2}$ (i.e., resistance $1/g_{m2}$) connected across node#2 and ground. This observation leads to the equivalent circuit shown in figure 3.21.

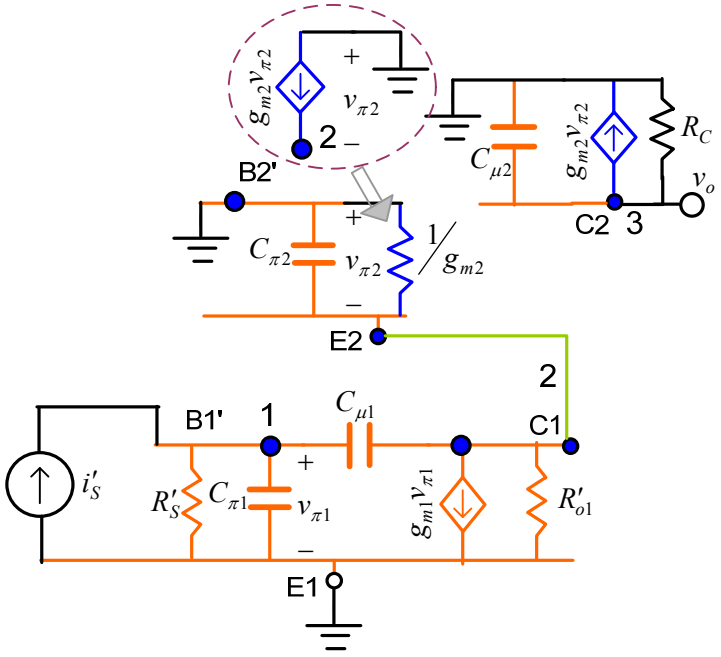



Figure 3.21: Conversion of Fig.3.20 after relocation of the controlled current source segments $g_{m2}v_{\pi 2}$ each.

Now we can apply the Miller effect magnification consideration to the floating capacitor $C_{\mu 1}$ running between nodes #1 and #2. The voltage gain between these nodes is (ignoring the feed-forward current through $C_{\mu 1}$ which is a very small capacitance) approximately given by the product of -$g_{m1}$ and $R'_{o1} \| 1/g_{m2}$. Considering the fact that $R'_{o1} = r_{o1} \| r_{\pi 2} \approx r_{\pi 2}$, and that $r_{\pi 2} >> 1/g_{m2}$, we can approximate $R'_{o1} \| 1/g_{m2}$ as $\approx 1/g_{m2}$. Hence the Miller magnification turns out to be $K \approx -g_{m1}/g_{m2}$, which is very close to $-1$ when the transistors Q1 and Q2 are matched to each other. By the principle of Miller effect the floating capacitor $C_{\mu 1}$ can now be replaced by two grounded capacitor of value $C_{\mu 1}(1\text{-}K)$, i.e., 2 $C_{\mu 1}$ at node #1, and $C_{\mu 1}(1\text{-}1/K)$, i.e., 2 $C_{\mu 1}$ at node#2. This leads to the final simplified form of the equivalent circuit as in figure 3.22.

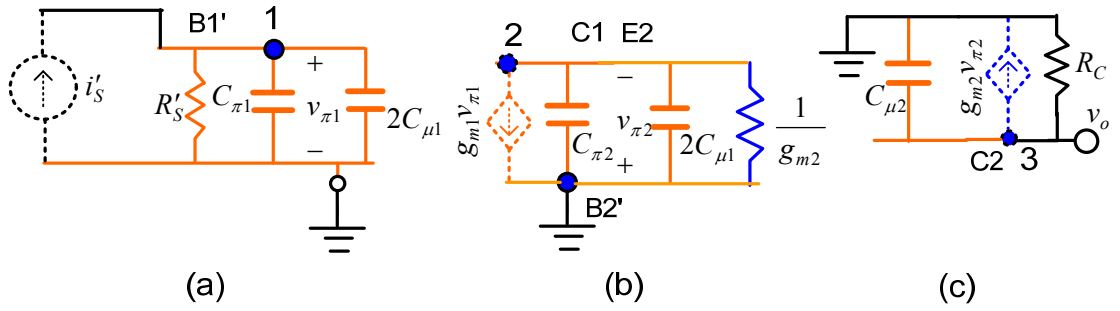



Figure 3.22: Final simplified high frequency equivalent circuit for the cascode amplifier.

Figure 3.22 present *three* disjoint sub-circuits with *three* distinct time constants. For Fig.3.22(a), the time constant is $\tau_a = (C_{\pi 1} + 2C_{\mu 1})R'_S$. For Fig.3.22(b) and (c) the time constants are respectively, $\tau_b = (C_{\pi 2} + 2C_{\mu 1})\dfrac{1}{g_{m2}}$, and $\tau_c = C_{\mu 2}R_C$. The higher -3dB frequency is then $\omega_H = \dfrac{1}{\tau_a + \tau_b + \tau_c}$, which can be considered as the bandwidth of the CE-CB cascode amplifier.

The mid-band gain of the cascode amplifier can be obtained by ignoring all the capacitors (as open circuits) and considering the circuit in figure 3.23.

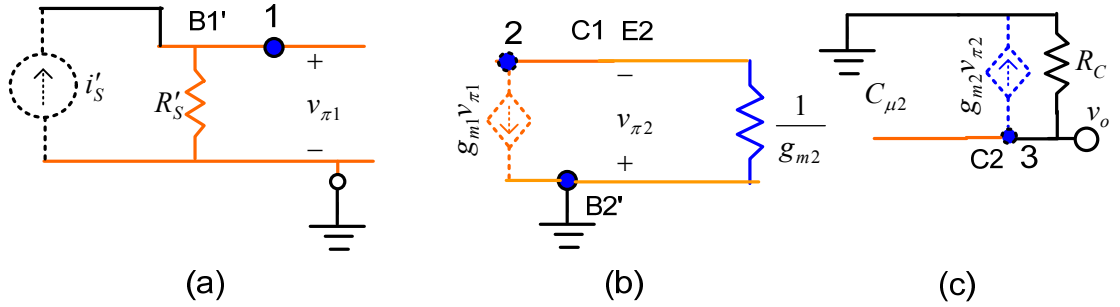



Figure 3.23: Equivalent circuit for the CE-CB cascode amplifier for mid-band (i.e., low frequency) gain calculation.

By inspection, $v_o = -g_{m2}R_C(g_{m1}\dfrac{1}{g_{m2}})R'_S\dfrac{v_s}{R_{sig}+r_{X1}} = -g_{m1}R_C\dfrac{r_{\pi 1}}{R_{sig}+r_{X1}+r_{\pi 1}}v_s$ (3.33)

The mid-band gain is then $\dfrac{v_o}{v_s} = A_M = -g_{m1}\dfrac{r_{\pi 1}}{R_{sig}+r_{X1}+r_{\pi 1}}R_C$ (3.34)

*Exercise 3.6.1.1.1:Consider an NPN BJT device with $h_{FE}$=100, $f_T$=6000 MHz, $C_\pi$= 25 pF biased to operate at $I_E$= 1 mA. Given that $r_X$=10 Ω, $V_A$ =50 V, and the signal source resistance $R_{sig}$ =100 Ω. The load resistance $R_C$ is 2.7 kΩ.*

*(a)The BJT is used as a CE amplifier with above given parameters. Find the mid-band gain $A_M$ , the upper cut-off frequency $f_{-3dB}$, and hence the Gain-Bandwidth (GBW) of the amplifier (*note: *GBW=$A_M$ times $f_{-3dB}$)*

*(b)Two matched BJT devices with above specifications are used to construct a CE-CB* ***cascode*** *amplifier. Find the mid-band gain $A_M$ , the upper cut-off frequency $f_{-3dB}$, and hence the Gain-Bandwidth (GBW) of the amplifier (*note: *GBW=$A_M$ times $f_{-3dB}$).*

*(c)How does the GBW$|_{CE}$ compare with the GBW$|_{Cascode}$* ?

(Hint: the student need to first determine *$g_m$, $r_\pi$, $r_o$, and $C_\mu$ for the BJT from the given information*)

*Example 3.6.1.1.2: On using a typical BJT devices from SPICE simulation library, we get the following results:*

| Amplifier mode | CE | CB | CE-CB cascode |
|---|---|---|---|
| Gain | 61.1 | 15.1 | 63.8 |
| Band width | 180.1MHz | 793.5MHz | 616.2MHz |

3.6.2 CS-CG MOSFET cascode amplifier

It is easy to construct a cascode of CS-CG amplifier stages using MOSFET devices. The schematic and the high frequency equivalent circuit are shown in figures 3.24(a)-(b) respectively. I should be noted that the source terminals of transistors M1,M2 cannot be connected to the respective body (substrate) terminals and hence the associated parasitic

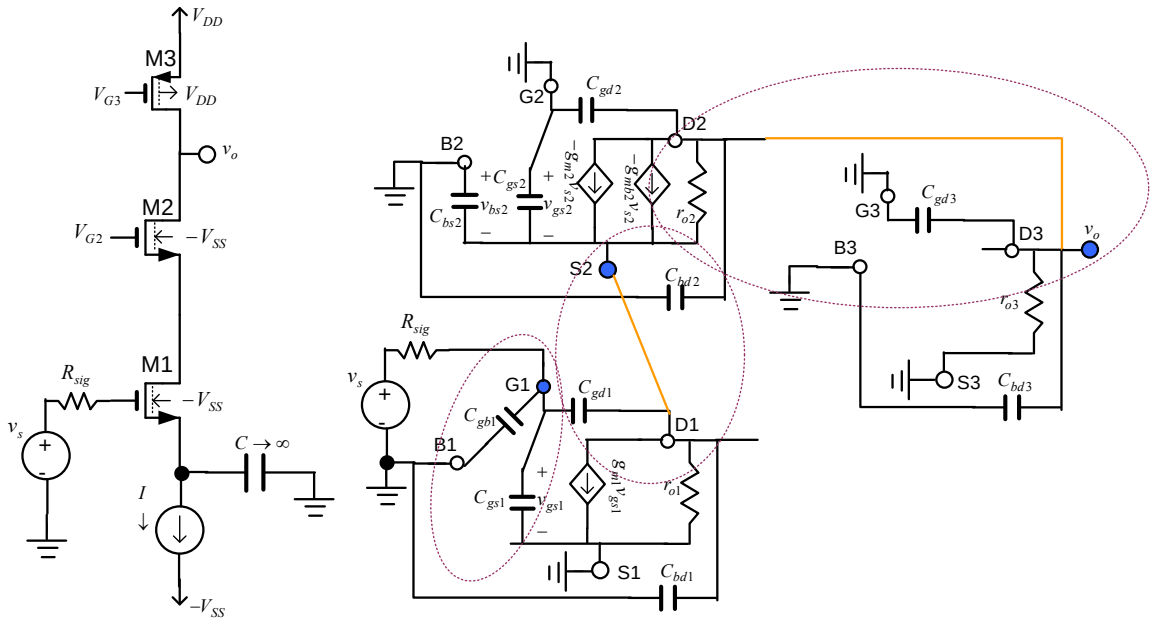



Figure 3.24: (a) Schematic of a CS-CG MOSFET cascode amplifier with active load and current source/mirror biasing, (b) high frequency equivalent circuit.

capacitances need be considered. For M1, however, since the S and B terminals are both at *ac* ground, the capacitance $C_{bs}$ is shorted out.

The equivalent circuit in Fig.3.24(b) has *three* ungrounded nodes (shown in blue shaded circles). The voltage gain $v_o/v_s$ can be calculated using standard nodal matrix formulation. Alternatively, the circuit can be simplified by adopting approximation procedures as used in the CS-CB cascode amplifier. This is left *as an exercise to the interested students*. Note that *Miller* magnification effect will be applicable to $C_{gd1}$.

### 3.6.3: Wide band differential amplifier with BJT devices

The cascode amplifier is single ended, i.e., has one terminal for signal input. It is of interest to investigate the possibility for a wide band differential amplifier. Towards this we can argue that a common differential amplifier with two CE stages accepting the differential input signals will not be desirable, because each CE stage will suffer degradation in high frequency performance because of Miller effect on $C_{\mu}$. In the following we discuss several possible configurations for wide-band differential amplifier.

*3.6.3.1: CE-CB cascode doublet as wide band differential amplifier*

The CE-CB cascode amplifier that we discussed already can be considered as a half circuit for constructing a differential amplifier. Figure 3.25 presents the schematic

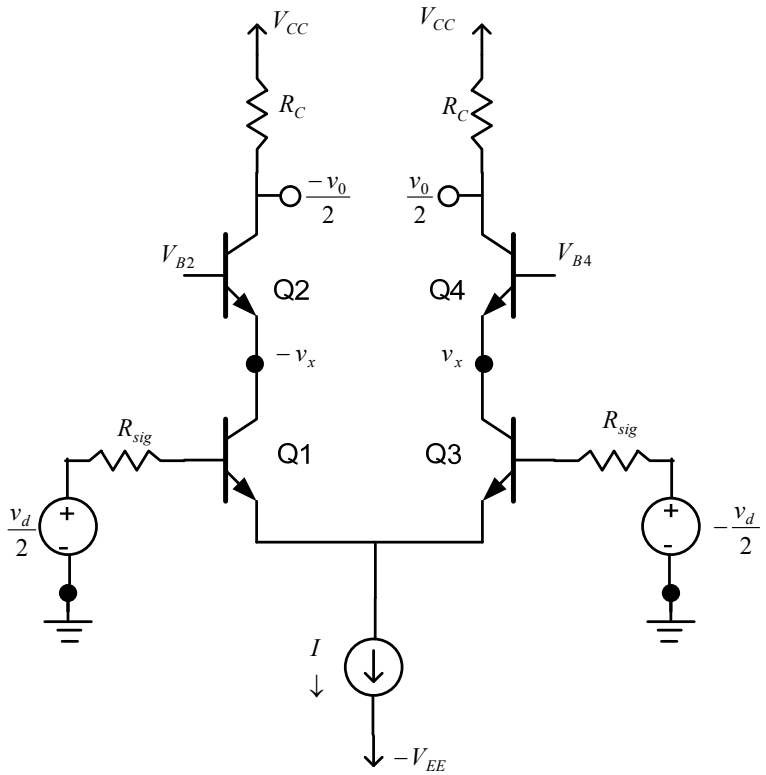



Figure 3.25: CE-CB cascode doublet as wide band differential amplifier

configuration. The analysis of the gain bandwidth (GBW) can be carried out as in the CE-CB cascode amplifier by considering only one half circuit of the configuration. The differential amplifier will preserve all the merits of the parent CE-CB cascode in addition to providing the special features of a differential amplifier (i.e., common mode rejection, removing even harmonic components)

*3.6.3.2: CC-CB cascade doublet as wide band differential amplifier*

The Miller magnification in a CE stage could be entirely removed if $R_C$ were zero. But that implies a CC stage, which has a low voltage gain (less but close to 1). The loss in voltage gain can be compensated partially, by cascading the CC stage with a CB stage. But then we are getting a voltage gain only from one stage. By using the CC-CB cascade

as a half circuit, it is possible to develop a wide band CC-CB doublet differential amplifier. The schematic is shown in figure 3.26.

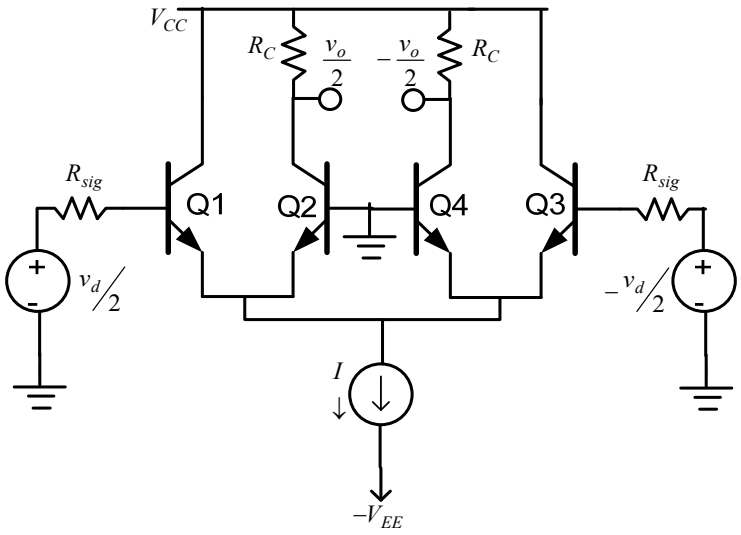



Figure 3.26: A CC-CB cascade doublet wide band differential amplifier.

The amplifier in Fig.3.26 will provide wide band operation with good voltage gain. But there are four transistors which need be supplied with DC bias current. The DC power consumption will be high. A *totem-pole* configuration where two transistors are stacked in one column will result in a lower DC power consumption. This is possible by using complementary (i.e., NPN and PNP) transistors to form the CC-CB cascade. Figure 3.27 presents the configuration.

*3.6.3.3: CC-CB cascade doublet differential amplifier with complementary transistors*

In the configuration of Fig.3.27 DC bias current is to be supplier only to two columns of transistors. So compared with Fig.3.26, the complementary CC-CB cascade doublet differential amplifier (Fig.3.27) will consume less DC power.

- *Analysis for gain bandwidth*

A simplified analysis for the band width of the differential amplifier can be carried out on the assumption that the NPN and the PNP transistors are matched pairs (it is *seldom true* in practice) and then working on one half circuit of the system. Thus considering the pair

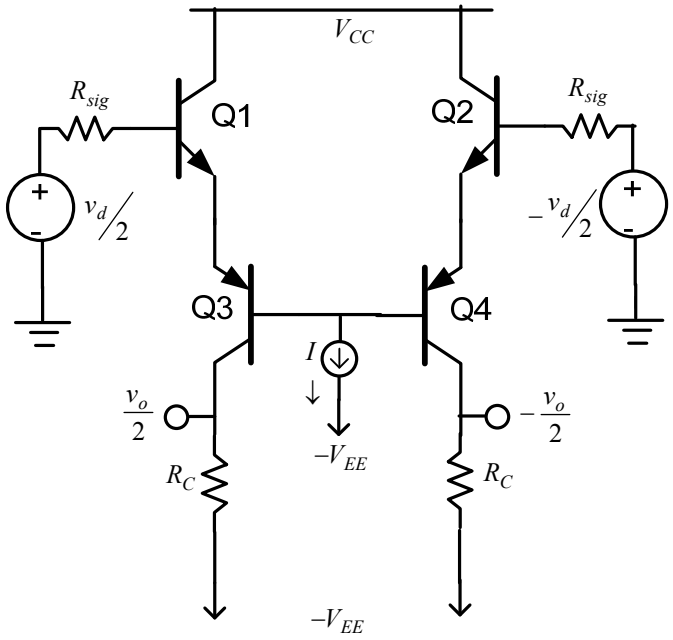



Figure 3.27: Schematic of complementary CC-CB cascade doublet differential amplifier

Q1,Q3 we can construct the high frequency equivalent circuit as shown in figure 3.28. We have ignored[2] $r_x$ and $r_o$ to further simplify the analysis.

We can now rearrange the direction of one of the controlled current sources by reversing the direction of the controlling voltage $v_\pi$. This leads to figure 3.29(a). Figure 3.29(b) reveals further simplification by combining the two identical parallel $C_\pi$ , $r_\pi$ circuits which occur in series connection. The current $g_m v_\pi$ coming *toward* and *leaving* from the node marked E1,E2 can be lifted off from this junction and has been shown as a single current $g_m v_\pi$ meeting the node C2.

[2] A *rule –of- thumb* regarding such simplifications is: a resistance in *series* connection can be neglected as *short circuit* if it is *small* compared with other resistances. Similarly, a resistance in *shunt* connection can be neglected *as an open circuit* if it is *high* compared with other resistances.

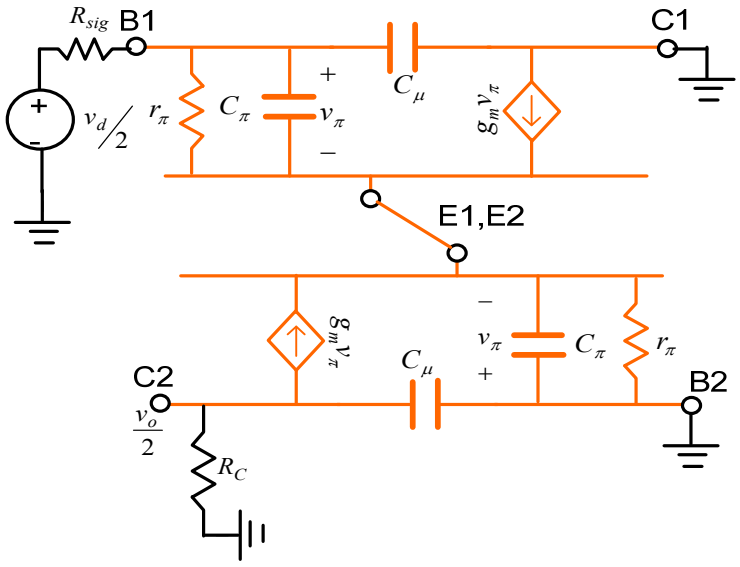



Figure 3.28: Approximate high frequency equivalent circuit for the schematic in Fig.3.27.

In Fig.3.29(b) we can see two disjoint circuits (shown by blue and *olive* green lines) with associated distinct time constants. The time constants are:

$\tau_1 = (\frac{C_\pi}{2} + C_\mu) \times (2r_\pi \,\|\, R_{sig})$, and $\tau_2 = C_\mu R_C$. The dominant high frequency pole is: $\omega_H = \frac{1}{\tau_1 + \tau_2}$, which can be regarded as the band width of the amplifier.

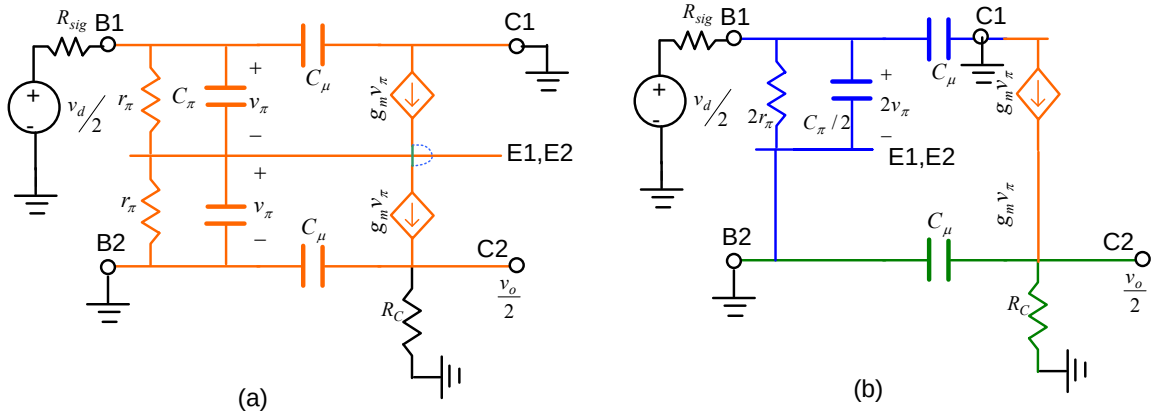



Figure 3.29: Further simplification and compaction of the circuit in Fig.3.28.

The *student is suggested to construct* the low-frequency form of the equivalent circuit in Fig.3.29(b) and find the expression for the mid-band gain $A_M$. The gain bandwidth is then $A_M\, \omega_H$.

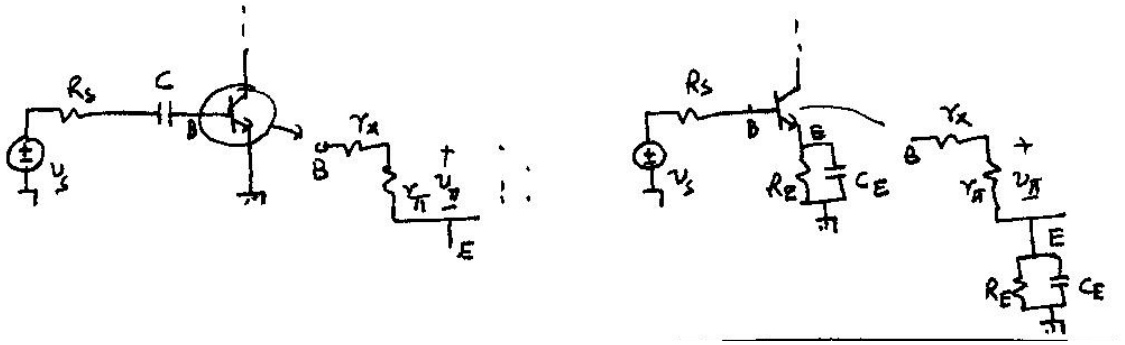
3.6.4:Wide band amplifiers with MOSFET transistors

Enhancement mode MOSFET can be connected in the same way as BJT stages to derive cascode and wide band differential amplifiers for high frequency applications. The analysis follows similarly.

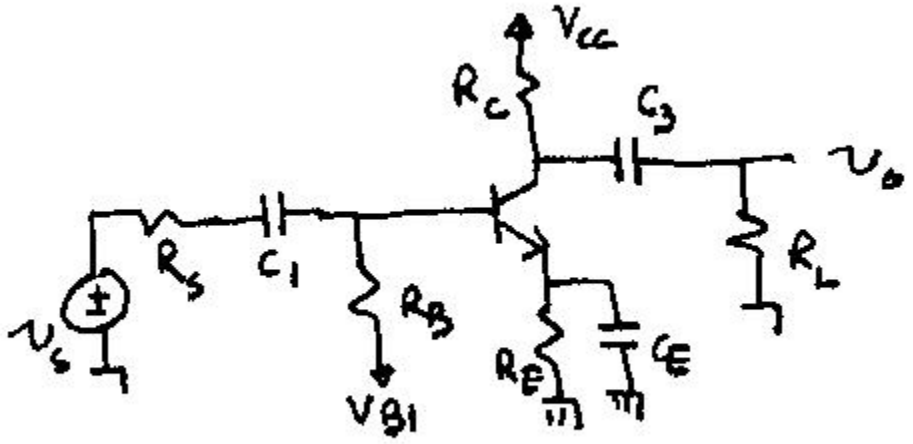
*The student is encouraged to draw the schematics with MOSFET devices by following the corresponding BJT configurations in sections 3.6.3.1-3.*

3.7: Practice Exercises

3.7.1: Show by appropriate analysis (KCL/KVL/Nodal matrix) that the voltage signal coupled across the internal base-emitter junction of a BJT (i.e., $v_\pi$) has a (a) zero at $\omega=0$, when a voltage source signal is fed to the base of the BJT via a series capacitor, and (b) has a zero at a finite frequency when parallel R,C network is in series with the voltage source. Use the low-frequency equivalent circuit for the transistor. Consider the representative cases as shown below.




3.7.2: For the BJT CE amplifier below, given $R_S$=600 ohms, $R_B$= 22 k ohms, $h_{fe}$=99, $I_C$=2 mA, $R_E$= 1.5 k ohms, $R_C$=2.2 k ohms, $R_L$=1 k ohms, $C_1$ =1 μF, $C_2$=25 μF, $C_3$= 10 μF. What will be the lower -3dB frequency for the amplifier?




3.7.3: In a BJT, CE amplifier the network parameters are: $R_S$= 100 ohms, $R_B$=1 k ohms, $r_x$= 50 ohms, $I_C$= 1 mA, $h_{fe}$= 99, $C_\pi$=1.2 pF, $C_\mu$=0.1 pF, $V_A$=50 V, $R_C$=1.5 k ohms. Find,

(a) The time constants associated with the capacitors using open-circuit time constant method.

(b) What is the approximate upper cut-off frequency?

(c) In the equivalent circuit of the amplifier use Miller's theorem assuming a gain of $-g_mR_C$ between the internal collector and base terminals of the BJT, and re-draw the equivalent circuit.

(d) Determine the pole frequencies in the equivalent circuit derived in step (c) above.

(e) What will be the approximate upper cut-off frequency using the results in (d)?

(f) Use the full transfer function determination method to the equivalent circuit of the CE amplifier and determine the pole frequencies using exact solution of *D(s)=0*, where the voltage gain function is : *N(s)/D(s)*.

(g) Determine the 'dominant' pole from the *D(s)* derived in step (f) above.

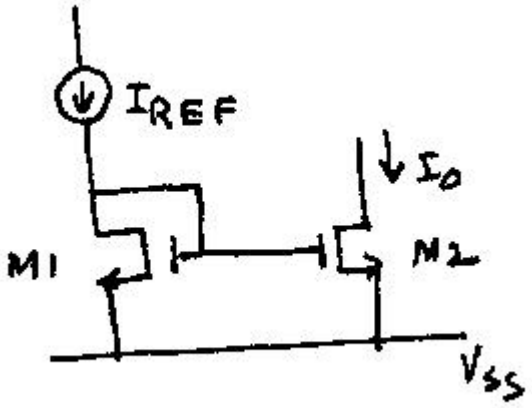
(h) What are your estimates about the upper cut-off frequencies if you use the results in (f) and (g)?

(i) Tabulate the upper cut-off frequency values obtained in steps (b), (e), (f), and (g).

3.7.4: In a MOSFET amplifier, you are given the following: $R_S$=100 ohms, $C_{gs}$=0.1 pF, $C_{gd}$=20 fF, $g_m$ =50 μ mho, $I_{DC}$=50 μA, $V_A$=20 V, and $R_L$= 5 k ohms. The MOSFET amplifier is configured to operate as CS amplifier. Find the dominant high-frequency pole of the amplifier using:

(a) Miller's theorem
(b) Full nodal analysis
(c) Open-circuit time constant method

3.7.5: Consider a basic MOSFET current mirror circuit. Find an expression for the high frequency current transfer function $i_o(s)/i_{in}(s)$. Use the high frequency ac equivalent circuit model for the transistors.




3.7.6: For the BJT amplifier shown below, determine the high frequency voltage gain transfer function in the form: $A(s) = A_M \dfrac{\omega_H}{s+\omega_H}$. Given $C_\mu$ =0.5 pF, $f_T$=600 MHz, $h_{fe}$=49.

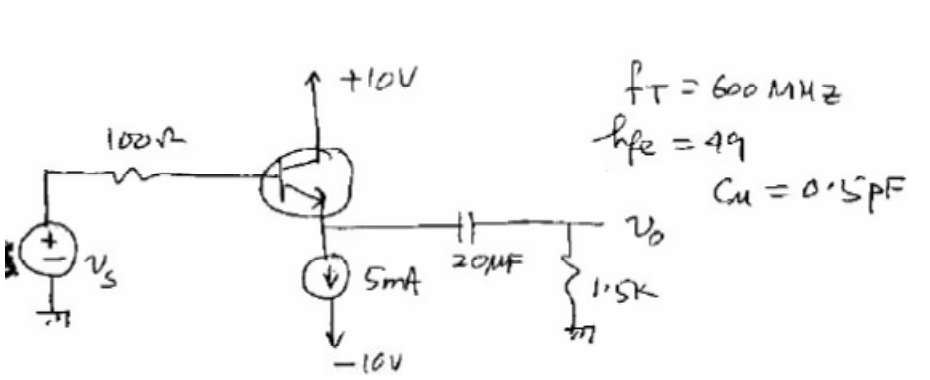



Fig. for Problem ~~3.8.6~~ 3.7.6

3.7.7: For the CD-CS cascade MOSFET composite amplifier, it is given that, $V_A$=20 V, $C_{gs}$=0.5 pF, $C_{gd}$= 0.1 pF, $I_{DC}$= 50($V_{GS}$- $V_{TH}$)$^2$ μA, $V_{TH}$ =1 V. Estimate $f_H$ for this amplifier system. The output resistance of each current source is 1 Mega ohms.

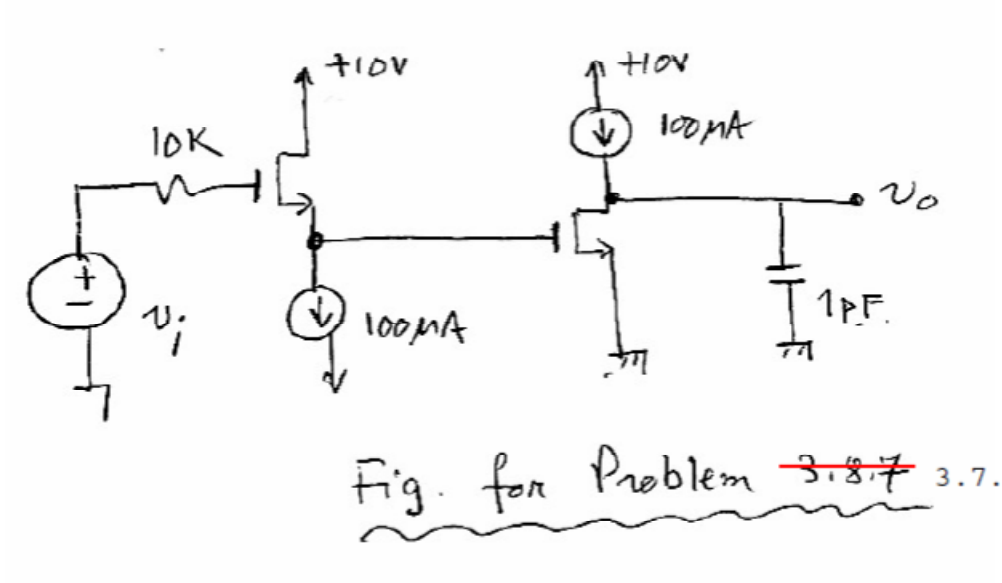
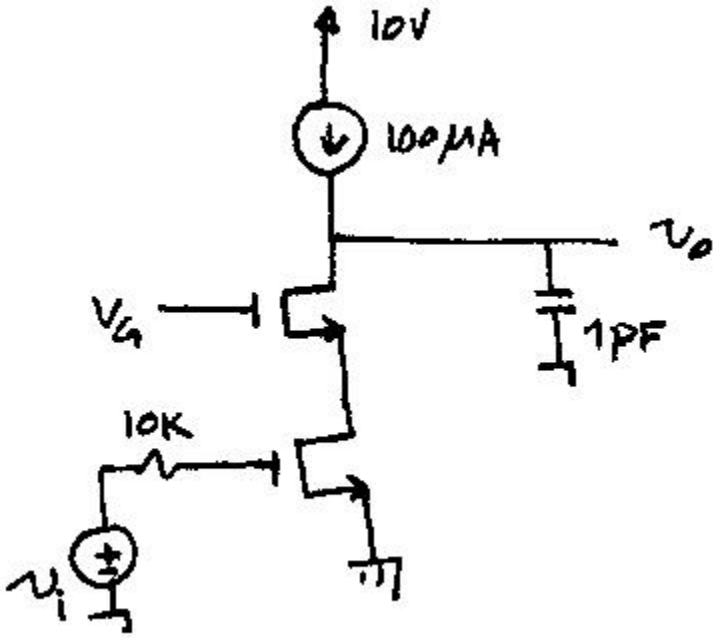



Fig. for Problem ~~3.8.7~~ 3.7.7

3.7.8: Find $f_H$ for the CS-CG cascade MOSFET amplifier system shown below. Use necessary data from problem # 3.7.7 above.


10V
100μA
$v_o$
$V_G$
1PF
10K
$v_i$

# Chapter 4

# FEEDBACK in AMPLIFIERS

(*Review Appendix 3.5 for background on two-port networks*)

Feedback implies feeding back (i.e., returning back) a part of the processed signal to the input side so as to enhance or diminish the input signal. When the input signal (current or voltage) is diminished, it is considered as negative feedback. When the input signal is enhanced, it is known as positive feedback. Negative feedback is employed in amplifying systems to achieve certain special characteristics that are not obtainable from the basic amplifier. Positive feedback is employed to produce signal generator, such as oscillators. In this chapter we shall consider the case of negative feedback. The following topics will be covered:

- Basic concepts and benefits of negative feedback.
- Interconnections and associated circuit models of the amplifier and the feedback network.
- Analysis techniques with examples for the four basic amplifier configurations (VCVS,CCCS,VCCS,CCVS).
- Negative feedback and stability- phase and gain margins.

## 4. 1: Basic negative feedback system

Consider the Figure below. The source signal could be a current or voltage. The basic amplifier has a gain $A$ from left to right direction. A part of the output signal $x_o$ is fed back by the factor $\beta$, from right to left, and subtracted (added with a phase inversion) from the input signal $x_s$.

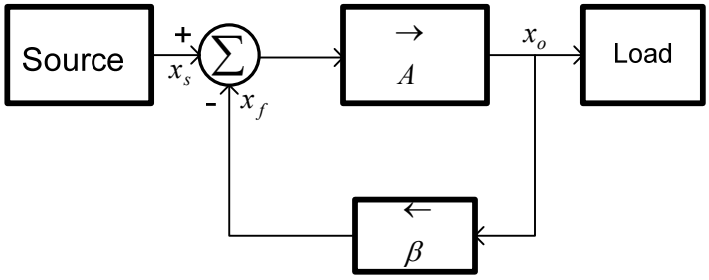



Figure 4.1: Basic negative feedback system

While the basic amplifier has a gain $A$ (i.e., $x_o / x_I$ ), the overall gain of the feedback system $x_o / x_s$ is $A_f$ which is $A/(1 + A\beta)$. This gain is called the gain with feedback. The quantities $A$ and $A_f$ could be any one of the four different kinds of function, i.e., (a) voltage gain, (b) current gain, (c) trans-resistance gain and (d) trans-conductance gain. Some special features of the negative feedback system can be appreciated very easily.

The quantity $A\beta$ is called the *loop gain* of the system. The term $1 + A\beta$ is referred to as the *feedback factor*.

*Exercise 4.1.1:* An audio amplifier has a gain of 100 V/V. It is placed under negative feedback with a feedback gain (=$\beta$) of 0.1. What will be the net gain now? (*ans*: 100/11)

4.1.1: Benefits of negative feedback

4.1.1.1: *Gain de-sensitivity*

This implies that if there occurs a variation by certain amount in the gain A of the main amplifier, the gain $A_f$ of the feedback system is not altered as much i.e., the gain variation is desensitized by negative feedback.

Assume $\beta$ is constant. Then if we take differential of $A_f$, we get $dA_f = \dfrac{dA}{(1+A\beta)^2}$

Thus it is evident that the variation $dA$ in $A$ has been reduced by the factor $(1+A\beta)^2$ because of negative feedback

*Exercise 4.1.1.1.1:* Consider the amplifier in *exercise 4.1.1*. Changes in the DC power supply may cause 20% variations in the gain of the amplifier. What will be the variation if it is connected in negative feedback with $\beta$=0.05?

4.1.1.2: *Bandwidth extension*

This implies that if the band width of the gain $A$ has certain values (say 1MHz), by applying negative feedback, it can be increased. The increase, however, happens by sacrificing the value of the gain $A$.

Thus, consider $A = \dfrac{A_M}{1 + s/\omega_H}$ This has a high frequency band with of $\omega_H$ rad/sec. If we apply negative feedback around the amplifier, the gain $A_f$ will become:

$$A_f(s) = \frac{A(s)}{1+\beta A(s)} = \frac{A_M \Big/ (1+\frac{s}{\omega_H})}{1+\beta \, A_M \Big/ (1+\frac{s}{\omega_H})}$$

After simplification : $A_f(s) = \frac{A_M/(1+A_M\beta)}{1+s/[\omega_H(1+A_M\beta)]} = \frac{A_{Mf}}{1+\frac{s}{\omega_H(1+A_M\beta)}} = \frac{A_{Mf}}{1+\frac{s}{\omega_{Hf}}}$

where, $A_{Mf} = \frac{A_M}{1+A_M\beta}$, and $\omega_{Hf} = \omega_H(1+A\beta)$

The above result implies a mid-band gain of $A_{Mf}$ and a high frequency band width of $\omega_{Hf}$. It can be clearly seen that the new mid-band gain is $(1+A\beta)$ times smaller than the mid-band gain without feedback, but the high frequency band width is $(1+A\beta)$ times larger than the band width without feedback. Thus an extension of band width by the factor $(1+A\beta)$ has been achieved.

*Exercise 4.1.1.2.1:* Consider the amplifier in *exercise 4.1.1*. It has a bandwidth of 5 kHz. It is required to increase the bandwidth to 25 kHz. What value of $\beta$ should be used? What will be the new gain of the amplifier under feedback?

4.1.1.3: *Reduction of non-linear distortion in amplifiers*

It is known that most practical amplifiers have a non-linear output input transfer characteristics. The non- linearity arises out of (i) non-linear response characteristic of the devices (i.e., transistors), and/or (ii) finite DC power supply values.

A non-linear transfer curve represents a gain (~ slope of the graph) which varies depending upon the location of operation on the curve (i.e., the operating point). Thus one can define a series of gains, say, $A_1$, $A_2$, .. along the transfer characteristics. Under negative feedback the corresponding gains become $A_1/(1 + A_1\beta)$, $A_2/(1 + A_2\beta)$, and so on. If the loop gain values (i.e., $A_1\beta$, $A_2\beta$) are very high (i.e., >>1), the feedback gain values approximate to $1/\beta$ in each case. Thus, the gains under negative feedback at different segments of the transfer characteristic appear to remain constant at a value $1/\beta$. A constant gain (~constant slope) implies a linear curve, i.e., a straight line. This is how the non-linearity in the response characteristic of the amplifier is reduced, and hence the attendant distortion gets reduced.

4. 2: Interconnections for the negative feedback systems

We will now consider the four distinct types of negative feedback connections and their respective characteristics as regards the overall gain, input and output impedances. The classification basically depends upon the four distinct types of amplifiers, namely, (a) voltage amplifier (VCVS), (b) current amplifier (CCCS), (c) trans-resistance amplifier (CCVS), and (d) trans-conductance amplifier (VCCS).

For each case, the topology (i.e., the style of interconnection) of the negative feedback network follows a regular pattern relative to the topology of the basic amplifier. Thus, for a voltage amplifier (VCVS), whose equivalent circuit model has (i) a series connection at the input through the input resistance, and (ii) a series connection at the output (i.e., the output controlled voltage source and its associated resistance connected in series), the feedback circuit will have (i) a series connection at the input, and (ii) a shunt (parallel) connection at the output. A *rule of thumb* is: the feedback *connection at input matches* with that of the basic amplifier, but the *connection at the output is opposite* to that of the basic amplifier.

4.2.1: System diagrams for the feedback connections

Consider figures 2(a)-(d) which depict the *four* possible interconnection styles (*topology*) around the *four* basic electronic amplifier systems.

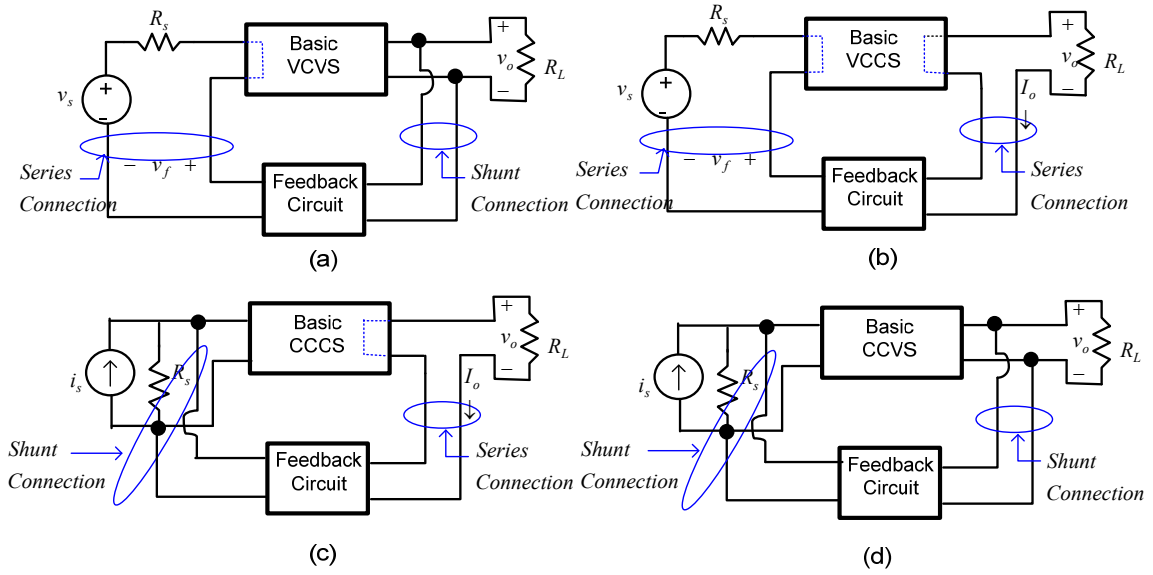



Figure 4.2: *Four* possible feedback connections

*Quiz:* Given a VCCS amplifier, what will be the topology of the feedback connections at the input and at the output? Apply the *rule of thumb*, then check your answer with Fig.4.2(b). (You need to recollect the topology of the VCCS amplifier though!)

4.2.2: Model of the input source according to the feedback connection style

The operation at the input of a feedback amplifier system involves *mixing* of signals. *Mixing* is possible only for signals of the *same type* i.e., voltage with voltage, current with current, and so on. Similarly, the operation at the output of the amplifier under feedback is called *sampling*. *Sampling* can be done for only *one kind* of signal i.e., a voltage or a current.

Consider Fig.4.2(a). The *mixing* is done with *series* connection at the input of a VCVS. The question is what kind of signal can be *mixed* in *series connection*? Recalling the practice of writing a KVL around a loop (i.e., a succession of *series connected* elements) prompts us to appreciate that such *mixing* in *series connection* is possible *only* with *voltage* signals. Since *voltage* signals are *mixed* in series, we obviously understand that the signal source in this case *must* be a *voltage* source. The *signal* source voltage is *mixed* with the *feedback* voltage in *series* at the input of a VCVS which has a *series* topology at its input.

Same conclusion follows for Fig.4.2(b), where the signal source is to be modeled as a voltage source. The VCCS has a *series* topology at its input. Hence the feedback connection at the input is a *series* connection. Only a *voltage signal* can be mixed in *series* with another *voltage signal* (in this case the feedback signal). Hence the source must be a voltage source.

*Hint to remember: Series in* implies a voltage signal as the source and a VCxx (*voltage controlled xx*) form of the basic amplifier. VCxx could be VCVS or VCCS.

In the same way, we can understand that for CCCS and CCVS (i.e., CCxx) [Figs. 4.2(c) - (d)], the input topology being a *shunt* (i.e., parallel connection) configuration, *only* current signals can be mixed under this kind of connections. *Shunt* implies a *node* – hence *KCL*- hence *current* signal being *mixed*. Hence the input sources for CCCS and CCVS amplifiers are to be modeled as current sources.

*Hint to remember: Shunt in* implies a current signal as the source and a CCxx (*current controlled xx*) form of the basic amplifier. CCxx could be CCVS or CCCS.

4.2.3: Model of the basic amplifier according to the feedback connection style

The purpose of this short section paragraph is to emphasize an understanding of the models of the basic amplifiers depicted in Figs. 4.2(a)-(d). From the section 4.2.2, the student can understand that for a *series in* feedback connection the basic amplifier will be of VCxx form. Similarly, for a *shunt in* feedback connection the basic amplifier will be CCxx form. How to figure out the xx part? For this we need to examine the style of the feedback connection at the *output*.

It has been mentioned in section 4.2 that the feedback connection at the *output* is *opposite* to that of the basic amplifier. Thus, a *shunt* connection at the output will imply a *series* connection style at the output of the amplifier. A *series* connection implies a **voltage source** with a series resistance. Now to put both the input and output feedback connections together, a *series in-shunt out* connections will imply a VC (for series in) VS (for shunt out), i.e., a VCVS amplifier model.

Similarly, a *series* connection at the output will imply a *shunt* connection style at the output of the amplifier. A *shunt* connection implies a **current source** with a shunt resistance. Now putting the input and output feedback connections together, a *series in-series out* connections will imply a VC (for series in) CS (for shunt out), i.e., a VCCS amplifier model.

The student may confirm his/her understanding of the models of the basic amplifiers in Figs. 4.2 (c)-(d) in light of the discussions above.

4.2.4: Input, output resistances under negative feedback

If we realize that resistances connected in *series* produces an *increase* in the resistance while resistances connected in *parallel* (shunt connection) produces a *decrease* of resistance, one can immediately infer that at the *series connection location* of the feedback system there will be an increase in the resistance value. Similarly, at the point where the feedback connection is in shunt, the resistance will decrease after feedback connection.

4.2.5: Modeling the feedback circuit by two-port network parameters

The expression for the gain with negative feedback in section 4.1 was derived under the assumption of a smooth interconnection between the amplifier and the feedback network. In practice such smooth interconnection does not happen, a loading is always present. Further, it was implicitly assumed that the signal transmission through the amplifier and

the feedback network are unidirectional, being from the *source toward the output* (load) *through the amplifier* (i.e., left to right in our diagrams) and from the *output toward to source* (i.e., right to left in our diagrams) *through the feedback network*. This is an ideal situation. So certain approximations are required and practical design must ensure that these assumptions are reasonably accurate.

The effect of loading of the amplifier can be efficiently taken care of by modeling the feedback circuit as a two port network (*review Appendix 3.5 for necessary background*). The two-port circuit models pertinent to the *four* feedback interconnection styles are presented in **Table 4.1**.

linear circuit elements (i.e., *passive, bilateral* impedance/admittance) and *two* controlled sources. The controlled source on the *right half* (i.e., toward port #2) of the model is *controlled by* a voltage/current present on the *left half* (i.e., toward port #1), and *vice versa*.

For the amplifier since the signal flow is from *left* (i.e., signal source) to *right* (i.e., amplifier output), the controlled source on the *right* half of the two port model is *most* effective and important. For the feedback circuit since the signal flow is from *right* (i.e., amplifier output) to *left* (i.e., signal source), the controlled source on the *left* half of the two port model is *most* effective and important.

We will use the two port model *only* for the feedback circuit. The *passive* linear components of the model will be connected at the input and the output of the basic amplifier in conformity with the feedback connection respectively at the input and at the output. This will produce the *loaded* amplifier. The controlled source on the *left half* of the two port model will be representing the feedback gain $\beta$ as introduced in section 4.1. The approximated two port models are also shown in **Table 4.1** (in column *three*).

It must be *emphasized* at this point that *the amplifier gain A* and *the feedback factor* $\beta$ as introduced in section 4.1 in practice correspond to (i) the gain of the *loaded* amplifier, and (ii) the gain represented by the controlled source of the pertinent model in column *three* of Table 4.1. Guidelines to construct the *loaded* amplifier are provided in **Table 4.2**

4.2.6: *Summary of the results for calculating gain and impedances under negative feedback*

An important characteristic of the various feedback systems is that if the *loaded* gain $A$ and the *feedback* gain $\beta$ can be determined, the expressions for various gain and resistance values can be easily calculated. These follow certain easy to remember

standard forms. **Table 4.3** provide various important formulae. The student should pay particular attention to the columns for $Z_{if}$ and $Z_{of}$.

**Table 4.1** (Two port equivalent models for the feedback circuits)

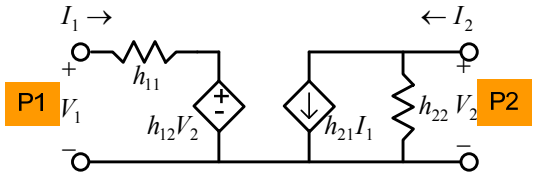
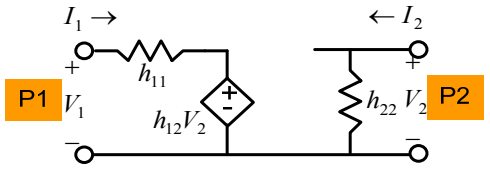
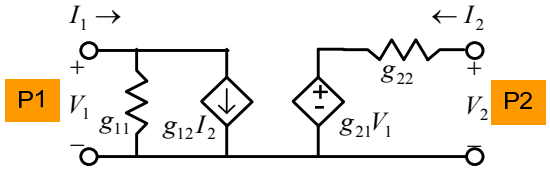
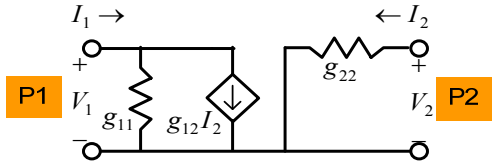
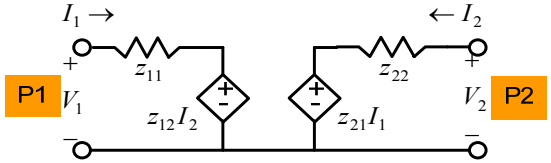
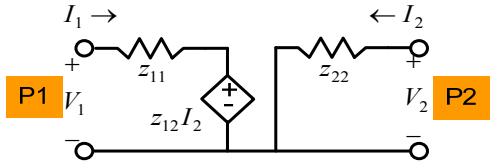
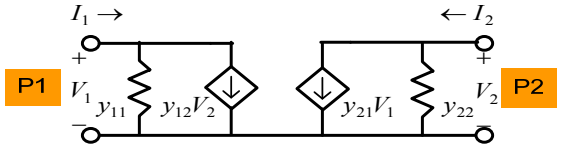
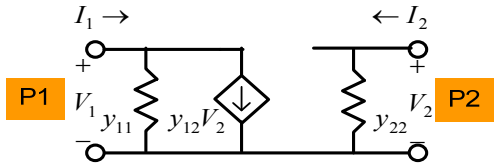
| Model name | General formulations (equations & circuit models) | Approximate circuit model | Feedback |
|---|---|---|---|
| [h] | $h_{11}I_1 + h_{12}V_2 = V_1$ ; $h_{21}I_1 + h_{22}V_2 = I_2$   |   | Series-Shunt |
| [g] | $g_{11}V_1 + g_{12}I_2 = I_1$ ; $g_{21}V_1 + g_{22}I_2 = V_2$   |   | Shunt-Series |
| [z] | $z_{11}I_1 + z_{12}I_2 = V_1$ ; $z_{21}I_1 + z_{22}I_2 = V_2$   |   | Series-Series |
| [y] | $y_{11}V_1 + y_{12}V_2 = I_1$ ; $y_{21}V_1 + y_{22}V_2 = I_2$   |   | Shunt-Shunt |

**Table 4.2** (Guidelines to create the *loaded* amplifier)

| Amplifier Model | Pertinent 2-port parameters | Feedback connection | Modifications to basic amplifier to create the *loaded* amplifier |
|---|---|---|---|
| VCVS | [h] | Series in Shunt out | $R_{11} = h_{11}$ in series with input<br>$R_{22}=(h_{22})^{-1}$ in parallel with output |
| CCCS | [g] | Shunt in Series out | $R_{11} =(g_{11})^{-1}$ in parallel with input<br>$R_{22} =g_{22}$ in series with output |
| VCCS | [z] | Series in Series out | $R_{11} = z_{11}$ in series with input<br>$R_{22} = z_{22}$ in series with output |
| CCVS | [y] | Shunt in Shunt out | $R_{11}=(y_{11})^{-1}$ in parallel with input<br>$R_{22}=(y_{22})^{-1}$ in parallel with output |

**Table 4.3:** ( Summary of the formulae, $A_f = X_o / X_S = \dfrac{A}{1+A\beta}$ for all cases)

| Feedback connection | $A$ | $\beta$ | Basic Amplifier | $Z_{if}$ | $Z_{of}$ |
|---|---|---|---|---|---|
| Series-shunt | $V_o/V_I$ | $V_f/V_o$ | VCVS | $Z_I(1+A\beta)$ | $Z_o/(1+A\beta)$ |
| Shunt-series | $I_o/I_I$ | $I_f/I_o$ | CCCS | $Z_I/(1+A\beta)$ | $Z_o(1+A\beta)$ |
| Series-series | $I_o/V_I$ | $V_f/I_o$ | VCCS | $Z_I(1+A\beta)$ | $Z_o(1+A\beta)$ |
| Shunt-shunt | $V_o/I_I$ | $I_f/V_o$ | CCVS | $Z_I/(1+A\beta)$ | $Z_o/(1+A\beta)$ |

It may be seen from the above table that whenever the feedback network has series interconnection, the corresponding (i.e., input or output) impedance is *increased* by the factor $(1+A\beta)$, while a shunt connection *reduces* the impedance at the pertinent location (i.e., input or output) by the factor $(1+A\beta)$. These observations can be of aid to remember the formulae.

4. 3: Analysis examples

4.3.1 Series-in shunt-out feedback (basic amplifier is VCVS)

- *OP-AMP based system example*

An OP-AMP having an open loop gain of 10000, an input differential resistance of 100k and an output resistance of 1k is connected as shown in figure 4.3. The resistances $R_1$ , $R_2$ form the feedback network. Find the resulting voltage gain, input resistance and output resistance.

**Solution**: Since the basic amplifier is a VCVS, the feedback is series-shunt type. In forming the "loaded" amplifier, we have to use *h-parameter* representation of the feedback network. After deriving the loaded amplifier, we shall calculate the gain $A$, $R_{in}$ and $R_{out}$ for the loaded amplifier. We have to calculate the feedback factor β as well. Then we shall apply the formulae in Table 1 to calculate the gain and resistances of the new system (i.e., the OP-AMP with feedback).

Given: $R_S = 10k\Omega, R_{id} = 100\,k\Omega, A_{VO} = 1000, R_O = 1k\Omega, R_1 = 1k\Omega, R_2 = 1M\Omega, R_L = 2k\Omega$

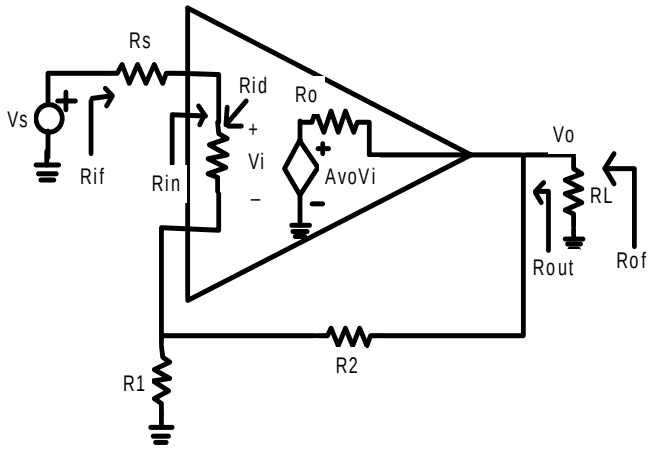



Figure 4.3: A series-in, shunt-out negative feedback system using an OP-AMP

The amplifier ac equivalent circuit using hybrid parameter description for the feedback circuit is shown in Fig.4.4.

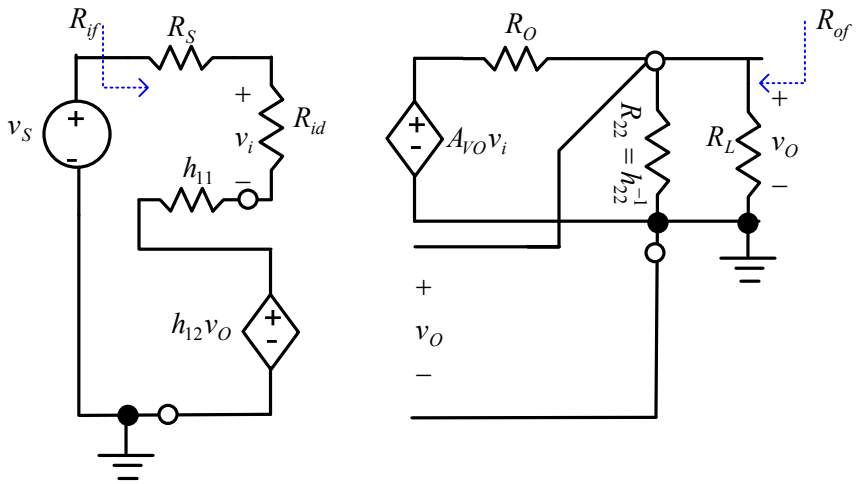
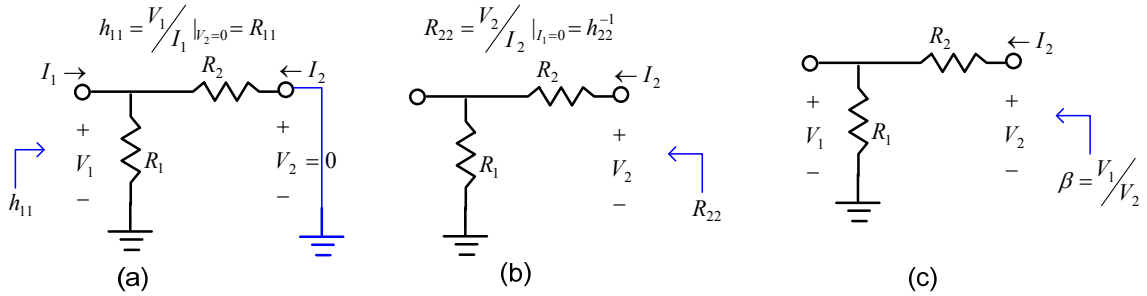



Figure 4.4: *ac* equivalent model of Fig.4.3 including the two-port model of the feedback network ($R_1$, $R_2$)

For the feedback network, the relevant *h*-parameters are evaluated using the partial *ac*




4.5 Partial equivalent circuit models to determine the *h* –parameter components.

equivalent circuit models depicted in figure 4.5(a)-(c).

We need now to attach the feedback circuit model to the amplifier circuit model. Figure 4.6(a) shows the amplifier model in black lines and the feedback part in blue lines. This is an intermediate step to form the *loaded* amplifier circuit (*A*-circuit). Figure 4.6(b) shows the *loaded* amplifier in pink lines. The feedback contribution as the controlled source is shown in orange lines. This is called as the $\beta$-circuit. At this stage we can apply the standard formulae in **Table 4.3** for the gain ($A_f$), input and output resistances ($R_{if}$, $R_{of}$) under feedback.

Note that for the loaded amplifier $R_{inx} = R_s + R_{id} + h_{11}$ = 10+100+1= 111k. Then since $\beta$ = 10E-3, $R_{if}$ (by formula)=$R_{inx}$ (i.e.= 111kΩ)*(1+$A\beta$). Now the gain $A$ of the loaded amplifier needs to be found out.

Thus, $A = \dfrac{100\ k\Omega}{(100+10+1)\ k\Omega} \times 10^4 \times \dfrac{1002\ k\Omega \,||\, 2\ k\Omega}{1002\ k\Omega \,||\, 2\ k\Omega + 1\ k\Omega} = 6006$ V/V

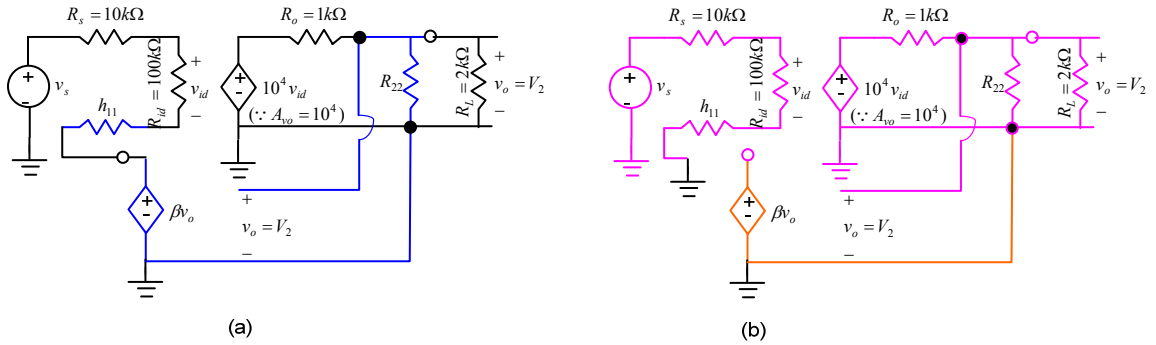



Figure 4.6: Construction of the *loaded* amplifier (a) complete equivalent circuit, (b) positioning of the loading elements inside the basic amplifier (pink lines).

Considering the equivalent circuit of the loaded amplifier, we can determine:

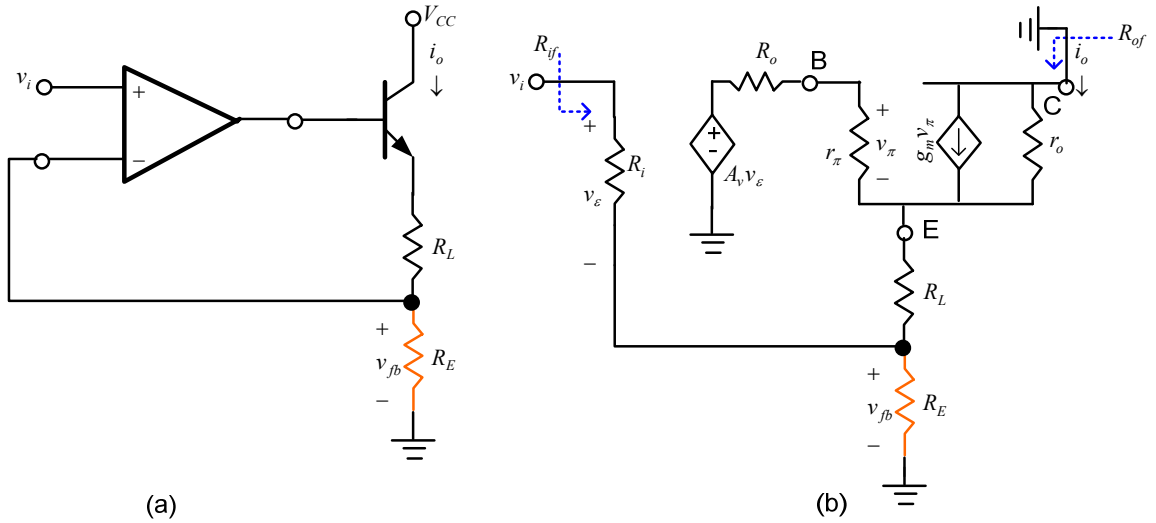
$1+A\beta$ = 1+6006*1E-3=7.006. Thus $A_f$ =$A$/7.006 = 858 V/V, $R_{if}$ =$R_{in}$ (1+Aβ) = 111*7.006=777k, and $R_{of}$ =($R_L$ | | $R_o$ | | $R_{22}$)/( $1+A\beta$) =667/7.006=95.3Ω.

Now, $R_{in}$ = $R_{if}$–$R_s$ =777k –10k =767k. But $R_{out}$ | | $R_L$ =$R_{of}$ giving $R_{out}$ =100Ω.

4.3.2 Series-in series-out feedback (basic amplifier is VCCS)

- *OP-AMP based system example*

Figure 4.7(a) presents an OP-AMP followed by a BJT common collector amplifier



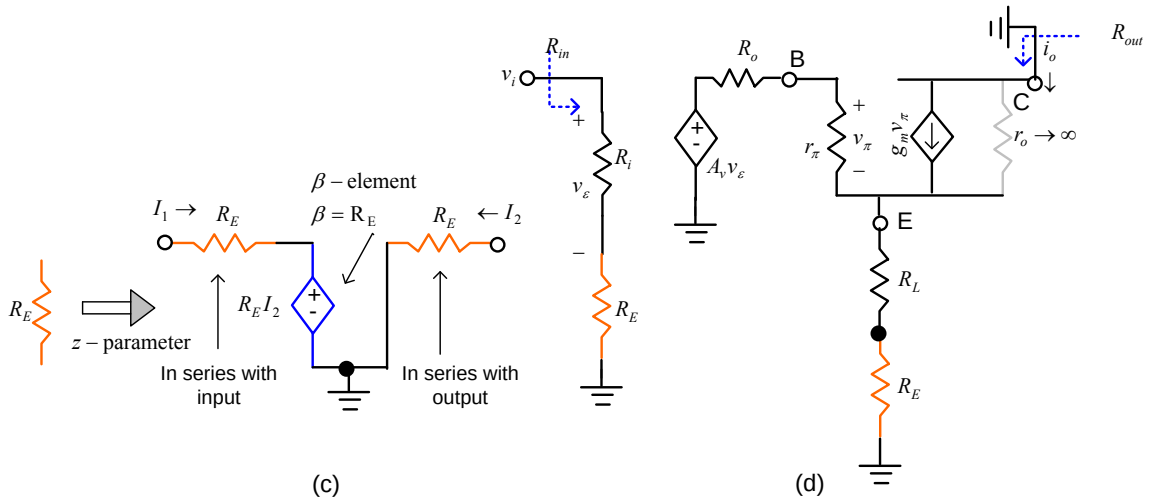



Figure 4.7:

connected in a series (in)-series (out) feedback system. The resistance $R_E$ provides the negative feedback. Given $R_i = 50k\Omega, A_v = 1000, R_o = 100\Omega, I_C = 2mA, h_{FE} = 100$. Further, $R_E = 100\Omega, R_L = 1k\Omega$. Figure 4.7(b) is the ac equivalent circuit of the connected system. We want to calculate the gain $i_o/v_i$, $R_{if}$, and $R_{of}$ as shown in Fig.4.7(b).

Because the feedback is *series-in, series-out*, the feedback resistance $R_E$ need be modeled using *z-parameter* equivalent circuit. Figure 4.7(c) shows the pertinent *z*-parameters, i.e., $z_{11}$ (=$R_E$), $z_{22}$ (=$R_E$), and $z_{12}$ (=$\beta$=$R_E$). Figure 4.7(d) presents the *loaded* amplifier.

***Analysis with the loaded amplifier circuit*

Since the *Early* voltage of the BJT is not given, we can assume $r_o$ → *infinity*. Then,

$$i_o = g_m v_\pi = g_m A_v v_\varepsilon \frac{r_\pi}{R_o + r_\pi + (h_{FE}+1)\times(R_L + R_E)} = g_m A_v \frac{r_\pi}{R_o + r_\pi + (h_{FE}+1)\times(R_L + R_E)} \frac{R_i}{R_i + R_E} v_i$$

From the given data, $g_m$ =0.08 mho, $r_\pi = h_{FE}/g_m$=1250Ω., we can get the *loaded* gain $A$ as $\frac{i_o}{v_i} = 0.8875$ mho. Then $A\beta = AR_E = 88.75$.

The *transconductance* gain with feedback is then $A_f = A/(1+A\beta) = 0.8875/89.75 = 0.01$ mho or 10 *milli* mhos (watch! it is approximately $1/\beta$)

For the loaded amplifier $R_{in} = R_i + R_E$ =50.1 *k*Ω. Hence, with *series-in* feedback, $R_{if}$ =$(1+A\beta)R_{in}$ =4.496 MΩ.

For the location of $R_{out}$ shown in Fig.4.7(b), clearly $R_{out}$ is infinity, since we assumed $r_o$ as infinity. Hence $R_{of}$ is also *infinity*. However, if we intend to evaluate $R_{of}$ at the emitter

node of the BJT (Fig.4.7(b)), we need to first *sever* (i.e., break) the circuit at this location and then consider the net *series* (coming from *se*ver) resistance (note: series connection implies the existence of a *loop)* $R_E+R_L+ (r_\pi+R_o)/(1+\beta)$ (checked by inspection) at this point.

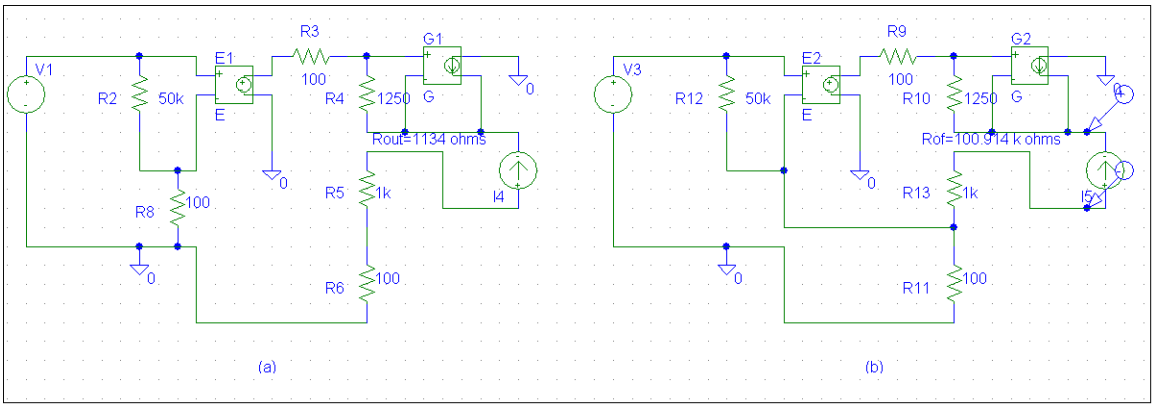



Figure 4.8:

Considering Fig.4.7(d) we find that $R_{out}$ is 1113.5 ohms. PSPICE simulation (Fig. 4.8(a)) gives a value of 1134 ohms. Then $R_{of}$ at this location will be $1113.5(1+A\beta)$= 99936.62 ohms Simulation by SPICE produces a value of 100.914 k ohms (see Figure 4.8(b)), which is very close to the value derived using the *loaded* amplifier equivalent circuit of Fig.4.7(d).

*Conclusion:* A question may arise about the utility of such a series-in, series-out system. The student may observe that neither an OA or a CC-BJT amplifier affords to *high* input and *high* output impedance as stand- alone devices. An OA has high input, but very low output impedance. So also is the case with a CC-BJT amplifier. Combining the OA and a CC-BJT amplifier in series-in, series-out negative feedback one can achieve the goal.

- *BJT based system example*

A simple example of a BJT based series-in, series-out feedback system is a CE-BJT amplifier with an emitter resistance $R_E$ as shown in figure 4.9(a). The *loaded* amplifier ac equivalent circuit is depicted in Fig.4.9(b). The feedback gain is $\beta=R_E$.

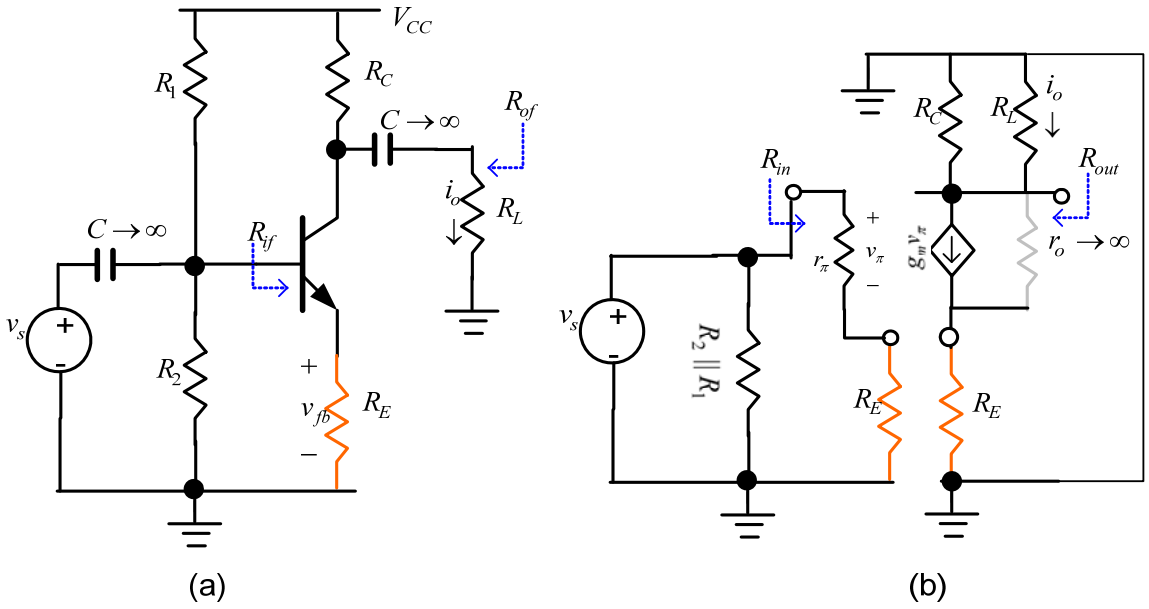



Figure 4.9:
The student is encouraged to work out the details to derive an expression for the voltage gain $v_o/v_s$ where $v_o$ is the signal voltage developed across the load resistance $R_L$. Note that the voltage gain will be $A_f$ times $R_L$ where $A_f$ is the transconductance gain under feedback.

4.3.3 Shunt-series feedback

- *OP-AMP based system example*

Figure 4.10 depicts a shunt-series negative feedback system using an OP-AMP.The resistances $R_1$ and $R_2$ form the feedback elements. We will analyze the system using the

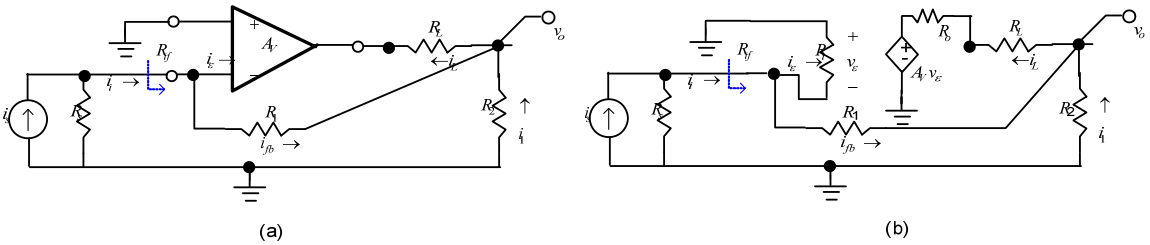



Figure 4.10: (a) The shunt-series feedback circuit schematic, (b) the associated ac equivalent circuit.

technique of *loaded* amplifier circuit.

A shunt series feedback needs the input source to be modeled as a current source. The two-port model of the feedback circuit elements will be the *g*- parameters. Figure 4.11(a)-(c) show the sub-circuits for the calculations of the *g*-parameter coefficients.

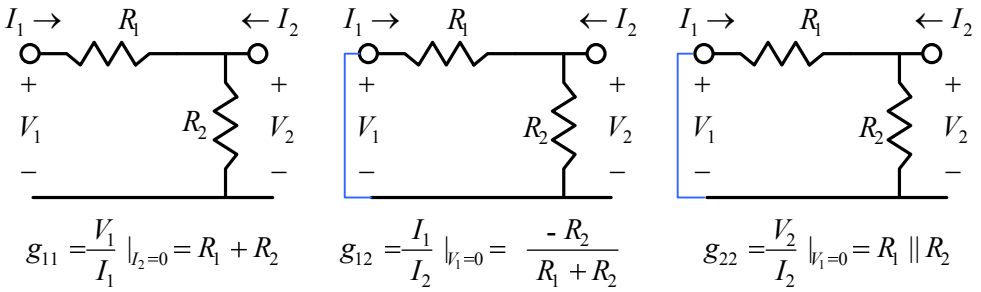



Figure 4.11: Illustration of calculation of the two-port model parameters

We now have to construct the *loaded* amplifier circuit by including $g_{11}$ in shunt at the input, $g_{22}$ in series with the output, and save $g_{12}$ as the feedback gain $\beta$. For shunt in-series out feedback, the basic amplifier is to be modeled as a CCCS, i.e., the *loaded* gain will be of the form $i_o/i_s$. The equivalent circuit for the loaded amplifier is shown in Fig. 4.12.

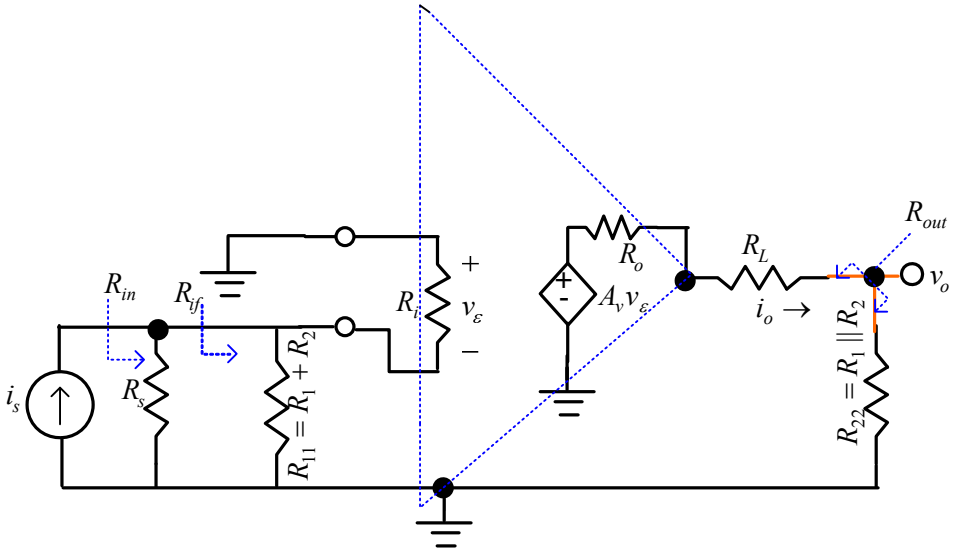



Figure 4.12: Loaded amplifier circuit after including the $g_{11}$ and $g_{22}$ parameters

***Analysis with the loaded amplifier*

From the equivalent circuit $A_i = \frac{i_o}{i_s} = -A_v \times \frac{R_s \| R_{11} \| R_i}{R_o + R_L + R_{22}}$; $R_{in} = R_s \| R_{11} \| R_i$, and $R_{out} = R_o + R_L + R_{22}$. The feedback factor is $1 + A_i\beta = 1 + A_v \frac{R_s \| R_{11} \| R_i}{R_o + R_L + R_{22}} \times \frac{R_2}{R_1 + R_2} = F$ (say).

Then, the current gain with feedback is $A_{if} = \frac{A_i}{F}$. The input resistance at the location of $R_{in}$ is $R_{\inf} = \frac{R_{in}}{F}$, and the output resistance at the location of the series (out) feedback will be $R_{outf} = R_{out}F$.

From Fig.4.12, we can see that $R_{if} \| R_s = R_{inf}$. With $R_s$, $R_{inf}$ known, $R_{if}$ can be found out.

4.3.4 Shunt-shunt feedback

- *OP-AMP based system example*

Figure 4.13 presents the case of an OP-AMP based shunt-shunt negative feedback circuit with $R_f$ as the feedback resistor. Shunt-shunt feedback will require the feedback resistor $R_f$ to be modeled as a two-port Y-parameter circuit. Further, the basic amplifier has to be modeled as a shunt-series device, i.e., a trans-resistance amplifier. Thus, the loaded amplifier gain need be calculated as $v_o/i_s$.

The ac equivalent circuit of the loaded amplifier is shown in Fig.4.14(a), while the $\beta$ circuit is shown in Fig.4.14(b).

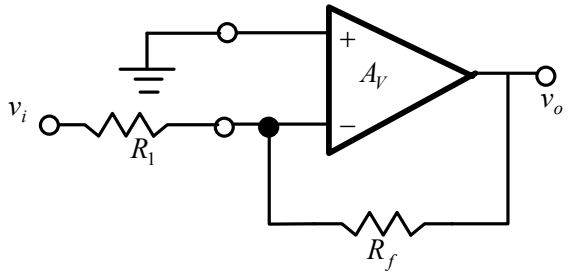



Figure 4.13: OP-AMP based inverting amplifier as a case for shunt-shunt feedback.

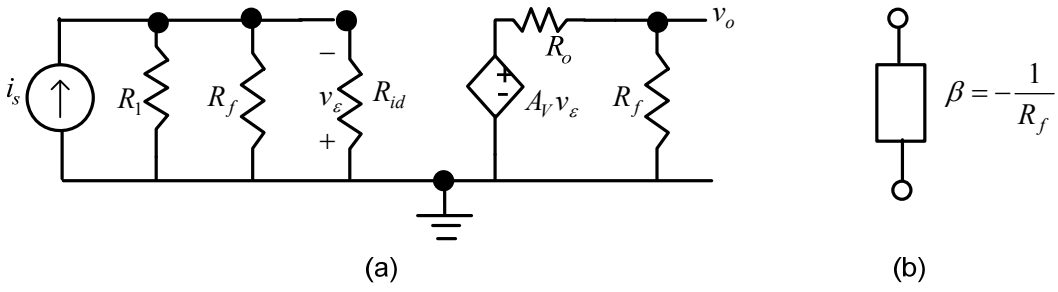



Figure 4.14: (a) ac equivalent circuit of the loaded amplifier, (b) the $\beta$ circuit.

** *Analysis with the loaded amplifier*

The loaded amplifier gain is $A = \frac{v_o}{i_s} = -A_v R_1 \,||\, R_{id} \,||\, R_f \times \frac{R_f}{R_o + R_f}$.

The feedback factor is $F = 1 + A\beta = \frac{R_o + R_f + A_v R_X}{R_o + R_f}$, $R_X = R_1 \,||\, R_{id} \,||\, R_f$

The feedback gain (as trans-resistance) is $A_f = \frac{A}{F} = -A_v R_X \frac{R_f}{R_o + R_f + A_v R_X} \approx -R_f$, when $A_v R_X >> R_o + R_f$ holds. Remember that $A_f$ is the trans-resistance gain $v_o/i_s$ under shunt-shunt (negative) feedback.

*Quiz*: Considering that $i_s = v_i/R_1$, what is the voltage gain $v_o/v_i$ in the present case?

## 4.4 Negative feedback and Stability

In the subject of the previous sections we assumed that the amplifier gain $A$ and the feedback gain $\beta$ are fixed numbers, independent of the frequency of the signal. This is far from truth. Since the amplifiers are built using BJT and/or MOS devices, the inherent parasitic capacitances in these devices render the amplifier gain $A$ a function of frequency, i.e., $A(s)$ with $s=j\omega$. Similarly, the feedback circuit may have the presence of reactive circuit elements (inductance, capacitance) either by design or as parasitic elements. Hence, in general, the feedback gain function $A_f = A/(1+A\beta)$ will be a function of frequency.

An interesting (but disturbing) result of such frequency dependence is that the system under negative feedback could become *unstable*, i.e., generate oscillations that are not expected. For a *stable* feedback system, it is necessary to investigate its stability characteristic before finalizing the design of the system. Specifically, we need to know if the designed system will be *potentially unstable* in the intended frequency range of application for signal processing. A procedure, originally introduced by H. Nyquist, is very convenient to determine the stability/potential instability scenario of a negative feedback system. In the following, we will assume that *only* the amplifier has a frequency dependent gain while the feedback gain $\beta$ is a fixed number (less than 1) independent of frequency.

### 4.4.1 Nyquist plot

The Nyquist plot is the graph of $A(j\omega)\beta$ as a function of frequency, plotted in polar co-ordinates. Consider the gain expression $A_f(j\omega) = \frac{A(j\omega)}{1 + A(j\omega)\beta} = \frac{x_o(j\omega)}{x_s(j\omega)}$ for a negative feedback system. If the denominator $1 + A(j\omega)\beta = 0$, we meet with the situation of

$A_f(j\omega) \to \infty$, or, equivalently, $x_o(j\omega)$ is *finite* while $x_s(j\omega) = 0$. When a *finite* output signal exists with *zero* input signal, the system is said to be *unstable*. The system will produce oscillations at a frequency $\omega_o$ which satisfies the equation $1 + A(j\omega_o)\beta = 0$.

Nyquist criterion says that a negative feedback system will be *potentially* unstable when the polar plot of $A(j\omega)\beta$ has a value of -1 (i.e, $1 + A(j\omega)\beta = 0$). Since we have assumed that $\beta$ is a constant, the criterion leads to the following two conditions.

$$|A(j\omega)\beta| = 1, \text{ and } \arctan[A(j\omega)] = -180^o$$

The negative sign before the phase angle is used to imply a causal system where the output signal *always* lags relative to the input signal. According to usual scientific convention a *negative* phase angle is drawn in a *clockwise* direction.

When the amplifier gain function is known, it is possible to find the frequency $\omega_o$ at which the angle $\varphi = \arctan[A(j\omega_o)] = -180^o$. If at the same frequency, the relation $|A(j\omega_o)\beta| = 1$ holds then the system will be unstable/*potentially* unstable at the frequency $\omega_o$.

An indication about the potential instability can be obtained easily by using the polar plot for the *loop-gain* function $A(j\omega)\beta$ and applying Nyquist criterion. Consider the plots shown in figure 4.15(a)-(c).

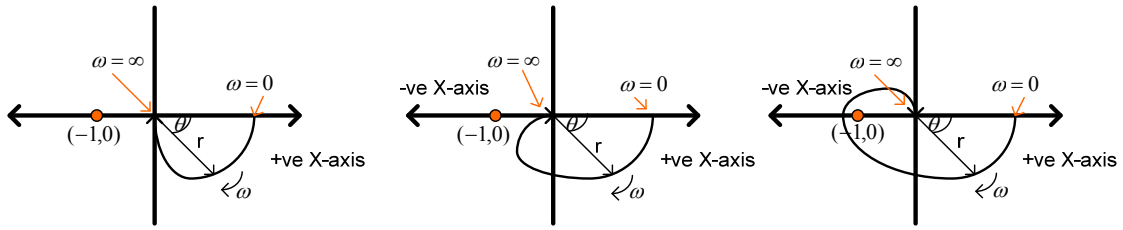



Figure 4.15: Polar plots of $A(j\omega)\beta$ with phase angles (at *infinite* frequency) of (a) $90^o$, (b) $180^o$, and (c) $270^o$.

In these plots the radius vector $r$ is $= |A(j\omega_o)\beta|$, while the angle $\arctan[A(j\omega)]$ (described *clockwise*) is labeled as $\theta$. The curves present successive frequency points $\omega$ from *zero* (i.e., dc) to *infinity* described *clockwise*.

In the graphs the point (-1,0) represents the radius $r$ of value 1, i.e., $|A(j\omega_o)\beta| = 1$, with the angle $\arctan[A(j\omega)] = -180^o$. On close examination we can understand that out of the three plots in Fig.4.15(a)-(c), only the curve in (c) with a phase angle $\theta = -270^o$ at $\omega = \infty$ can cross the *negative* X-axis and hence has the possibility of *enclosing* the point (-1,0). One must realize that the *negative* X-axis represents a phase angle of $-180^o$. At the point

where curve in (c) intersects the *negative* X-axis, we have $|A(j\omega_o)\beta|>1$, and $\arctan[A(j\omega)]=-180^o$. In terms of the polar plots in Fig.4.15(a)-(c), we can re-state Nyquist criterion as follows.

A negative feedback system with a forward gain *A(s)* and a feedback gain $\beta$ will be *potentially* unstable if the polar plot of $A(j\omega)\beta$ *encloses* or *passes through* the point (-1,0) on the X-axis. The word *encloses* implies that the point in question remains on the *right* of the curve which is described *clockwise* as the frequency $\omega$ spans the values from *zero* to *infinity*.

When the plot *passes* through (-1,0), we have the conditions $|A(j\omega_o)\beta|=1$, and $\arctan[A(j\omega)]=180^o$ satisfied exactly. When the plot *enclose* (-1,0), we have $|A(j\omega_o)\beta|>1$, while $\arctan[A(j\omega)]=-180^o$. In the both the cases, the system will be *potentially* unstable.

### 4.4.2 Applications of Nyquist criterion

#### *4.4.2.1 First order transfer function*

Consider $A(s)=K/(s+a)$, where *K* and *a* are constants.

The phase angle of $A(j\omega)$ is $-\arctan(\omega/a)$. As the frequency $\omega$ spans the values from *zero* to *infinity*, the angle will span the value from *zero* to $-\pi/2$ (i.e., $-90^o$). Figure 4.15(a) represents this case.

Thus, for a first order (i.e., order of denominator *minus* the order of the numerator=1) gain function (or, transfer function) the condition $\arctan(A(j\omega)) =-180^o$ will never arise.

Hence a *first* order gain (or transfer) function will remain stable according to Nyquist criterion.

#### *4.4.2.2 Third order function*

Consider $A(s)=\dfrac{K}{(s+a)(s+b)(s+c)}, c>b>a$ .

The phase angle is: $-\arctan(\omega/a)-\arctan(\omega/b)-\arctan(\omega/c)$. Each term can contribute up to $-90^o$ as the frequency to *infinity*. Hence, total phase angle can be $-270^o$. Thus, for a third order gain function, the phase angle can exceed $-180^o$ at some *finite* value of frequency. Figure 4.15(c) represents this case.

One can intuitively see that the gain function *A(jω)* must be of order *two* for the phase angle to become 180$^o$ in magnitude at *inifinite* frequency.

*Conclusion:* In general if a transfer function *A(s)* has $m_z$ number of simple (i.e., first order factors as $(s+z_i)$, $i=1,2,..$) zeros and $n_p$ number of simple (i.e., first order factors as $(s+p_i)$, $i=1,2,..$) poles, the phase angle at *infinite* frequency will approach $(m_z-n_p)$ times 90$^o$.

*Example 4.4.2.1*: Consider the gain function $A(s)=(\frac{10}{1+s/10^3})^3$. If the feedback ratio $\beta$ is independent of frequency, what value it should have so that the feedback system with the loop gain $A(s)\beta$ remains stable?

*Solution/hint:* First find the frequency where *arctan*(*A(jω)*) is -π radian, i.e., -180$^o$. For the given function *arctan* [*A(jω)*]$=-3\tan^{-1}(\omega/10^3)$. If this is to be -180$^o$ (i.e., π radians) we can solve for $\tan^{-1}(\omega/10^3)=\pi/3$ i.e., 60$^o$. The result is $\omega=1.732\times10^3$ rad/sec.

So at $\omega_o=1.732\times10^3$ rad/sec, *arctan*[1] [*A(jω)*] becomes -180$^o$.

Now, we need to check for $|A(j\omega_o)\beta|<1$, i.e., $\beta<1/|A(j\omega_o)|$.

From the given expression for *A(s)*, we find $|A(j\omega_o)|=|\frac{10}{1+j\frac{1.732\times10^3}{10^3}}|^3=5^3=125$.

Hence, for the feedback system to be stable, $\beta<1/125$ ,i.e., <0.008

4.4.3 Gain margin and Phase margin

From the above it is becoming clear that if at the frequency $\omega$ where *A(jω)* has a phase angle equal to -180$^o$, the quantity $|A(j\omega)\beta|$ remains <1, the possibility of instability can be avoided. Alternatively, if $|A(j\omega)\beta|$ becomes =1 at certain frequency $\omega$, but *ATan*[*A(jω)*] remains <-180$^o$ , the instability can be avoided.

The above inequalities are given more quantitative implications by the definitions of *gain margin* and *phase margin.*

The *gain margin* (GM) is the difference between the number 1 and the magnitude of *A(jω)* on the logarithmic scale, i.e., decibels (dB), when *ATan*[*A(jω)*] =-180$^o$. It is given by:

[1] Henceforth we will use *ATan* for *arctan*

GM=0- $20\log_{10}|A(j\omega)|$, i.e., - $|A(j\omega)|_{dB}$

The *phase margin* (PM) is the difference between $180^o$ and the magnitude of *ATan*[*A(jω)*] in degrees, when $|A(j\omega)\beta| = 1$. It is given by:

PM=$180^o$ - $|ATan[A(j\omega)]|_{\text{degrees}}$

A rule of thumb for a stable negative feedback system design is to maintain a GM $\geq 20$ dB, and/or a PM $\geq 45^o$.

*Example 4.4.3.1*: Consider an amplifier with an open loop gain of $A_o = 10^5$. At high frequencies it is modeled as a single time-constant system with a pole frequency $f_p = 10$ Hz. The amplifier is connected in a negative feedback with a closed loop gain of +100 at low frequencies.

At what frequency will $|A(jf)\beta| = 1$? What is the phase margin?

*Solution/hint:*

The high-frequency model of the amplifier is $A(jf) = \dfrac{A_o}{1 + j\dfrac{f}{10}}$.

The feedback gain at *low-frequency* is $\dfrac{A_o}{1 + A_o\beta}$, which is given as +100, with $A_o = 10^5$.

Solving for $\dfrac{10^5}{1 + 10^5\beta} = 100$, one gets $\beta = 0.01$.

Now we set up the equation $\dfrac{10^5 \times 0.01}{|1 + j\dfrac{f}{10}|} = 1$, for $|A(jf)\beta| = 1$. On solving, we get $f = 10^4$ Hz.

For phase margin, we need to find *ATan*[*A(jf)*] at $f = 10^4$ Hz. That is $-ATan(10^4/10)$ which is $\approx -90^o$. Hence the PM is $180^o - |-90^o| = 90^o$, i.e., 90 degrees.

## 4.4.4 Frequency compensation

Frequency compensation modifies the frequency response of the feedback system so that the system remains stable. In particular, the gain function of the amplifier is modified such that at a frequency where the phase shift of the amplifier is equal or close to -$180^o$, the gain magnitude is reduced to a value below unity by a good margin.

A high gain amplifier, such as an OP-AMP, containing several devices (i.e., transistors) the gain function will in general be of order three or more. From the discussion in section 4.4.2 we can infer that the phase angle will reach the value of $180^o$ at some (*finite*) frequency in between the second and the third pole of the frequency response function.

Thus, if the gain of the amplifier is reduced to *unity* at the frequency of the *second pole*, the gain magnitude will assume a value less than *unity* at the frequency of -180$^o$ phase shift. Figure 4.16 clarifies the concept.

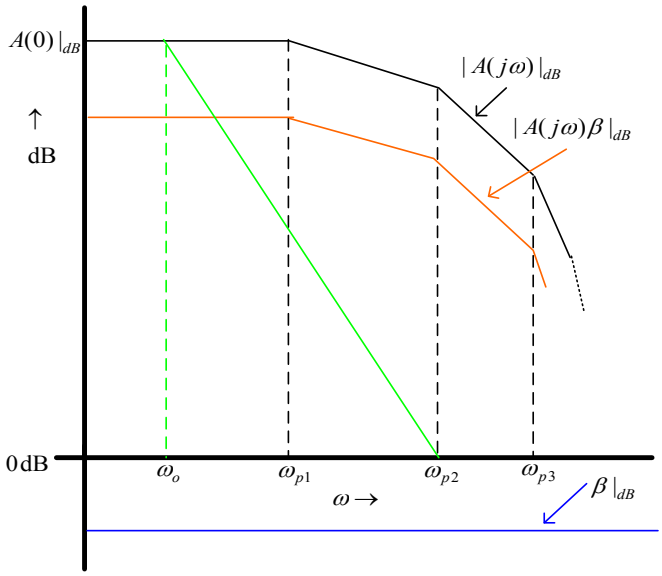



Figure 4.16: An amplifier gain plot and construction of the compensated gain curve

In a practical feedback system, the quantity $\beta$ is always < 1, so that the loop gain $|A(j\omega)\beta|$ will become <<1 when $|A(j\omega)|$ is rendered <1. Hence a substantial GM will be achieved which, in turn, will render the system *stable*.

In Figure 4.16 we can erect a line at the second pole ($\omega_{p2}$) with a slope of +6 dB/octve (i.e., +20 dB/decade) and extend it upwards until it intersects the mid-band segment (see *green* line in Fig.4.16) of the gain curve. If the corresponding frequency is $\omega_o$, the system can now be viewed as a *first order* system with the pole at $\omega_o$. In other words, the gain function of the frequency compensated can now be formulated as $\frac{A(0)}{1+s/\omega_o}$. Since this represents a *first order* system, it will be stable under negative feedback.

In terms of the compensated gain curve (*green* line in Fig.4.16), at frequencies >> $\omega_o$, the gain will change as $A(0)\omega_o/s$. This will become equal to *unity* (i.e., 0 dB) in magnitude at $\omega = \omega_t = A(0)\omega_o$. The frequency $\omega_t$ is the *unity gain-bandwidth* of the frequency compensated amplifier. In terms of Fig.4.16, since the compensated gain curve starts off from zero dB (=*unity* in value) at $\omega_{p2}$, the $\omega_t$ equals $\omega_{p2}$, the second pole of the frequency uncompensated amplifier. Thus $A(0)\omega_o=\omega_{p2}$.

Viewed from another angle, since the compensated gain curve falls off at 20dB/decade from the value $A(0)|_{dB}$, an alternative relation between the -3dB frequency (i.e., $\omega_o$) of the

compensated curve and the second pole $\omega_{p2}$ of the uncompensated curve is $\omega_o = 10^{-m}\omega_{p2}, m = {A(0)|_{dB}}/{20}$ .Thus,

$\omega_o = {\omega_{p2}}/{A(0)} = 10^{-m}\omega_{p2}$, where $m = {A(0)|_{dB}}/{20}$.

*Example 4.4.4.1:* Consider a multi-stage voltage amplifier with a low-frequency gain of 100 dB and poles at 10,000 rad/sec, 30,000 rad/sec and $10^5$ rad/sec.

(a) Write an expression for the gain of the amplifier as a function of frequency.
(b) Find the frequency at which the phase angle of the gain function reaches -180°.
(c) Assuming that we need to maintain a gain margin of 20 dB, suggest the procedure to accomplish the task and calculate the new *compensated* pole of the compensated first order system.
(d) Assuming that we adopt a frequency compensation scheme to fix the *unity gain* bandwidth at the second pole of the uncompensated amplifier, what will be the realized gain margin relative to the *uncompensated* gain response curve?

*Solution/hint*:

(a) Since 100 dB is equivalent to the ratio $10^5$, the gain function can be expressed as

$$A(j\omega) = \frac{10^5}{(1+j\frac{\omega}{10000})(1+j\frac{\omega}{30000})(1+j\frac{\omega}{10^5})}$$

(b) The phase angle (in *radians*) of the gain function is

$$\varphi = -ATan(\frac{\omega}{10000}) - ATan(\frac{\omega}{30000}) - ATan(\frac{\omega}{10^5})$$

From the analysis presented in section 4.4.2, it is understood that the phase angle will be -180° (i.e. –π radians) at a frequency in between the second and the third poles. At this frequency, the contribution due to the first pole will be close to -90°.

Thus we need to solve for $\frac{\pi}{2} = ATan(\frac{\omega}{30000}) + ATan(\frac{\omega}{10^5}) = ATan\frac{\frac{\omega}{30000}+\frac{\omega}{10^5}}{1-\frac{\omega^2}{3\times10^9}}$

Since *tan*(π/2) is *infinity*, the solution is $1-{\omega^2}/{3\times10^9}$ =0, or $\boldsymbol{\omega}$**=54,772.26** rad/sec.

(c) According to the principle of frequency compensation discussed in section 4.4.4, the gain magnitude (in dB) at 54,772.26 rad/sec will be forced to -20 dB. The response curve will be a straight line rising upward at +20 dB/decade of frequency (characteristic of a first order pole) beginning from -20 dB at 54,772.26 rad/sec.

Since the low-frequency (i.e., mid-band) gain is 100 dB, the straight line will have to rise by 120 dB, i.e., by 120/20=6 decades of frequency, to intersect the mid-band gain line (see Fig.4.16, the *green* line). Hence, the new *compensated pole* frequency will be located at 54,772.26/$10^6$, i.e., **0.05477** rad/sec.

(d) If the compensated curve is set to *zero* dB (i.e., *unity* value) at $\omega$=30,000 rad/sec, the *compensated* pole will be at $30{,}000\times10^{-100/20}$=0.3 rad/sec. The *compensating* straight line of slope 20db/decade will now glide down from 0.3 rad/sec., to 54,772.26 rad/sec which is the frequency of -180$^o$ phase angle of the *uncompensated* frequency response curve.
The frequency 54,772.26 is $\log_{10}$ (54772.26/0.3)=5.26 decades above the *compensated* pole of the system. The compensated gain curve will drop by 105.23 dB (i.e., @ 20 dB/decade) over 5.26 decades. So the gain will reach a value of 100-105.23=-5.23 dB.
The gain margin relative to the *uncompensated* gain response curve will be 5.23 dB.

Quiz? Will the system be stable with only 5.23 dB of gain margin? Justify your answer.
*Example 4.4.4.2*: Repeat *example* 4.4.4.1 for an amplifier gain of 60 dB and the pole frequencies of 20,000, 60,000, and 200,000 rad/sec.

*Hint:* Following similar procedure as in *example* 4.4.4.1, the frequency for -180$^o$ phase shift will be $\sqrt{6\times2\times10^9}$ rad/sec. Proceed on.

4.4.5: A technique to implement frequency compensation

The simplest technique to implement the frequency compensation in a multi-stage voltage amplifier system (i.e., an OP-AMP) is to locate two output nodes in the chain of amplifiers with a known *low-frequency* gain. Suppose these nodes are labeled as *m* and *p* respectively with an inter-stage gain of -$K_{mp}$ (take note of the *negative* sign). If we connect a capacitor *C* between nodes *m* and *n*, this will be reflected as a capacitor $(1+K_{mp})C$ (by Miller's theorem) between node *m* and ground. If $R_{om}$ is the output resistance at the node *m*, the Miller magnified capacitor and the resistor forms a time constant of $(1+K_{mp})CR_{om}$.

The frequency compensation technique involves setting the *compensated pole* of the amplifier (i.e., 0.05477 radian/sec, in part (c) of *example 4.4.4.1*) equal to inverse of the time constant, i.e., equal to $1/(1+K_{mp})C$. We can then determine the value of the necessary compensating capacitor *C*.

In practice, however, we include a *lead* compensation by inserting a resistance in series with the capacitor *C*. This resistance can be realized, in an integrated circuit technology, by diode connected transistor(s). The interested student may refer to more advanced text books on this subject.[2]

### 4.5 Additional practice exercises

Q.1: Consider a feedback amplifier with open-loop gain of $10^4$ at low frequencies. It has a -3 dB frequency of 100 Hz. Under negative feedback the low-frequency (closed loop) gain becomes 50.
(a) Write an expression for the frequency-dependent gain of the amplifier.
(b)What will be the -3 dB frequency under negative feedback?
(c) What is the loop gain (i.e., Aβ) at low-frequency?
(d) What is the feedback factor (i.e., 1+Aβ) at low frequency?

Q.2: You need to amplify a signal from a microphone and deliver to a speaker. The mike produces 10 mV ac signal and has an output resistance of 5 kΩ. The signal input to the speaker pre-amplifier must be 0.5 V ac and the input resistance of the pre-amplifier is 50 Ω.
You are given an OP-AMP with $R_i$ =10 kΩ, $R_o$ =100 Ω, and a low-frequency open loop gain of $10^4$. Use negative feedback principle to design the driver stage between the mike and the pre-amplifier. Neglect frequency dependence of gain.

(hint: *The OP-AMP output resistance has be lot smaller than pre-amplifier input resistance. So a negative feedback with shunt connection at output will be required. Similarly, the input resistance of the OP-AMP should be lot higher than just 10 kΩ. This can be achieved with … ? feedback connection that at the input*. Proceed further.)

Q.3: Design a feedback amplifier producing a closed loop current gain of 10. The current source has $R_S$ =10 kΩ, and the load is $R_L$ =50 Ω. An OP-AMP with $R_i$ =10 kΩ, $R_o$ =100 Ω, $A_{vo}$ =$10^4$ can be used as the active device.
(hint: *a shunt-in, series-out feedback will be required around the OP-AMP (why?). Proceed further)*

Q.4: deleted
Q.5: Consider the single stage BJT amplifier in figure P.5(a) with a shunt-shunt feedback applied via $R_F$= 82 kΩ. The bias current is $I_C$= 0.5 mA. Given that $h_{fe}$=99, $V_{BE}$ (ON)=0.7 V, $V_A$ = infinity. Find the trans-resistance gain of the system under negative feedback.

[2] *Analog Integrated Circuit Design* (ch.5) by David A. Johns and Ken Martin, John Wiley & Sons Inc.,© 1997, ISBN 0-471-14448-7.

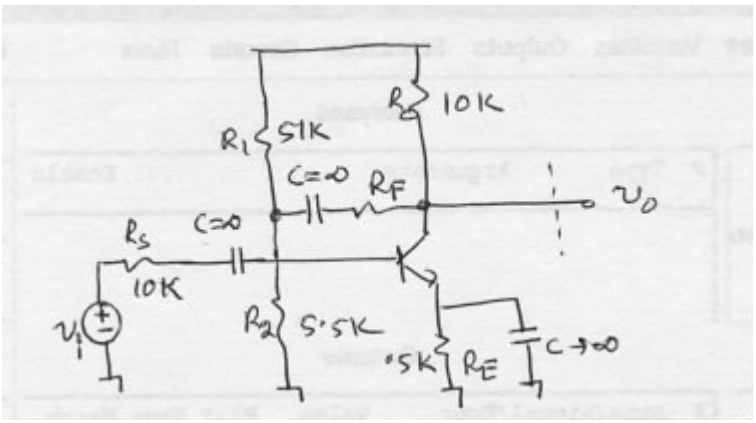



Figure P.5(a):

(hints: $r_\pi = 5\,k\Omega$, $g_m = 18.9\ mA/V$, $A_f = \frac{v_o}{i_s} = -65.8\ k\Omega$. *Use the ac equivalent circuit given in Fig.P.5(b).*)

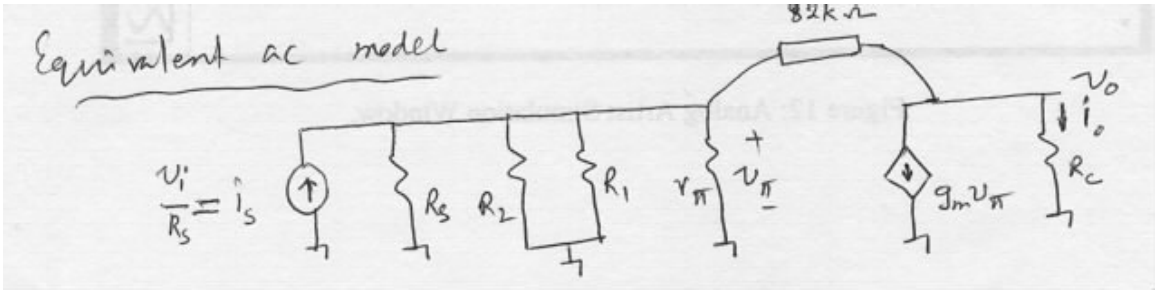



Figure P.5(b):

Q.6: A three-pole amplifier has a loop-gain function $T(f) = \frac{100\beta}{(1 + j\frac{f}{10^5})^3}$. Determine the stability condition of this function for (i) β=0.2, and β=0.02. (hint: Determine the frequency where phase angle of *T(f)* is 180 degrees. Then find |T(f)| at this frequency for the different values of β. Then comment on these results.)

Q.7: Consider a three-pole feedback amplifier with a *loop gain* function given by:

$T(f) = \frac{100\beta}{(1 + j\frac{f}{10^3})(1 + j\frac{f}{5\times10^4})(1 + j\frac{f}{10^6})}$. Determine the value of β that yields a phase margin of 45 degrees. (hint: Find *f* where *T(f)* has -135$^o$ of phase angle. Use this *f* and set $|T(f)|=1$. You will find $\beta = 0.705$ (approx.))

Q.8: For the loop gain function in Q.6 above, find $\beta$ (i) at which the system becomes unstable, (ii) at which the system has a phase margin of 60$^o$. (ans: 0.08, 0.022 respectively).

Q.9: Given a 3-pole feedback amplifier with a *loop gain* function $T(f)=\dfrac{5\times10^5}{(1+j\frac{f}{10^6})(1+j\frac{f}{10^7})(1+j\frac{f}{10^8})}$, find a compensating dominant pole frequency ($<<10^6$ Hz) which will ensure stability of the system by maintaining a phase margin of $45^o$ at $f=10^6$ Hz. (hint: *the new dominant pole can be M decades below $10^6$ where* $M=20\log_{10}(5\times10^5)/20=5.7$. *Then proceed*.)

Q.10: Consider Figures P.10(a)-(b) which are examples of series-series negative feedback using BJT and MOSFET devices respectively. The feedback elements are $R_{E2}$, and $R_{S2}$ respectively.
(a) Draw the ac equivalent circuit for the loaded amplifier corresponding to Fig.P.10(a).
(b) Draw the ac equivalent circuit for the loaded amplifier corresponding to Fig.P.10(b).

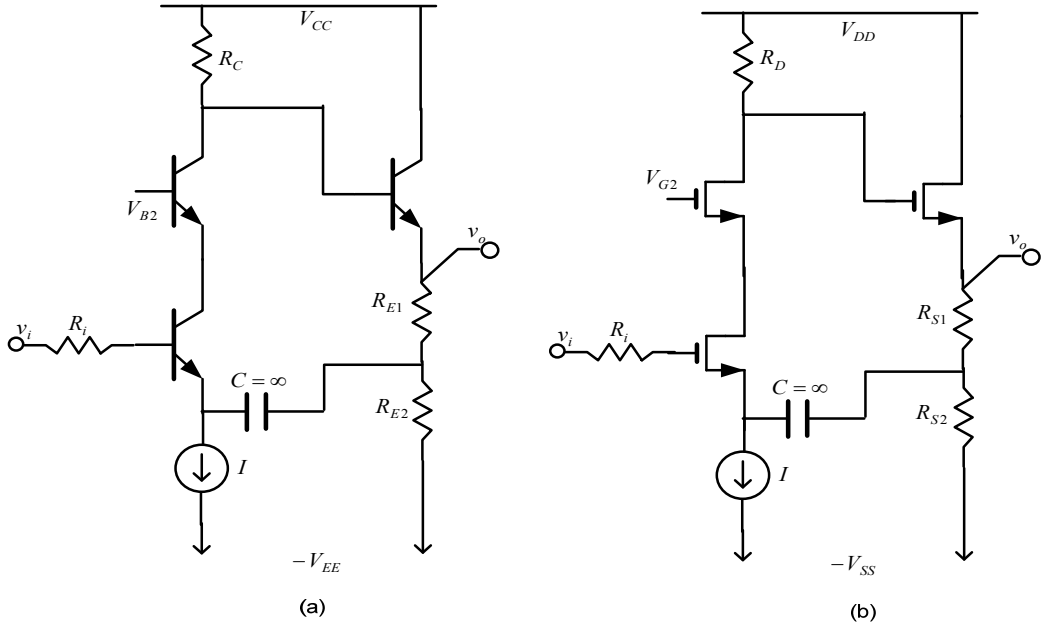



Figure P.10:

Q.11: Consider Figures P.11(a)-(b) which are examples of series-shunt negative feedback using BJT and MOSFET devices respectively. The feedback elements are $R_{E1}$, and $R_{E2}$ in (a), and $R_{S1}$, and $R_{S2}$ in (b).

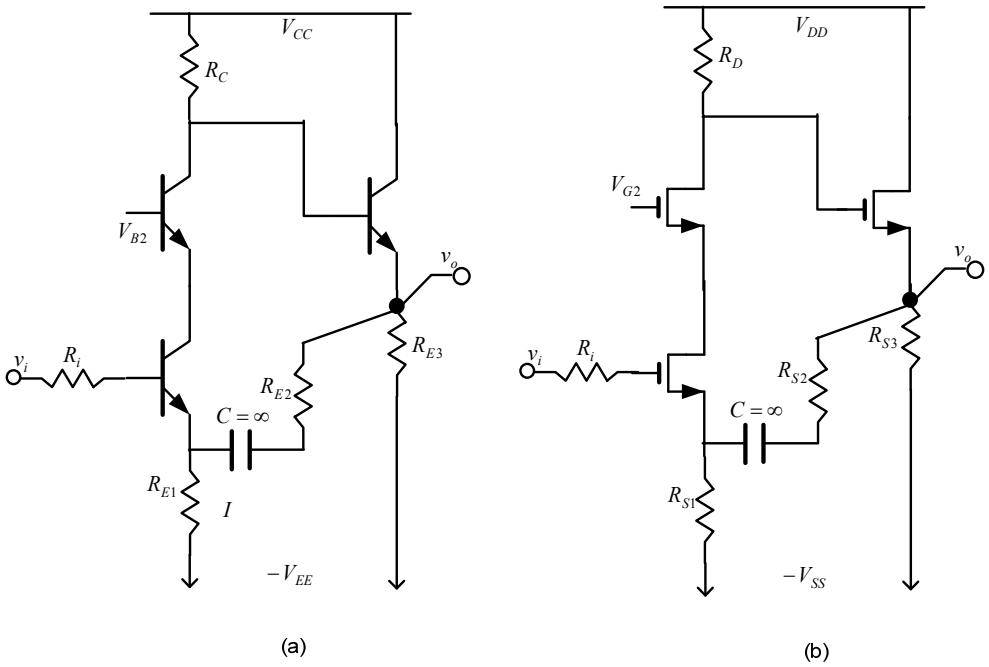



Figure P.11:

(a) Draw the ac equivalent circuit for the loaded amplifier corresponding to Fig.P.11(a).

(b) Draw the ac equivalent circuit for the loaded amplifier corresponding to Fig.P.11(b).

Q.12: Consider Figures P.12(a)-(b) which are examples of shunt-series negative feedback using BJT and MOSFET devices respectively. The feedback elements are $R_{E1}$, and $R_{E2}$ in (a), and $R_{S1}$, and $R_{S2}$ in (b).

(a) Draw the ac equivalent circuit for the loaded amplifier corresponding to Fig.P.12(a).

(b) Draw the ac equivalent circuit for the loaded amplifier corresponding to Fig.P.12(b).

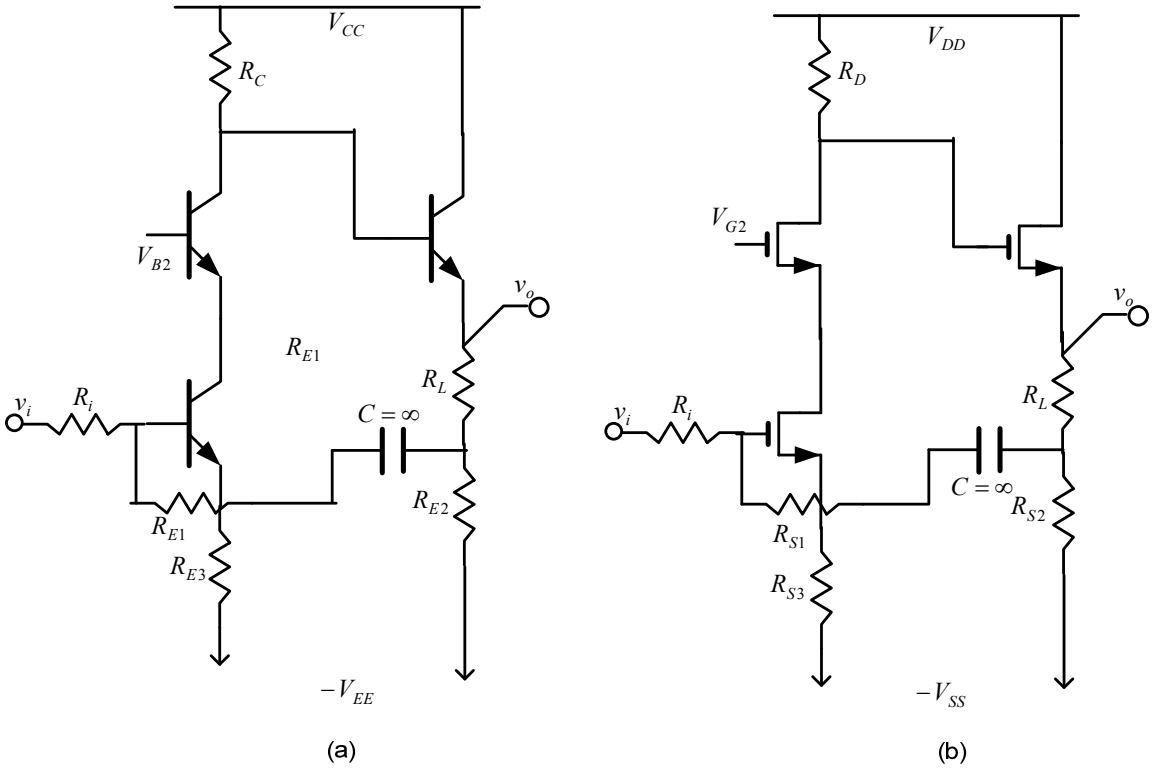

$V_{CC}$
$R_C$
$V_{B2}$
$v_o$
$R_{E1}$
$R_L$
$v_i$
$R_i$
$C = \infty$
$R_{E2}$
$R_{E1}$
$R_{E3}$
$-V_{EE}$
(a)
$V_{DD}$
$R_D$
$V_{G2}$
$v_o$
$R_L$
$v_i$
$R_i$
$C = \infty$
$R_{S2}$
$R_{S1}$
$R_{S3}$
$-V_{SS}$
(b)

Figure P.12:

# Chapter 5

# OUTPUT STAGES IN A VOLTAGE AMPLIFIER SYSTEM

5. Output Stage, desirable characteristics

The output stage is supposed to deliver the final output to an appropriate receiving device, i.e., a lamp, human ear, loud speaker, etc. Within the limits of given DC power supplies, the output stage should provide maximum amount of signal power to the load without large dissipation of electrical signal energy as heat. In a voltage amplifier system, the output resistance should be very low. Further, the output signal waveform should be very close replica of the input signal which means that the output should have very small *distortion* characteristic. Usually when devices deliver high power, the operation creeps into the domain of nonlinear characteristics and hence harmonics of the signal are generated at the output. A measure of these harmonics is expressed by Total Harmonic Distortion (THD). A high fidelity audio amplifier will perhaps have a THD of the order of a fraction of a percent i.e., 0.1%.

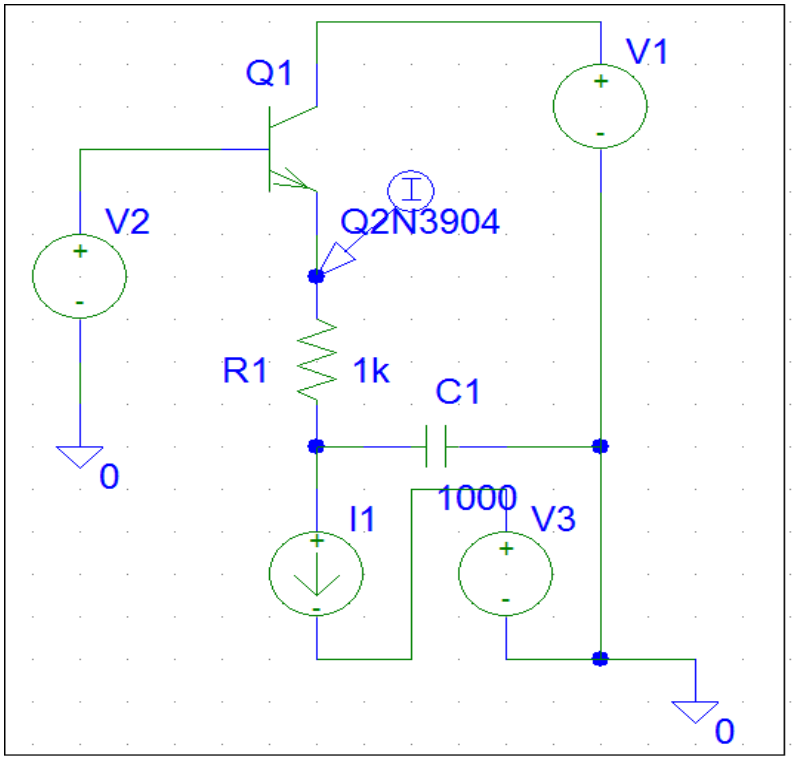
The most challenging task in the design of the output storage is that it delivers the required amount of power to the load in an efficient manner i.e., with as little as possible of power dissipation in the transistors at the output stage. The efficiency depends upon the way the output stage conducts upon application of the signal power. This is achieved by special DC biasing of the transistor. Thus we come across class A, class B and class AB stages. The following are discussed in this chapter.

- Different DC biasing of output stages and associated characteristics
- Special circuits for class AB biasing
- Short circuit protection technique
- Thermal considerations
- Power transistors

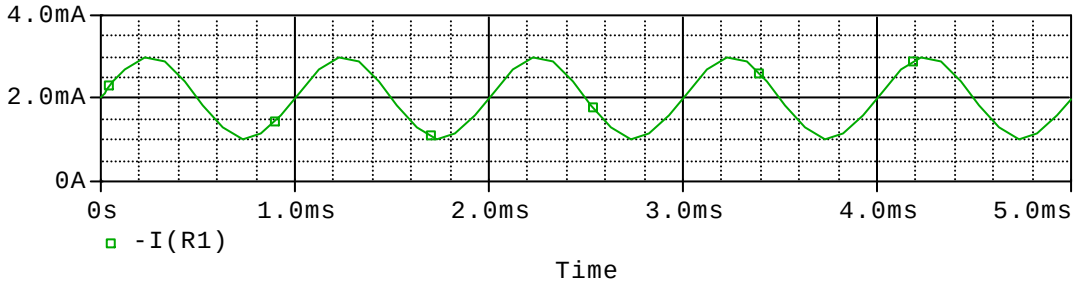
5.1: Operation by Different Biasing

5.1.1: Class A operation

In class A operation, the output stage is biased at a DC current level $I_C$ which is greater than the peak signal component of the current $I_m$ . Thus, if the signal is sinusoidal, the instantaneous current through the device never falls below zero over the entire cycle of the input signal. That means the conduction angle of the output stage is 360°, i.e. full cycle. Figures 5.1(a)-(c) demonstrate the concept. The device Q1 is biased with *I1*=2mA. The capacitor *C1* is for isolating the DC and is assumed as a *short circuit* for *ac* signals. When an input signal $v_I$ of value $V_m$ is applied, the current $i_E$ through the emitter resistance *R1* follows the input sinusoidal variation as $v_I/R1$. As long as $|V_m/R1|$ is less than *I1*, the waveform of $i_E$ resembles that of $v_I$ (Figs. 5.1(b)-(c)). When $|V_m/R1|$ exceeds the DC bias current *I1*, $i_E$ becomes *zero* during the negative going excursion of $v_I$. Thus, the condition of class A operation is violated (Fig.5.1(d)). The current through *R1* and hence the output signal voltage suffers distortion.




(a)

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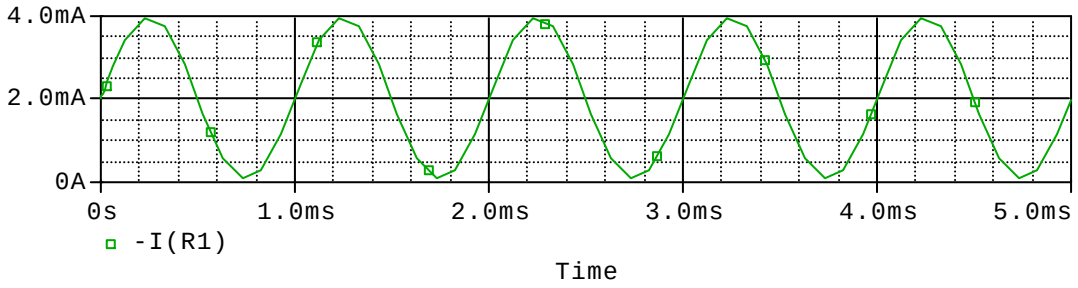


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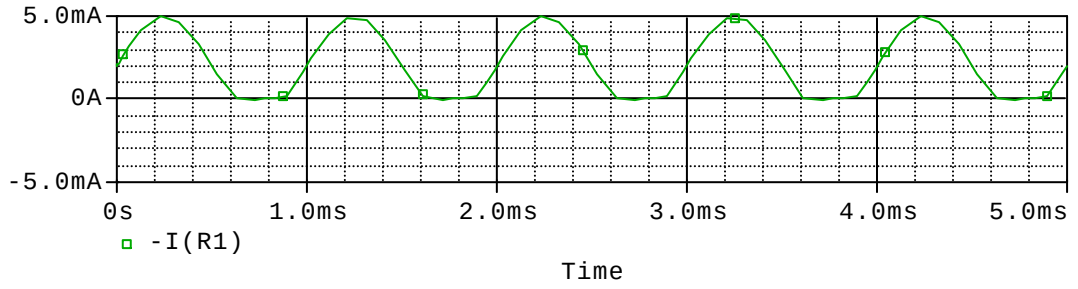
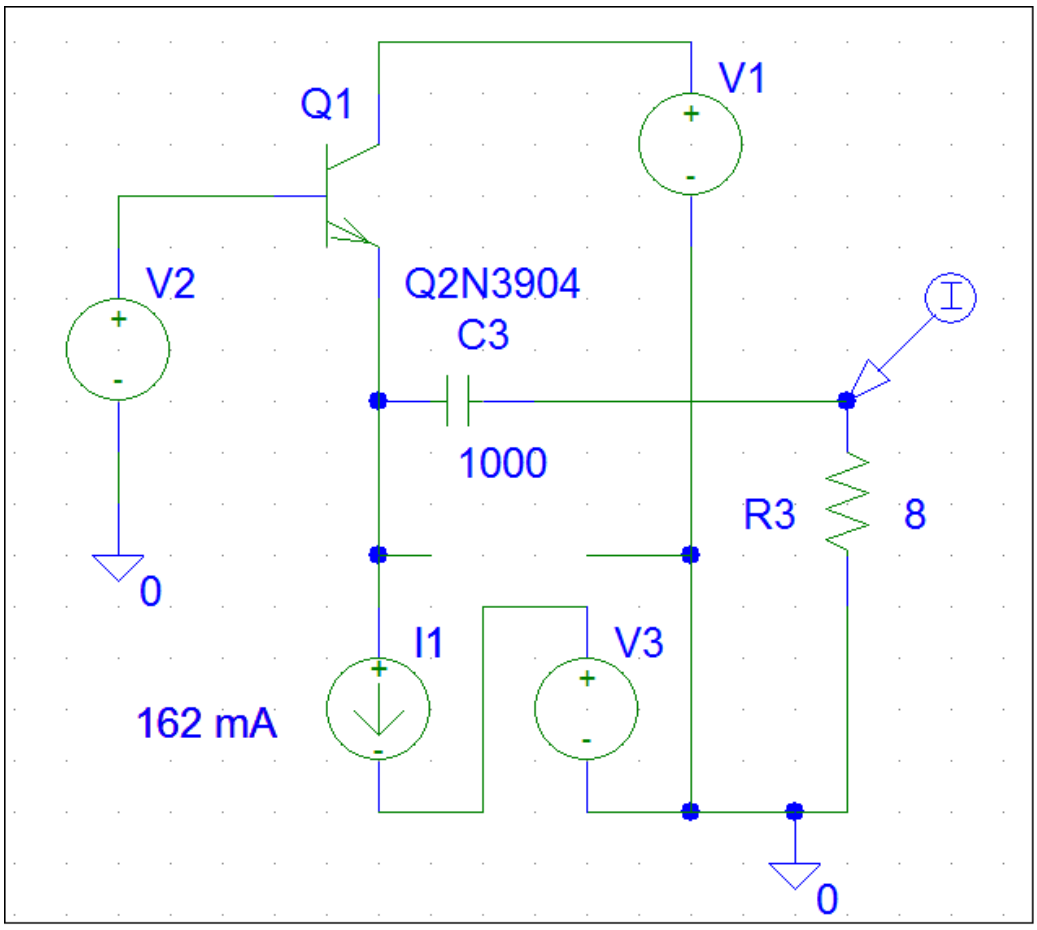



(d)

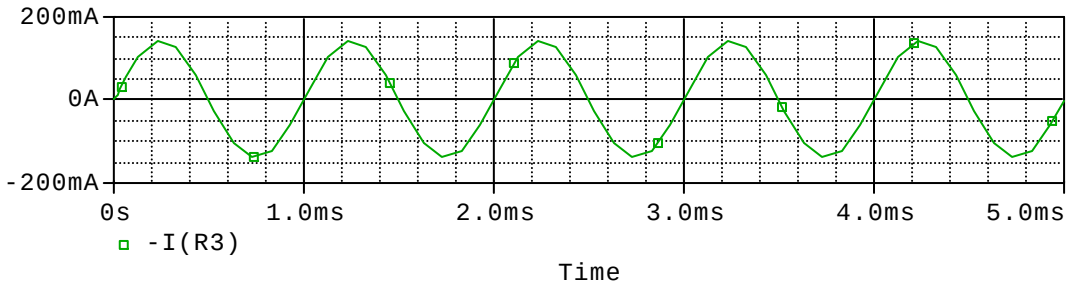
Figure 5.1: DC bias current vs. signal handling capability of Class A output stage (a) the schematic with NPN-BJT device biased for $I_E$=2 mA, (b) VSIN=1V peak, $i_E$=1 mA (peak) sinusoidal around 2 mA DC bias, (c) VSIN=2V peak, $i_E$=2 mA (peak) sinusoidal around 2 mA DC bias, (d) VSIN=3V peak, $i_E$=3 mA positive peak but cutting off toward the negative peak , being limited by the 2 mA DC bias.

Considering from output side, if the amplifier is required to deliver a given level of voltage (say, $v_{om}$) across the output load (say, $R_L$), the DC bias level should be sufficient

( i.e., > $|v_{om}/R_L|$) so that the transistor never cuts off (i.e., $i_E$ becoming=0) for class A operation. Figure 5.2(a)-(c) illustrate the situation. The schematic in Fig.5.2(a) shows a CC-BJT amplifier output stage biased by a current source and having a load of 8 ohms. It is intended for an output signal power of 100 mW. This corresponds to a peak *ac* current of $I_m$=160 mA. The capacitor *C3* is for isolating the DC and is assumed as a *short circuit* for *ac* signals. The DC bias current is set for 162 mA (i.e., > $I_m$= 160 mA). Figure 5.2(b) shows the case for a load current drive of 150 mA ($v_{in}$ =1.2V peak Sine-wave), while Fig.5.2(c) depicts the case for a load current drive exceeding the DC bias current of 162 mA. This happens for an input signal drive of 2.5V peak Sine-wave requiring the load current to be (noting that the CC stage has a voltage gain close to unity) 312.5 mA. This current exceeds the DC bias current arranged in Fig.5.2(a). The BE junction of the BJT device cuts off for the duration when the signal current remains below -162 mA (see Fig.5.2(d)). Hence, the output signal (current/voltage) encounters distortion over this duration of time.



(a)

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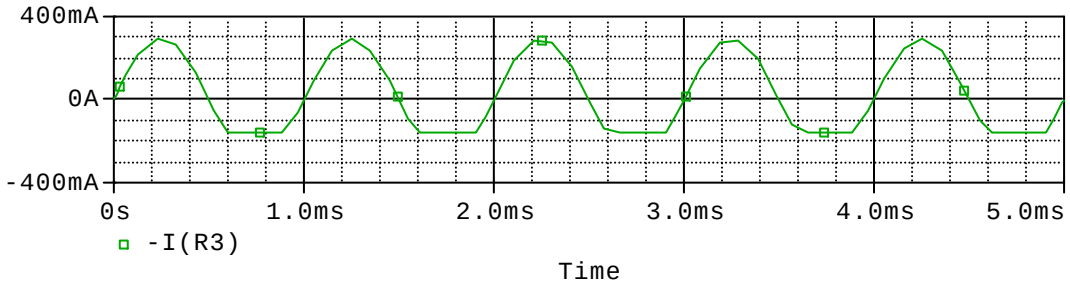
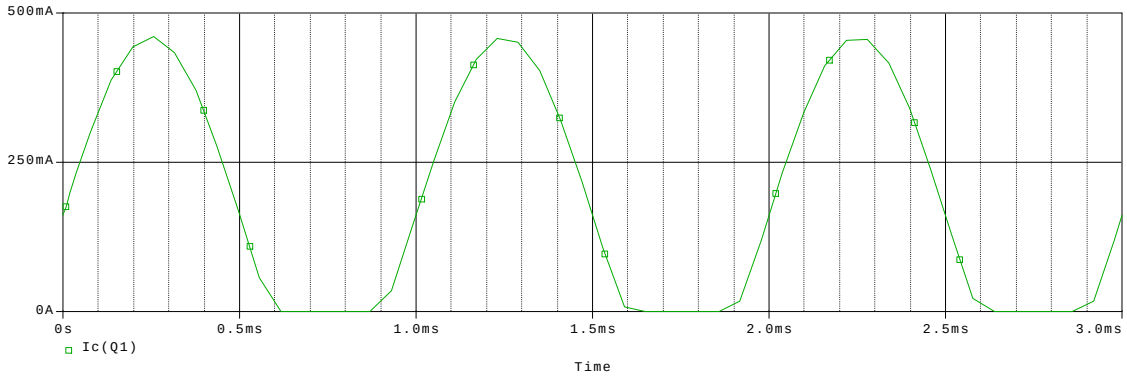



(c)




(d)

Figure 5.2: A CC-BJT output stage rated for 100 mW of output power ($v_L$=1.28V peak); (a) the schematic, (b) output current for $v_L$=$v_{in}$=1.2V peak, (c) output current for $v_L$=$v_{in}$=2.5V peak, (d) current through the BJT device for $v_L$=$v_{in}$=2.5V peak

*5.1.1.1: Bias current circuit design*

Consider a CC-BJT amplifier in an IC environment where the device $Q_1$ (an NPN BJT device) is biased by the current-mirror circuit comprised of $Q_2$ and $Q_3$ (see Figure 5.3). The instantaneous load current is $i_L$, and the dc bias current is I. Then

$$i_{E1} = I + i_L$$

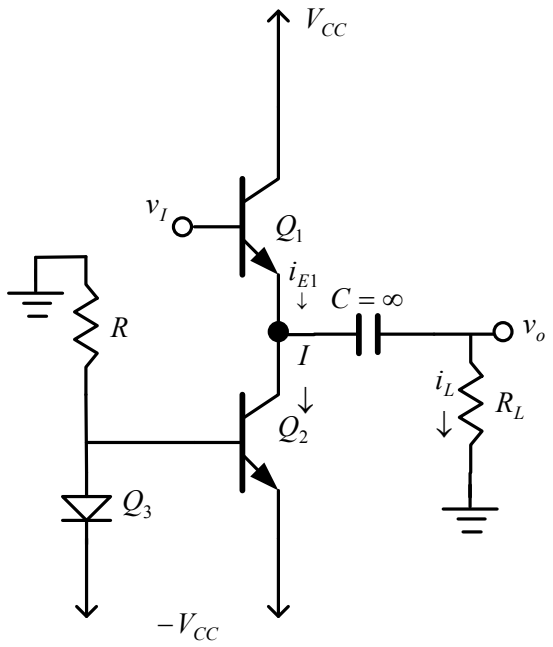



Figure 5.3: Class A output stage biased by a diode connected transistor $Q_3$. $Q_2$ serves as a bias source for $Q_1$.

For class A operation, $i_{E1}$ is always > 0 ie $I > i_L$. In the linear operation region, maximum positive output is $v_o^+|_{max}=V_{CC}-v_{CE,sat}|_{Q1}$ . Similarly, maximum negative output is $v_o^-|_{max} =-V_{cc}+v_{CE,sat}|_{Q2}$

Corresponding to the worst case negative swing at the output, the load current will be $i_L = \frac{-V_{CC} + v_{CE,sat}|_{Q_2}}{R_L}$, where $R_L$ is the load resistance. Since, for class A operation $I > i_L$, then $I > i_L = \frac{-V_{CC} + v_{CE,sat}|_{Q_2}}{R_L}$, gives a guideline for designing the proper DC bias current for class A operation. On the positive swing side: $I \le \frac{V_{CC} - v_{CE,sat}|_{Q1}}{R_L}$. In a practical case one need to choose higher of the two possible values of $I$. The biasing resistance in the reference current source transistor ($Q_3$) can now be chosen as (ignoring the effect of finite *beta* of the BJT)

$$R \le \frac{0-(-V_{CC}+0.7)}{I}$$

*Example 5.1.1.1*: In Fig.5.3 consider $V_{CC}$ =15V, $V_{CE(sat)}$=0.2V, $V_{BE}$=0.7V, and that $h_{FE}$ is very high. Find $R$ to allow for the largest possible output signal swing across the load $R_L$=1kΩ. Determine the minimum and maximum currents through the device $Q_1$.

*Solution/hints*:

Maximum signal swing =15-0.2=14.8V peak (both positive and negative)

Peak load current $i_L$=14.8V/1kΩ=14.8 mA (both positive and negative)

For class A operation, $i_{E1} = i_L + I$ will always be > 0, so $I$ =14.8 mA.

With $h_{FE}$ very high, $I_{REF} = I_C$ in $Q_3$ will be =$I$=14.8 mA.

With $V_{BE}$ =0.7V, $R$ =[(-15)+0.7]/14.8 mA=0.97kΩ.

Minimum (instantaneous) current through $Q_1$= 0

Maximum (instantaneous) current through $Q_1$ =14.8 times 2=29.6 mA (assuming a sinusoidal input signal).

*5.1.1.2: Power conversion efficiency*

In the class A amplifier the DC power consumption is = $I(V_{CC}$ in $Q_1 - (-V_{CC}$ in $Q_2)) = 2IV_{CC}$ → both carrying average current $I$ and bus to bus voltage being $2V_{CC}$. Let $P_s = 2IV_{CC}$ be the power drawn from the supply bus.

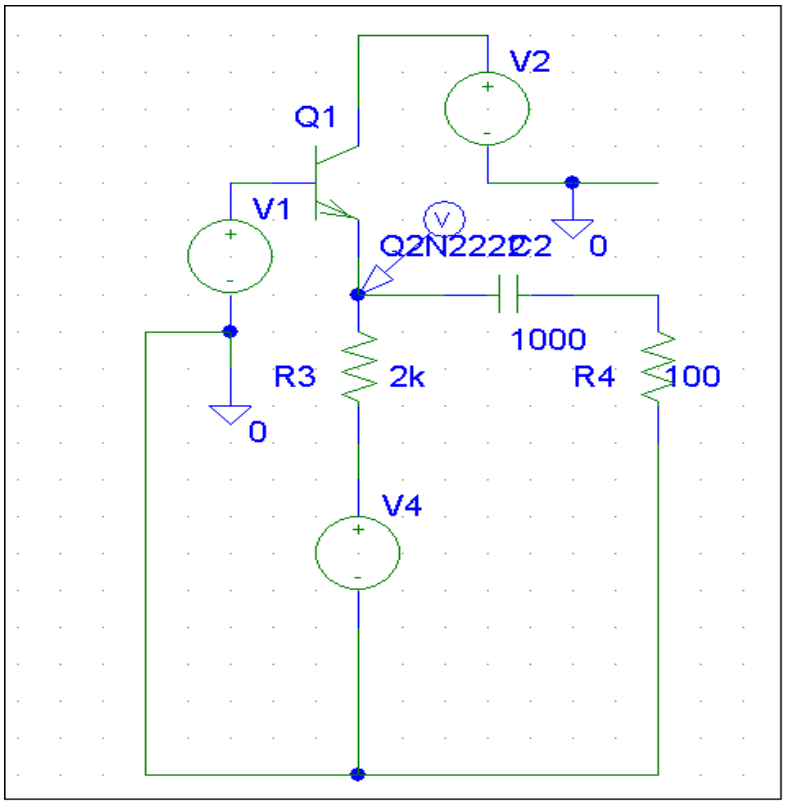
Average *ac* (sinusoidal) signal power delivered to the load is : $P_L = \frac{\hat{v}_o^2}{2R_L}$, where $\hat{v}_o$ is the peak output *ac* voltage.

Efficiency of power conversion $\eta = \frac{P_L}{P_s} = \frac{1}{4}\frac{\hat{v}_o^2}{V_{CC} I R_L}$.

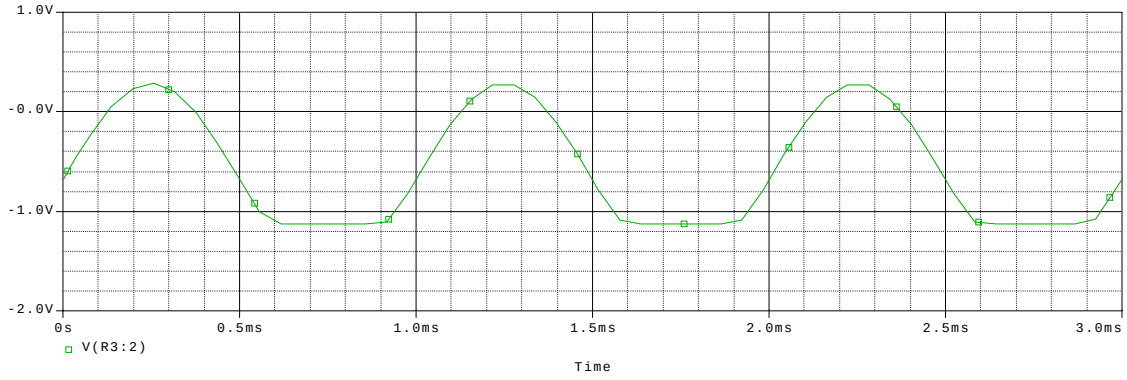
The highest value of the efficiency will be ¼, i.e., 25% when $\hat{v}_o = V_{CC} = IR_L$. In general, since $\hat{v}_o < V_{CC}$, and $\hat{v}_o < IR_L$ the power conversion efficiency will be < ¼, i.e., 25 %. The best case efficiency that can be obtained in a Class A operation is thus 25%.

5.1.2 : Class B operation

In class B operation, the DC bias current through the device (Fig.5.4(a)) is kept at zero. So the device conducts current for only ½ of the input signal cycle (Fig.5.4(b)). The conduction angle is thus, 180. The output signal is highly non-linear. To overcome this drawback a complementary pair of PNP and NPN transistors is used in practice.




(a)



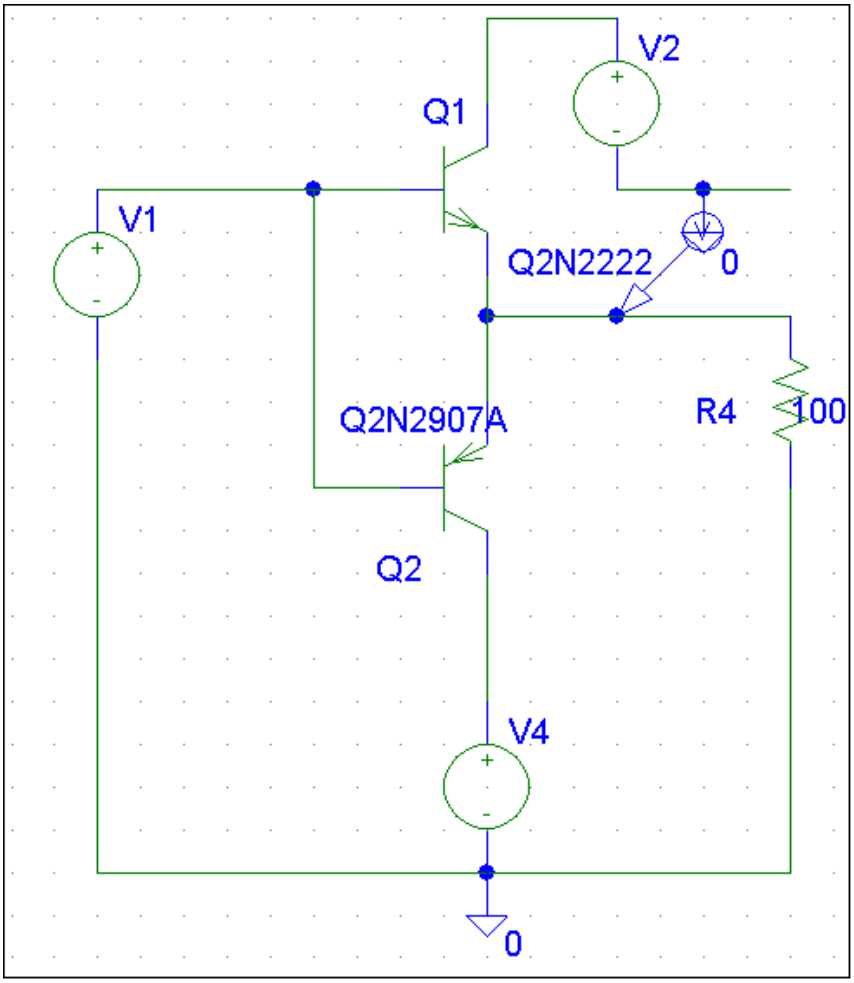

(b)

Figure 5.4: Class B amplifier stage (a) schematic (in PSpice), (b) output waveform at the emitter of the BJT.

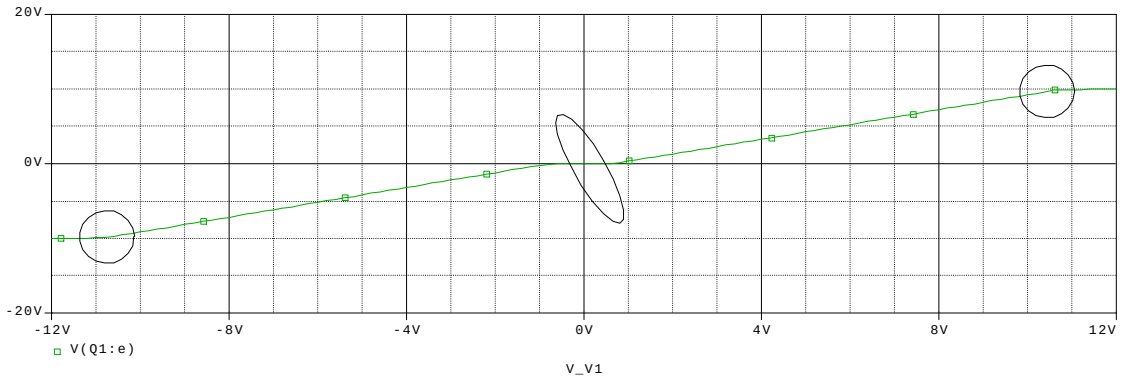
5.1.2.1: *Practical Class B output stage*

A practical class B amplifier using BJT devices appears as in Fig.5.5(a). The linearity characteristic of the amplifier is shown in Fig.5.5(b) and the output waveform with a

sinusoidal input signal appears as in Fig.5.5(c). The linearity characteristic (Fig.5.5(b)) shows saturation at the limits of the DC supply voltages (±10V in this case) and the *crossover* (i.e., no-conduction zone shown by an *elliptic* curve in Fig.5.5(b)) zone when in the input is within $\pm V_\gamma$ , where $V_\gamma$ is the cut-in voltage of the emitter-base junction of the transistors.




(a)

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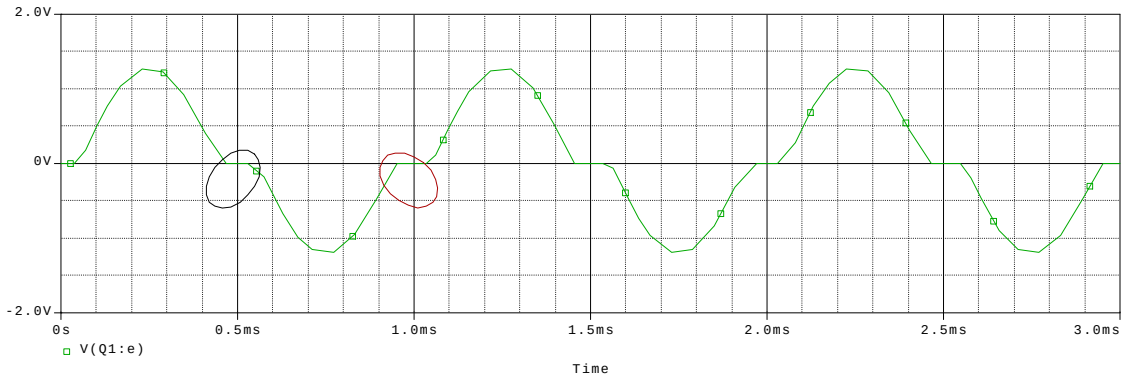



(c)

Figure 5.5: (a) Schematic of a class B output stage using BJT devices, (b) large signal output-input characteristic, (c) output with sinusoidal input.

Figure 5.5(c) shows the output for an input sinusoidal signal. The region of no (or poor) conduction corresponds to zero (or very small) output (shown by elliptic enclosure). This produces distortion components at the output. The distortion is referred to as *crossover* distortion since the distortion occurs when the current conduction changes over from one transistor (say, the NPN) to the other (i.e., the PNP) and vice versa. SPICE analysis of the

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(R_R4)

DC COMPONENT = -3.004535E-02

| HARMONIC NO | FREQUENCY (HZ) | FOURIER COMPONENT | NORMALIZED COMPONENT | PHASE (DEG) | NORMALIZED PHASE (DEG) |
|---|---|---|---|---|---|
| 1 | 1.000E+03 | 1.070E+00 | 1.000E+00 | 1.796E+02 | 0.000E+00 |
| 2 | 2.000E+03 | 1.806E-02 | 1.687E-02 | 9.215E+01 | -2.670E+02 |
| 3 | 3.000E+03 | 2.128E-01 | 1.988E-01 | 2.249E+00 | -5.364E+02 |

| | | | | | |
|---|---|---|---|---|---|
| 4 | 4.000E+03 | 1.557E-02 | 1.454E-02 | 8.659E+01 | -6.317E+02 |
| 5 | 5.000E+03 | 7.293E-02 | 6.813E-02 | 1.817E+00 | -8.960E+02 |
| 6 | 6.000E+03 | 1.375E-02 | 1.285E-02 | 8.499E+01 | -9.924E+02 |
| 7 | 7.000E+03 | 2.218E-02 | 2.072E-02 | 6.019E+00 | -1.251E+03 |
| 8 | 8.000E+03 | 1.340E-02 | 1.252E-02 | 8.185E+01 | -1.355E+03 |
| 9 | 9.000E+03 | 9.838E-03 | 9.191E-03 | 3.431E+01 | -1.582E+03 |

TOTAL HARMONIC DISTORTION = 2.132541E+01 PERCENT

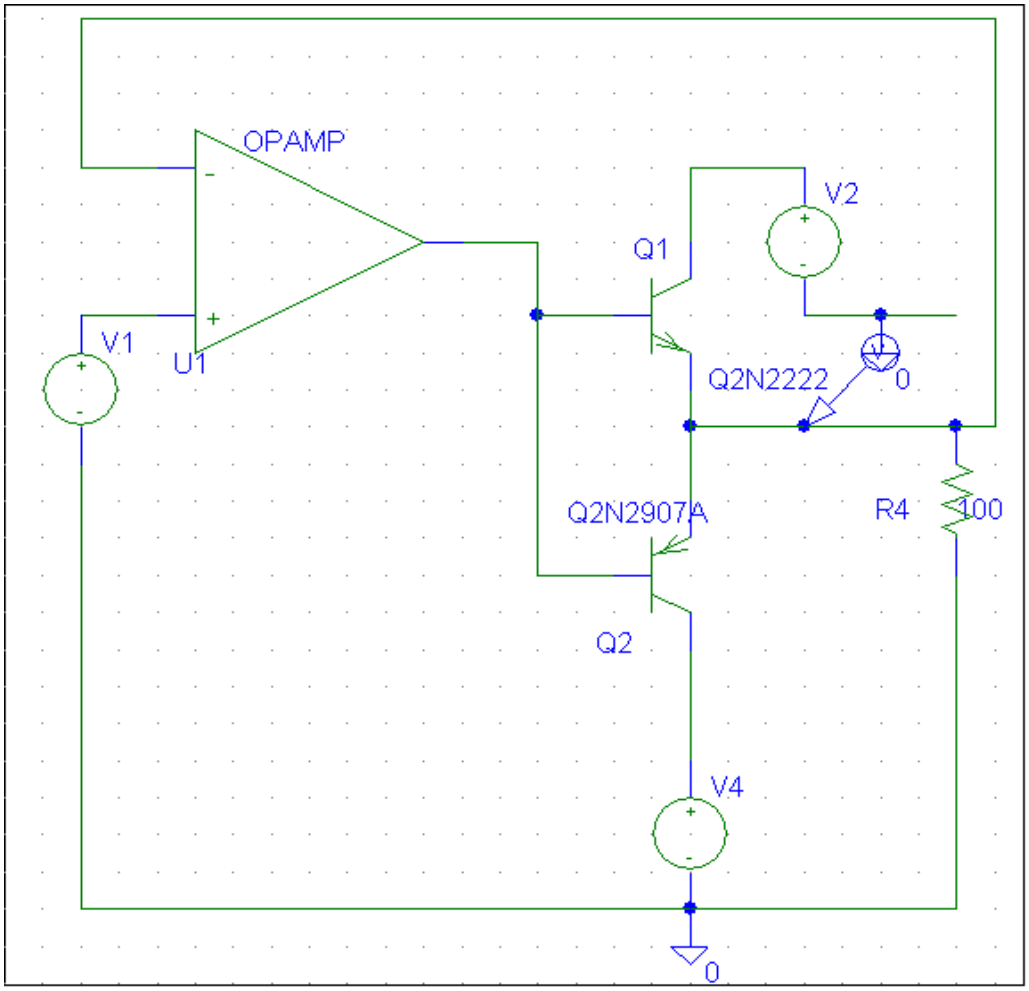
circuit in Fig.5.5(a) indicates a total harmonic distortion (THD) of of 21.32%. The principal contribution to the THD comes from the crossover distortion.

The crossover distortion can be reduced by including the class B stage in a negative feedback loop with a high gain amplifier (i.e., an operational amplifier). The circuit is shown in figure 5.6(a). The output waveform now appears as in figure 5.6(b). The Fourier analysis data shows a THD of only 0.093%.

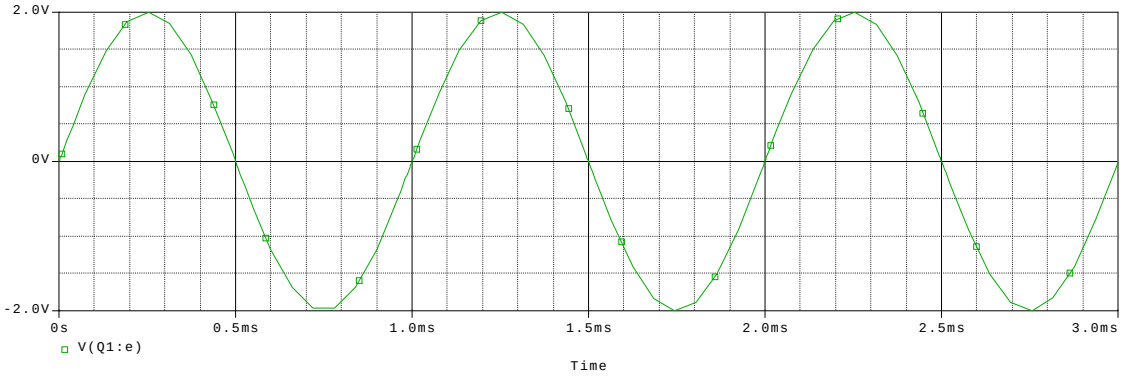
FOURIER COMPONENTS OF TRANSIENT RESPONSE V(R_R4)
DC COMPONENT = -7.467272E-05

| HARMONIC NO | FREQUENCY (HZ) | FOURIER COMPONENT | NORMALIZED COMPONENT | PHASE (DEG) | NORMALIZED PHASE (DEG) |
|---|---|---|---|---|---|
| 1 | 1.000E+03 | 1.977E+00 | 1.000E+00 | -1.800E+02 | 0.000E+00 |
| 2 | 2.000E+03 | 1.595E-04 | 8.070E-05 | 1.850E+01 | 3.784E+02 |
| 3 | 3.000E+03 | 1.154E-03 | 5.839E-04 | -1.329E+02 | 4.070E+02 |
| 4 | 4.000E+03 | 2.000E-05 | 1.012E-05 | -1.010E+01 | 7.098E+02 |
| 5 | 5.000E+03 | 9.928E-04 | 5.023E-04 | -1.613E+02 | 7.385E+02 |
| 6 | 6.000E+03 | 1.960E-05 | 9.914E-06 | -8.828E+01 | 9.915E+02 |
| 7 | 7.000E+03 | 8.112E-04 | 4.104E-04 | 1.667E+02 | 1.426E+03 |
| 8 | 8.000E+03 | 3.022E-05 | 1.529E-05 | -1.319E+02 | 1.308E+03 |
| 9 | 9.000E+03 | 6.182E-04 | 3.128E-04 | 1.272E+02 | 1.747E+03 |

TOTAL HARMONIC DISTORTION = 9.308423E-02 PERCENT




(a)




(b)

Figure 5.6: Class B output stage with reduced crossover distortion arrangement (a) the schematic, (b) the output waveform.

5.1.2.2: *Power Conversion Efficiency*

Consider the illustrations shown in Fig. 5.7. The traces in *red* corresponds to conduction by the NPN BJT and the traces in blue are due to conduction of the PNP BJT. We have ignored the crossover distortion zone (*dead-zone*) in this case. If $\hat{v}_o$ is the peak value of the output voltage $v_o$, the average signal power output is $\hat{v}_o^{\,2}/2R_L$ (ignoring the dead-zone effect). For the positive half of $v_I$, the load current comprise of half sinusoids (ignoring the dead zone) like in a half-wave rectifier (*red* traces). So the average current will be $\frac{1}{\pi}\frac{\hat{v}_o}{R_L}$ (as obtained by Fourier Series expansion). Similarly, for the negative half of

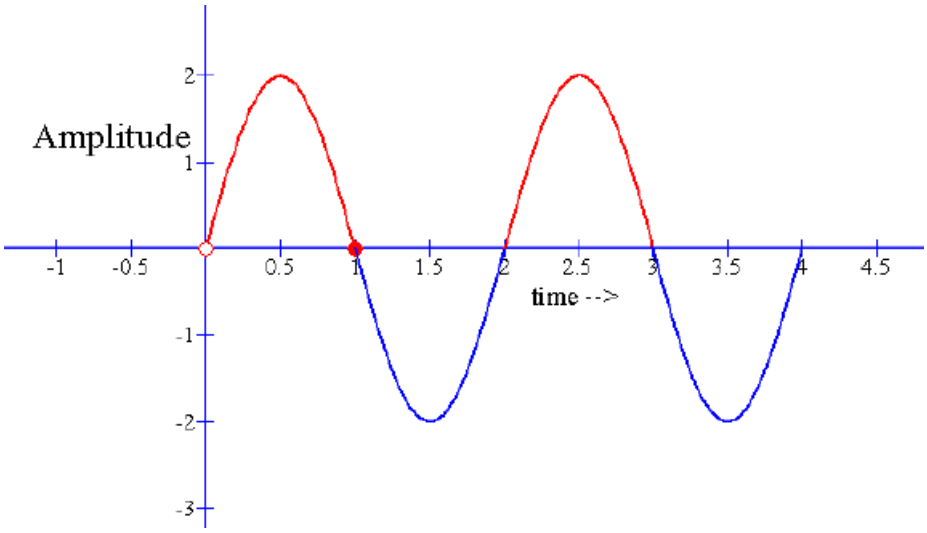



Figure 5.7: Output wave shapes in class B operation (*red* trace due to $Q_1$, and *blue* trace due to $Q_2$ ). The crossover distortion component has been assumed negligible.

$v_I$, the load current will appear as a half-wave rectified form, but all the lobes will be in the negative direction now (*blue* traces in Fig.5.7). So the average dc current in this case will be $-\frac{1}{\pi}\frac{\hat{v}_o}{R_L}$.

When $v_I$ is >0, the dc power is consumed from $+V_{CC}$ supply. So the average power consumed is: $V_{CC}\,\frac{1}{\pi}\frac{\hat{v}_o}{R_L}$. When $v_I$ is < 0, the dc power is consumed from $-V_{CC}$ supply. So the average power consumed is $(-V_{CC})(-\frac{1}{\pi}\frac{\hat{v}_o}{R_L})$.

Net average power consumed over the entire period of $v_I = 2\ V_{CC}\,\frac{1}{\pi}\frac{\hat{v}_o}{R_L}$. Then, power conversion efficiency is: (average signal power in $R_L$) / (average power consumed from the DC supply rails)

$$= (\hat{v}_o^{\,2} / 2R_L)/(2V_{CC}\hat{v}_o / \pi R_L)$$

In an ideal case (ignoring $v_{CE,sat}$, of the BJT devices), $\hat{v}_o \cong V_{CC}$. So the best case efficiency $\eta$ will be $\pi/4$,i.e., about 78.5%. Maximum average signal power available from a class B output stage is obtained by putting $\hat{v}_o \cong V_{CC}$, and is $(1/2)(V_{CC}^{\,2} / R_L)$.

*5.1.2.3: Power Dissipation in the Devices (i.e., transistors) for class B operation*

In class B stage, no power is dissipated under quiescent (no signal) condition. When a signal is applied, a certain part of the power is dissipated as heat in the device. This can be figured out as follows.

$P_D = P_{sup} - P_L$ = DC supply power – average signal power at load.

Since (for sinusoidal output signal) $P_L|_{avg} = v_o^{\,2} / 2R_L$, and $P_{sup} = 2\hat{v}_o V_{CC} / \pi R_L$,

$P_D = \frac{2}{\pi}\frac{\hat{v}_o}{R_L}V_{CC} - \frac{1}{2}\frac{\hat{v}_o^{\,2}}{R_L}$. Thus, $P_D$ depends on $v_O$ by a non-linear (i.e., quadratic) relation. So, a maximum or minimum of $P_D$ is possible, as a function of $v_o$. This can be formed, by letting $\partial P_D / \partial \hat{v}_o = 0$, and checking the sign of $\partial^2 P_D / \partial \hat{v}_o^2$. The procedure leads to an optimum value for $v_o$, $v_o|_{opt} = (2/\pi)\ V_{CC}$ for a maximum of $P_D$. Then, $P_D|_{max}$ (by substituting $v_o = (2/\pi)\ V_{CC}$) in the above expression)= $\frac{2}{\pi^2}\frac{V_{CC}^{\,2}}{R_L}$ (see Fig.5.8).

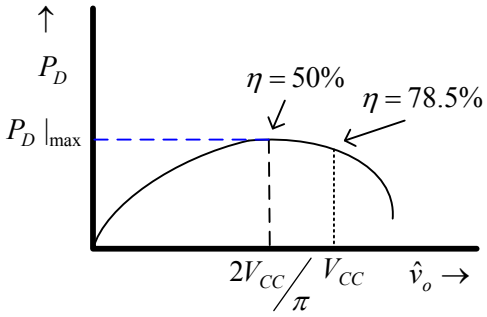



Figure 5.8: Plot of power dissipation with output voltage magnitude

One- half of this power is dissipated in each of the P-and N type BJT. So each transistor dissipates a maximum power of $P_{D|max}/2$, i.e., $\frac{1}{\pi^2}\frac{V_{CC}^{\ 2}}{R_L}$; a fact to be considered to choose proper BJT devices for the design of the output stage.

When the transistors dissipates maximum power, the efficiency drops. Thus, $\eta = \frac{\pi}{4}\frac{\hat{v}_o}{V_{CC}}|_{\hat{v}_o=\frac{2}{\pi}V_{CC}} = \frac{1}{2}$, i.e., 50% only.

*Example 5.1.2.1:* In a class B output stage we need the average output signal power to be 20W across an 8Ω load. The DC supply should be about 5V greater than the peak output voltage. Determine

(i) DC supply required.

(ii) Peak current drawn from each supply.

(iii) Total power drawn from the DC supplies.

(iv) Power conversion efficiency.

(v) Power dissipation in each transistor of the class B circuit.

*Solution/hints*: (i) $P_L = \frac{1}{2}\frac{\hat{v}_o^2}{R_L} = 20$, gives $\hat{v}_o = 17.9\,\text{V}$. Then $V_{CC} = |-V_{CC}| = 5 + 17.9 \cong 23\text{V}$.

(ii) Peak current $= \frac{17.9}{8} = 2.24$ A drawn from each supply.

(iii) Average current drawn from each supply is $\frac{\hat{i}_L}{\pi} = 0.713$ A. So average DC power drawn from the two DC supplies is $2 \times 23 \times 0.713 = 32.79$ W.

(iv) Power conversion efficiency $\eta = \dfrac{20}{32.79} \rightarrow 61\%$

(v) Power dissipation in each transistor $(32.79 - 20)/2 = 6.4\,\text{W}$. The maximum power dissipation in each transistor will be $\dfrac{V_{CC}^2}{\pi^2}\dfrac{1}{R_L} \cong 6.7\,\text{W}$

5.1.3: Class AB Operation

*5.1.3.1: Principle of operation*

In class AB operation, a small DC bias is added to the base of a complementary (i.e., PNP-NPN BJT, or PMOS-NMOS devices) pair. As a result, with input signal $v_I = 0$, a small quiescent current $I_Q$ flows. The load current $i_L$ remains = 0. Thus consider the schematic in Fig. 5.9. For $v_I = 0$, $i_L = 0$, $i_P = i_N = I_Q = I_S e^{V_{BB}/2V_T}$, where we have assumed $I_S$ for both NPN and PNP device as same. The bias voltage $V_{BB}$ is set up to produce the required $I_Q$.

When $v_I$ increases $Q_N$ conducts more since $v_{BEN}$ becomes higher than $V_{BB}/2$; similarly $Q_P$ conducts less since $v_{EBP}$, goes below $V_{BB}/2$. The difference $i_N - i_P = i_L$ flows out as load

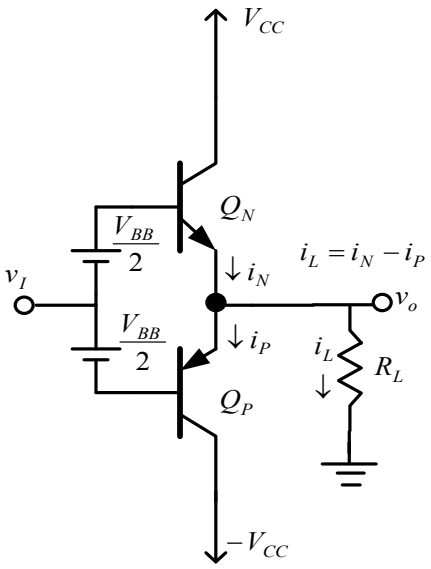



Figure 5.9: Schematic of a basic class AB output amplifier using BJT devices

current $i_L$ producing the output $v_o = i_L R_L$ , increasing in the positive direction. Specifically, $v_o = v_I + V_{BB}/2 - v_{BEN}$.

The increase in $i_N$ is accompanied by a corresponding decrease (or vice versa) in $i_P$ in accordance with the relation as derived below.

$v_{BEN} + v_{EBP} = V_{BB,}$ $i_N = I_S e^{v_{BEN}/V_T}$, $i_P = I_S e^{v_{EBP}/V_T}$ . Then,

$v_{BEN} = V_T \ln(i_N / I_S)$, $v_{EBP} = V_T \ln(i_P / I_S)$ , while from $I_Q = I_S e^{V_{BB}/2V_T}$ , we get:

$V_{BB} = 2V_T \ln(I_Q / I_S)$ . Then, $V_T \ln(i_N / I_S) + V_T \ln(i_P / I_S) = 2V_T \ln(I_Q / I_S)$ , leading to

$i_N i_P = I_Q^{\,2}$ , which holds right from the quiescent point (i.e., $v_I = 0$). The equation $i_N i_P = I_Q^{\,2}$ can be combined with $i_L = i_N - i_P$ to solve for either $i_N$ or $i_P$ in terms of $I_Q$ and $i_L$ in a quadratic equation of the form, for example, in $i_N$ (substituting $i_P = i_N - i_L$):

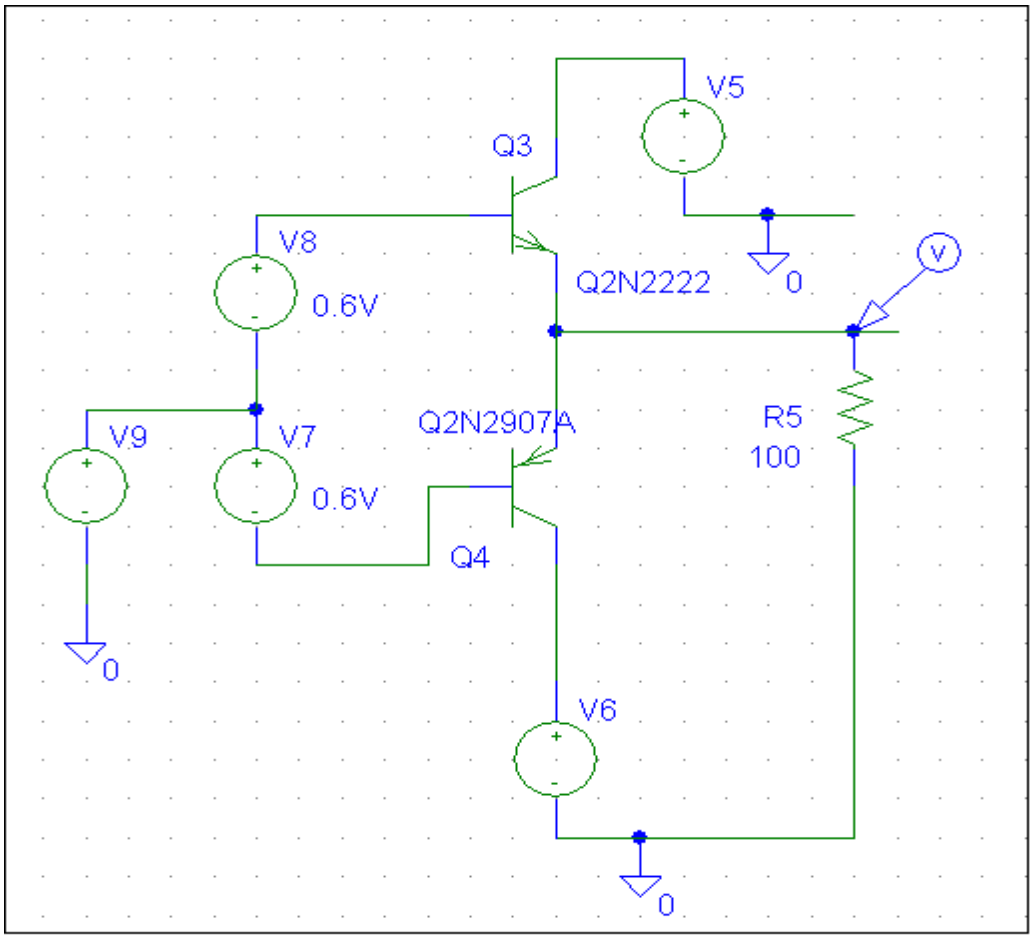
$$i_N^{\,2} - i_L i_N - I_Q^{\,2} = 0$$

When $v_I$ goes negative, $v_{EBP}$ increases, $v_{BEN}$ decreases, $i_N$ decreases, $i_P$ increases, $i_L$ reverses sign and $v_o$ decreases towards negative values thereby following $v_I$ again. This accounts for the negative going swing of $v_o$. Thus the push-pull action as in class B stage continues. Since $I_Q \neq 0$ , transition of conduction from the NMOS to PMOS occurs in a smooth manner. Cross-over distortion is thereby reduced considerably.
Figure 5.10(a) shows the PSpice schematic of a class AB output stage. Figure 5.10(b) shows the output waveform for an input signal of 1kHz with 2V amaplitude. The crossover distortion zone is considerably reduced compared with that in Fig.5.5(c) (class B output stage).

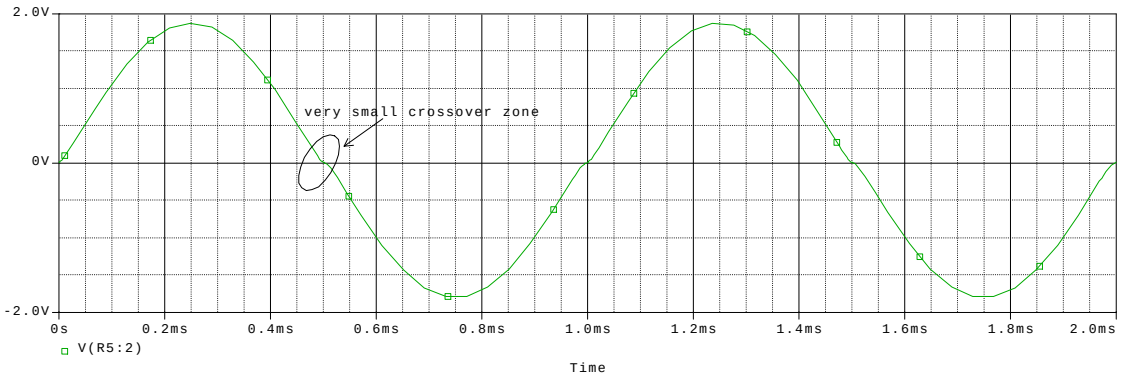
*Example 5.1.3.1:* For a class AB stage shown in figure 5.11, consider the given data: $V_{CC}$=15V; $R_L$=100Ω; $v_o$=10*Sin* ωt; the output devices $Q_P$ and $Q_N$ are matched with $I_S = 10^{-13}$ A; $h_{FE}$=50; The biasing diodes have 1/3$^{rd}$ the junction area of the output devices. Find (i) The value of required $I_{Bias}$ so that a minimum of 1mA current flows through the biasing diodes *all the time*.
(ii) The *zero signal* (i.e., quiescent) bias current through the output devices.
(iii) Quiescent power dissipation in the devices.

(iv) $V_{BB}$ for $v_o$ =0

(v) $V_{BB}$ for $v_o$=10V peak




(a)




(b)

Figure 5.10: Performance of a class AB output stage; (a) PSpice schematic, (b) output waveform for 1kHz input sinusoidal signal of 2V amplitude.

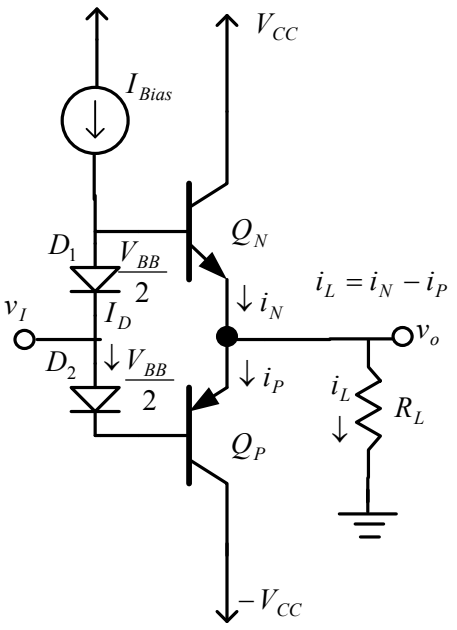



Figure 5.11 (refer *Example 5.1.3.1*)

*Solution/hints*:

(i) Since $v_o$ (peak) is 10V, $i_L$(peak)=$\hat{i}_L = 0.1\,\text{A}$.

For maximum positive swing of $v_o$, $i_N\,|_{\max} = \hat{i}_L = 0.1\,\text{A}$=100 mA.

Then $i_{BN}\,|_{\max} = {}^{100}\!/_{h_{FE}} = 2\ mA$. The current through the diode column follows the KCL equation: $I_D = I_{Bias} - i_{BN}$. Then for a minimum value of $I_D$ =1mA, we must have $I_{Bias} \geq 3\text{mA}$

(ii) Let $I_{Bias}$ =3mA. Since $Q_N$, $Q_P$ has three times the junction area relative to the biasing diodes ($D_1$,$D_2$), $I_Q$ for the output devices will be *three* times of 3mA, i.e., 9 mA.

(iii) Quiescent power dissipation is $2 \times 15 \times 9$ =270 mW.

(iv) For $v_o$ =0, $i_{BN}$ =9/50=0.18 mA. Then $I_D$=3-0.18=2.82 mA. For the diodes $I'_S = I_S/3 = 0.33 \times 10^{-14}$ mA. We now have to use the diode I-V equation

$I_D = I'_S \exp({}^{V_{BB}}\!/_{2V_T})$, with $V_T$ =25 mV (assumed since no other value is provided).

Thus, $V_{BB}$ =1.26V.

(v) For $v_o$ (peak)=10V, $i_{BN}$ =2mA, $I_D$ =1mA, $V_{BB}$ =1.21V.

In practice two diode connected transistors can be used for $D_1$, and $D_2$.

*Quiz:* What is the total DC power consumption, and hence the overall power conversion efficiency of the class AB stage in Fig. 5.11?

5.2: Different techniques for deriving the bias voltage $V_{BB}$

*5.2.1: Class AB biasing circuit using $V_{BE}$ multiplier*

Figure 5.12 shows a popular technique to derive the biasing voltage $V_{BB}$ in class AB output stage. In transistor $Q_1$, if the base current is neglected, we can see that $V_{BE1} = I_R.R_1$. Then, $V_{BB} = I_R(R_1 + R_2) = V_{BE1}(1 + \frac{R_2}{R_1})$. Hence the name $V_{BE}$-multiplier. Choosing the ratio $R_2/R_1$, any suitable $V_{BB}$ value (greater than $V_{BE1}$) can be generated.

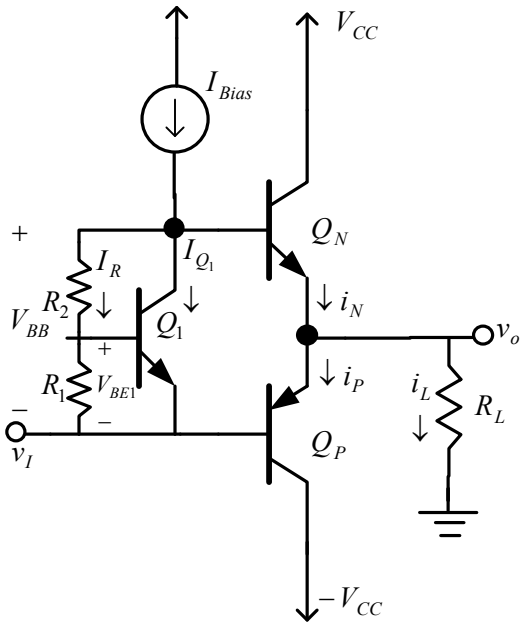



Figure 5.12: Class AB stage with $V_{BE}$ multiplier circuit.

$V_{BE1}$ is basically related to the collector current of $Q_1$. Thus, $I_{C1} = I_{S1}e^{V_{BE1}/V_T}$, where $I_{C1} = I_{Bias} - I_R$ (neglecting $i_{BN}$). Then $V_{BE1} = V_T \ln (I_{C1}/I_{S1})$. Another assumption is that during the positive half cycle or positive going swing of $v_o$, $i_{BN}$ increases and this might compete with $I_{C1}$ since $I_{Bias} = I_{C1} + I_R + i_{BN}$. Since $i_{BN}$ is very small and even large change in $I_{C1}$ may cause only little change in $V_{BE1}$ (because of exponential *I-V* relation), $V_{BE1}$ and hence $V_{BB}$ remains substantially unchanged.

*Example 5.2.1.1:* For a class AB stage shown in figure 5.12, consider the following: $V_{CC}$=15V; $R_L$=100Ω; $v_o$=10*Sin* ωt; the output devices $Q_P$ and $Q_N$ are matched with $I_S = 10^{-13}$ A; $h_{FE}$=50; In absence of any signal $I_{Q_N} = I_{Q_P} = 2$mA. The transistor $Q_1$ has $I_S$=$10^{-14}$ A. The $I_{Bias}$ has to drive a minimum of 1mA through the $V_{BE}$ multiplier circuit when the maximum input signal drive occurs producing a corresponding maximum output voltage level of 10V peak.

Provide a design for the $V_{BE}$ multiplier circuit.

*Solution/hint:* Following the case for *Example 5.1.3.1*, we see that for peak value of $v_o$ (i.e., 10V), $i_L$(peak)=$\hat{i}_L = 0.1\,\text{A} = i_N|_{\max}$.

Then $i_{BN}|_{\max} = 100/h_{FE}$ = =2 mA. Thus $I_{Bias} = I_R + I_{Q1} + i_{BN}|_{\max}$ must be $\geq 3$ mA. The 1mA current through the $V_{BE}$ multiplier circuit can be distributed as $I_R = 0.5$ mA, and $I_{Q_1} = 0.5$ mA.

With *minimum signal* drive (i.e., $v_o$=0) the entire $I_{Bias}$ of 3mA will be divided between $I_R$ and $I_{Q_1}$. We will assume the distribution as $I_R = 0.5$ mA and $I_{Q_1} = 2.5$mA.

For $v_o$=0, the condition $I_{Q_N} = I_{Q_P} = 2$mA, leads to $V_{BB} = 2V_T \ln(2\times10^{-3}/10^{-13})$=1.185V. This being the voltage drop across $R_1$,$R_2$ in series with $I_R$ =o.5 mA, we can deduce $R_1$+$R_2$ = 2.38 kΩ.

At the same time the value $I_{Q_1} = 2.5$mA provides $V_{BE1}$=$V_T \ln(2.5\times10^{-3}/10^{-14})$=0.66V.

Hence $R_1$ =0.66V/0.5mA=1.32 kΩ. Then $R_2$=1.06 kΩ.

*5.2.2: Class AB biasing circuit using complementary CC stages*

Figure 5.13 shows an arrangement where a complementary pair of common collector (CC) BJT devices are used to provide the $V_{BB}$ bias to the output transistors $Q_P$ and $Q_N$. The resistances $R_{E1}$, $R_{E2}$ ensure to stabilize the DC bias current through $Q_N$, $Q_P$ transistors. The resistances $R_1$, and $R_2$ are designed to provide the required $V_{BB}$ =$V_{E1}$-$V_{E2}$ , where $V_{E1}$ and $V_{E2}$ are dependent upon the DC bias component in $v_I$, the input signal.

*5.2.3: Class AB output stage using compound transistors*

Figures 5.14(a)-(b) show two compound transistor stages each of which is equivalent to a single transistor with an effective current gain factor equal to the product of the individual current gain factor of the constituent transistors. The arrangement in Fig.5.14(a) is also known as *Darlington* pair, while Fig.5.14(b) presents a compound PNP transistor.

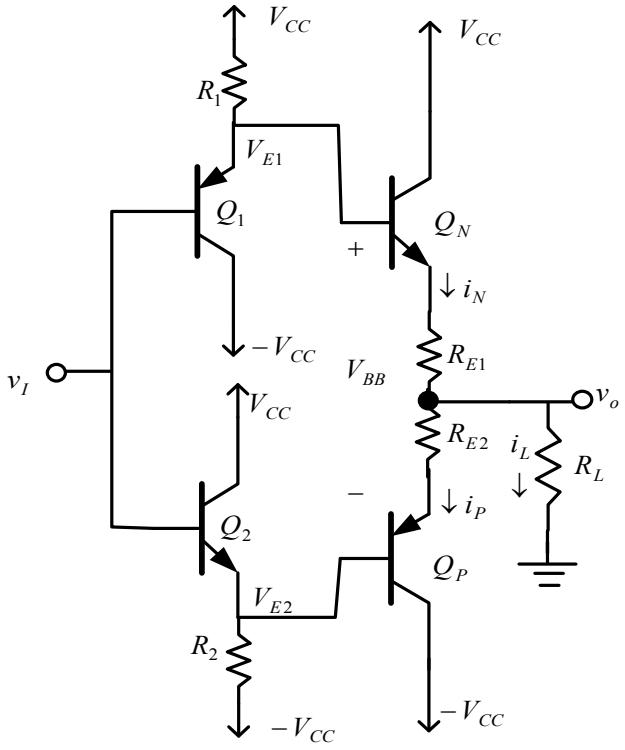



Figure 5.13: Class AB stage with $V_{BB}$ biasing by complementary CC stages

For either of the cases, the current gain factor is $h_{FE}=h_{FE1}h_{FE2}$, where $h_{FE1}$, $h_{FE2}$ are the current gain factors of $Q_1$ and $Q_2$ respectively.

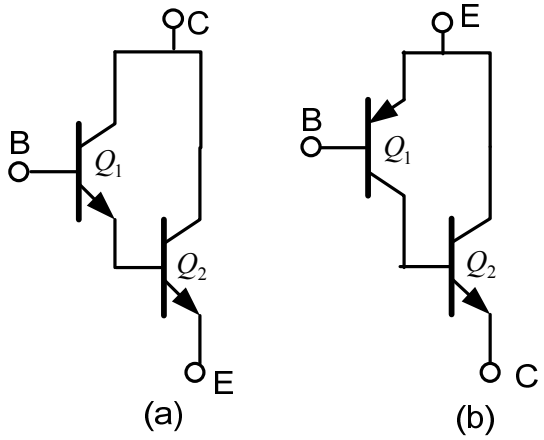


Figure 5.14:Compound transistors; (a) Darlington pair, (b) Compound PNP transistor

A class AB output stage employing the compound transistors and a $V_{BE}$ multiplier circuit is shown in figure 5.15.

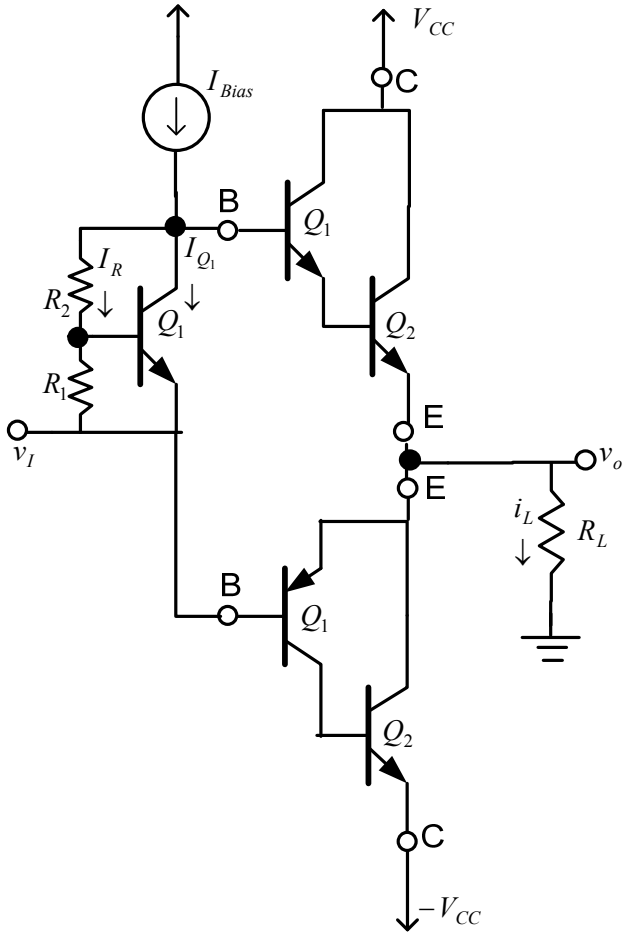



Figure 5.15 A class AB output stage with compound transistors biased by a $V_{BE}$ multiplier circuit.

## 5.3 Short Circuit Protection in Output Power Stages

Protecting the output stage from burn out because of accidental short circuit is an important concern in high output power system. Short circuit means $R_L \rightarrow 0$ by accident. A short circuit protection scheme for a class AB output stage is shown in Fig.5.16.

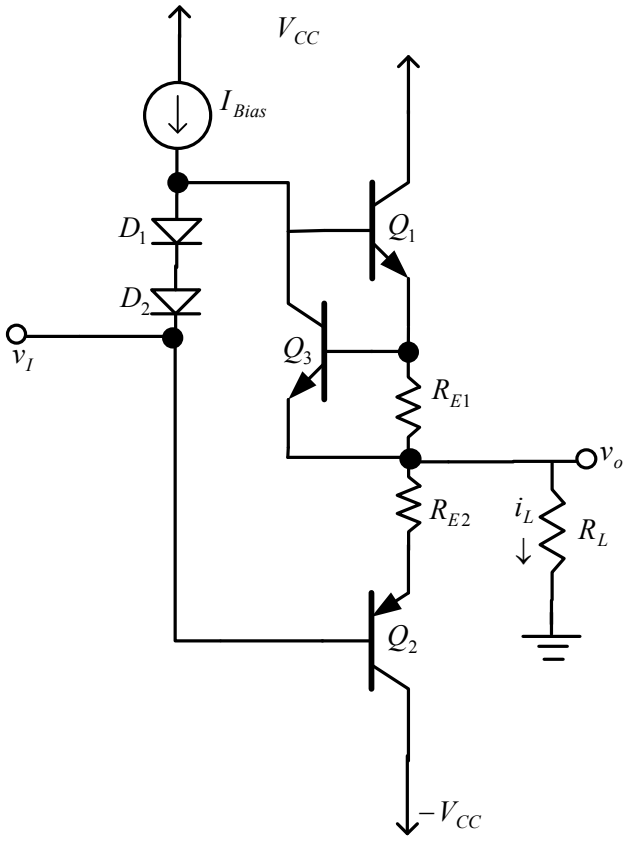



Figure 5.16: Class AB stage with short circuit protection by the transistor $Q_3$.

Basically any sudden surge of current in the output because of $R_L \rightarrow 0$, causes a drop across $R_{E1}$ (or $R_{E2}$) of such magnitude that the by-pass transistor $Q_3$ turns ON. Then $Q_3$ shunts away large part of the base bias drive current to $Q_1$. This way $Q_1$ is saved from a burn out. Note that for accidental short circuit $i_L>0$, so consideration of current in the opposite direction, i.e., protection of $Q_2$ (the PNP) transistor does not arise. The disadvantage of the protection scheme is a slight reduction in the output voltage $v_o$ because of series voltage drop in $R_{E1}$.

## 5.4: Power BJTs

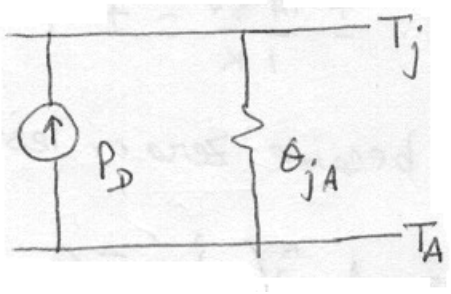
Transistors that deliver large power have to carry large amount of currents. Thus they have to be of special construction, special packaging and special mounting. Since large amount of power is dissipated in the transistor, the collector-base junction area has to be large. Such dissipation of heat increases the junction temperature. Undue rise in

temperature may damage the transistor. The wafer may fuse, the thin bonding wires may melt. Transistor manufactures specify a maximum junction temperature $T_{jmax}$ which must not be exceeded while the device is in operation. For silicon devices this range from 150 $^{o}$C to 200$^{o}$ C. BJTs fabricated with high power dissipation ability are called power BJTs. The power level range from few watts to hundreds of watts.

## 5.5 Thermal considerations

### *5.5.1: Thermal Resistance*

As the BJT junction temperature rises, heat is generated and is dissipated in the surrounding environment. This tends to lower the junction temperature. This is analogous to flow of current through a resistance trying to lower the voltage difference between the ends of the resistance. The temperature difference may be considered as a voltage difference while the power dissipated into the medium can be considered as a current. In the steady state in which the transistor is dissipating $P_D$ watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as: $T_j - T_A = \theta_{jA} P_D$, where $\theta_{jA}$ is the thermal resistance between the junction and the ambience. $\theta_{jA}$ has the unit of $^{o}$C per watt. In order that the transistor can dissipate large amount of power without raising the junction temperature above $T_{jmax}$, it is desirable to have as small value of $\theta_{jA}$ as possible. What it means that $T_j - T_A$ should be maintained constant, with $T_j \rightarrow T_{jmax}$, then $\theta_{jA} P_D \rightarrow$ constant. Hence, if $P_D$ increase, $\theta_{jA}$ must decrease. The relationship $T_j - T_A = \theta_{jA} P_D$ can be depicted by an equivalent electric network as shown in Fig.5.17.




$$T_j - T_A = P_D . \theta_{jA}$$

Figure 5.17: Equivalent circuit relating heat dissipation with rise of junction temperature

The transistor manufacturers usually specify $T_{jmax}$, the maximum power dissipation at a particular ambient temperature $T_{AO}$° C (usually 25° C) and the thermal resistance $\theta_{jA}$. These are related by $\theta_{jA} = \dfrac{T_{j\max} - T_{AO}}{P_{DO}}$.

At an ambient temperature $T_A$ higher than $T_{AO}$, the maximum allowable power dissipation $P_{Dmax}$ can be obtained from the above relation by $P_{D\max} = \dfrac{T_{j\max} - T_A}{\theta_{jA}}$.

As $T_A$ becomes close to $T_{jmax}$, $P_{Dmax}$ decreases. For $T_A < T_{AO}$, it is assumed that $P_D$ is = $P_{DO}$, a steady state value. Only when $T_A > T_{AO}$, $P_D$ degrades or derates with a slope of *minus* $\dfrac{1}{\theta_{jA}}$.

Utility of the above relationships can be understood by considering the following example.

*Example 5.5.1.1:* A BJT is specified to have a maximum power dissipation $P_{DO}$ of 2W at $T_{Ao}$=25°C, and a maximum junction temperature $T_{jmax}$ of 150°C. Find (i) the thermal resistance of the device, (ii) the maximum power that can be safely dissipated at an ambient temperature of 50°C.

*Solution:* (i) $\theta_{jA} = \dfrac{T_{j\max} - T_{Ao}}{P_{Do}} = \dfrac{150-25}{2} = 62.5\,^{o}\mathrm{C/W}$

(ii) $P_{D\max} = \dfrac{T_{j\max} - T_{Ao}}{\theta_{jA}} = \dfrac{150-50}{62.5} = 1.6\,\mathrm{W}$

*5.5.2: Transistor Case and Heat Sink*

In order to improve the heat dissipation capacity of a transistor, the transistor is encapsulated in a large area case with the collector connected to the case and the case is bolted to a large metal plate called heat sink. For high power transistors these heat sinks are also made of special structure with several fins, which increases the heat dissipating surface area without undue increase in volume. See the back of the power amplifiers, of your stereo system, for example. With all these interfaces, the equivalent thermal resistance becomes sum total of the thermal resistances of the elements. Thus, one can

express $\theta_{jA}$ as $\theta_{jA} = \theta_{jC} + \theta_{CA}$, where $\theta_{jC}$ is the thermal resistance between the junctions of the transistor and the transistor case (package), $\theta_{CA}$ is the thermal resistance between the case and the ambient. $\theta_{jC}$ can be reduced by having a large metal case for packaging the transistor. $\theta_{CA}$ can be reducing using a *heat sink,* an option at the disposal of the amplifier and the package designer.

With a heat sink, $\theta_{CA} = \theta_{CS} + \theta_{SA}$. In this $\theta_{CS,}$ is the thermal resistance between case to heat sink, and $\theta_{SA}$, is the heat sink to ambient thermal resistance. The overall electrical equivalent circuit can be modeled as shown in Fig.5.18. The power dissipation equation becomes: $T_j - T_A = P_D(\theta_{jC} + \theta_{CS} + \theta_{SA})$.

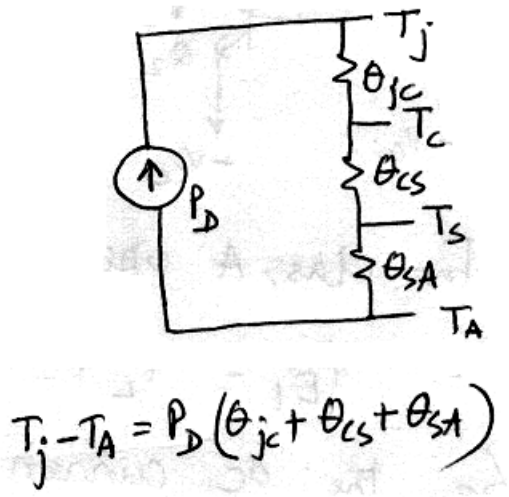
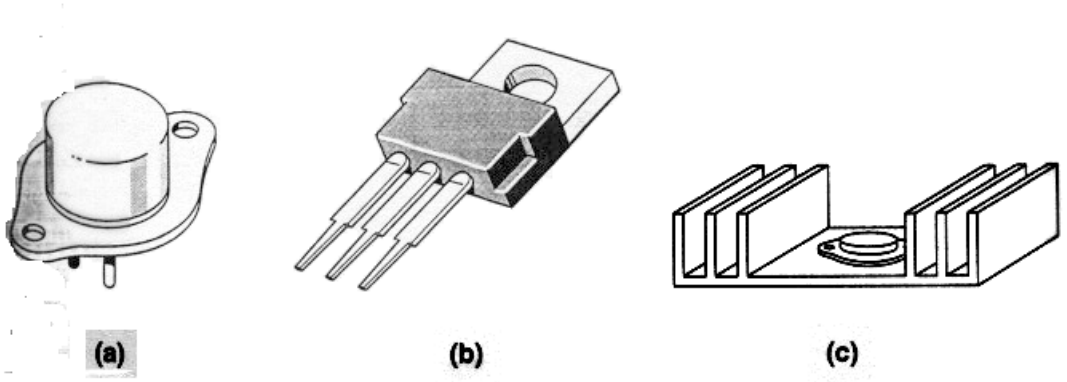



Figure 5.18: Transistor heat dissipation equivalent circuit with casing and heat sink.

It may be noted that the $\theta$'s in the above equation behave similar to conductances ,i.e., thermal resistances connected in parallel. Device manufacturers also supply $\theta_{jC}$ and a derating curve of $P_{Dmax}$ versus case temperature $T_C$. If the device case temperature $T_C$ can be maintained in the range $T_{CO} \le T_C \le T_{j\max}$, the maximum safe power dissipation is obtained when $T_j = T_{jmax}$, with $P_{D\max} = \dfrac{T_{j\max} - T_{CO}}{\theta_{jC}}$. $T_{CO}$ is usually taken as 25° C. Figure 5.19 depicts several packaging and heat sinking arrangements for high power transistors.




Two packaging schemes: (a) and (b) for power transistors and (c) typical heat

Figure 5.19: Packaging and heat sinking arrangements for power transistors; (a), (b) two different packaging technique, (c) typical heat sink arrangement.

5.6: Large and Small signal parameters for Power BJT

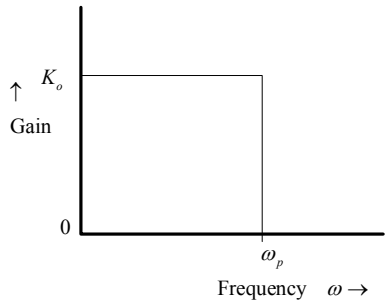
1. At high currents the constant n in the exponential I-V characteristic assume a value close to 2, i.e., $i\ i_C = I_S e^{v_{BE}/2V_T}$.
2. β is low, typically about 50, but could be as low as 5. It must be remembered that β has a positive temperature coefficient.
3. At high currents $r_\pi$ becomes very small and hence the base material resistance $r_x$ assumes a dominant role.
4. The short circuit current gain transition frequency $f_T$ is low (few MHz only), $C_\mu$ becomes large (hundreds of pF) and $C_\pi$ is even larger.
5. $I_{CBO}$ is large (few tens of micro amps.) and doubles every $10^oC$ rise in temperature.
6. $BV_{CEO}$ is typically 50 to 100 V, but it can be as high as 500V.
7. $I_{Cmax}$ is typically in the ampere range, but can become as high as 100A.

# Chapter 6

ELECTRONIC FILTERS, TUNED AMPLIFIERS and OSCILLATORS

## 6.1 Filter types, characteristics, parameters[1]

An electronic filter is a system which transmit signals in a specified frequency band to pass through with very little loss, while signals at some other frequency bands are severely attenuated through the system. An ideal low-pass filter will have a brick-wall type of transmission characteristics




Thus, the gain is constant over the frequency range $0 < w < w_p$ and the gain abruptly reduces to zero at $w = w_p$. The frequency range $0 \rightarrow w_p$ is called the pass-band, the frequency $w_p$ is called the pass-band edge frequency. The band $w > w_p$ of frequencies is known as the stop- band.

When the pass-band is $0 < w < wp$ and stop-band is $w > wp$, the filter is termed as a low-pass filter. Other types of filters are defined as follows.

| Passband | Stopband | Filter type |
|---|---|---|
| $w_p < w <$ infinite | $0 < w < w_p$ | High- pass |
| $w_{p1} < w < w_{p2}$ | $0 < w < w_{p1}$, $w_{p2} < w < \infty$ | Band-pass |
| $0 < w < w_{p1}$, $w_{p2} < w < \infty$ | $w_{p1} < w < w_{p2}$ | Band -stop |
| $0 < w < \infty$ | - | All- pass |

An ideal characteristic such as the brick-wall type is seldom achievable in practice. Thus the ideal characteristic is approximated by suitable mathematical function. This is known as filter approximation problem. In this approximation, the loss in the pass-band is held

[1] R. Raut and M.N.S. Swamy, *Modern Analog Filter Analysis and Design, A Practical Approach* , WILEY-VCH, ISBN 978-3-527-40766-8, © 2010.

to below an worst case limit $A_{max}$ (or $A_p$), while the loss in the stop-band is held above an worst case minimum limit $A_{min}$ (or $A_a$ ). *These losses are measured in decibels (db).*

The band of frequencies over which the loss changes gradually from $A_p$ to $A_a$ is known as the transition band. Narrower this transition band is, sharper is the gain characteristics of the filter and closer it is to ideal brick-wall characteristics. But more complex and expensive it becomes to realize such near ideal filters in practice.

Before implementing a filter, one must know at least the following four parameters:

$A_p = A_{max}$ → maximum loss (in decibels) in the pass- band
$A_a = A_{min}$ → minimum loss (in decibels) in the stop-band
$w_p$ = pass-band edge (i.e. frequency after which the loss becomes > $A_{max}$)
$w_a$ = stop-band edge (frequency where the loss > $A_{min}$)

## 6.2 Transfer function, poles, zeros

The filter transfer function is the ratio of an output quantity to an input quantity. Both of these will, in general, be functions of frequency. There can be four different kinds of transfer functions such as:

$V_o/V_i$ (voltage gain), $V_o/I_i$ (trans-impedance gain), $I_o/I_i$ (current gain), and $I_o/V_i$ (trans-conductance gain) functions.

In majority of the cases we shall assume the voltage gain function as the desired transfer function. Since these are functions of frequency one can readily write:

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{a_M(s-z_1)(s-z_2)...(s-z_M)}{(s-p_1)(s-p_2)...(s-p_N)}, \quad s = j\omega, \quad \omega = \text{ radian frequency.}$$

At the frequencies s = jw = $z_1$, $z_2$,….|T(s)| becomes = 0. So $z_1$, $z_2$…. are called transmission zeros.

At the frequencies s = jw = $p_1$, $p_2$,….|T(s)| becomes = infinite. So $p_1$, $p_2$…. are called transmission poles or simply, the poles of the transfer function.

If no transmission zeros are cited for finite values of the frequency w, it is assumed that the transmission zeros are located at infinity (i.e. for w → infinity). When all the

transmission zeros are at infinity, the transfer function is known as an all- pole transfer function. Then

$$T(s)=\frac{V_o(s)}{V_i(s)}=\frac{a_M}{(s-p_1)(s-p_2)...(s-p_N)},\quad s=j\omega,\quad \omega=\text{ radian frequency.}$$

## 6.3 Maximally Flat, Butterworth and Chebyshev Filter functions

Classically, it has been the practice to define a given filter response characteristics in terms of an associated low pass filter with a pass-band edge at $w_p$ =1 rad/sec. This reference filter is called the *normalized* low-pass filter. The actual filter transfer function can be obtained from this normalized low pass function by appropriately scaling the frequency variable 's' or by transforming the frequency variable 's' to other frequency function.

For an all- pole filter function, two types of approximating functions are principally used to define the normalized low-pass function. These are:

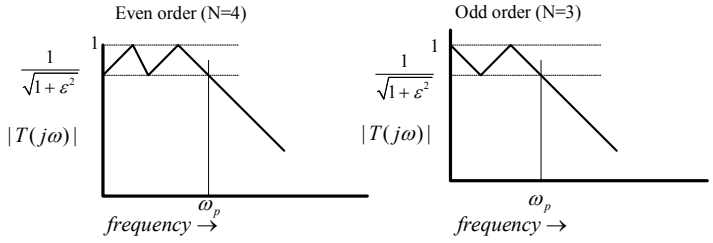
1) *Maximally flat magnitude approximation*: In this function, the response is a continuous curve beginning at w = 0 and passes through a loss of $A_{max}$ at w = $w_p$. The functional form for a filter of order N (i.e., N number of poles) is:

$$|T(j\omega)|=\frac{1}{\sqrt{1+\varepsilon^2(\frac{\omega}{\omega_p})^{2N}}}$$

When ε = 1, the loss at w = $w_p$ is $20\log\frac{1}{\sqrt{1+1}}=-3$ (db). For this special case the filter approximation is known as Butterworth approximation and the filter satisfying this characteristic is called a Butterworth filter. This is an all-pole filter function. In general, for maximally flat magnitude approximation

$$A_{\max}=A_p=20\log\sqrt{1+\varepsilon^2},\quad A_{\min}=A_a=20\log\sqrt{1+\varepsilon^2(\frac{\omega_a}{\omega_p})^2}$$

2) *Chebyshev magnitude approximation*: In this, the response has sinusoidal ripples in the passband 0 < w < $w_p$, but it rolls off monotonically after w > $w_p$. The loss in the pass-band is known as *loss- ripple*. Graphically, the characteristic appears as shown below.



## 6.4 First order functions

The order of the filter is represented by the degree of the denominator polynomial D(s) in the transfer function $T(s) = N(s)/D(s)$ .Thus a first order transfer function can be given by $T_1(s) = \frac{A_o}{s+\omega_o}, \quad T_2(s) = \frac{a_1 s + a_o}{b_1 s + \omega_o}$ , and so on. The function $T_1(s)$ is an all-pole function with a gain of $A_o/w_o$ at dc (i.e. w = 0), a pole at w = $w_o$ and represents a low -pass characteristic.The Second function $T_2(s)$ is a bilinear first order function since both the numerator N(s) and denominator D(s) have first order (i.e., exponent of 's' is unity) terms in the complex frequency 's'. This function has a pole at $\omega_p = \omega_o / b_1$ , a zero at $\omega_z = a_o / a_1$ , a low frequency (w = 0, s = 0) gain of $a_o/w_o$ and a high frequency (i.e., $\omega \to \infty$ ) gain of $a_1/b_1$.

*Further reading suggestion* (Sedra and Smith's book, 5th edn. p.1098-1100, 6th edn. p. 1271-1273).

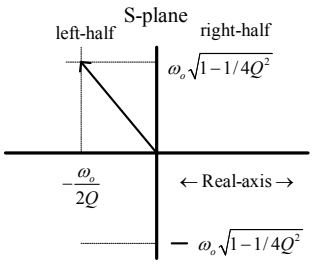
A general second order transfer function is given by:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_o}{s^2 + (\omega_o / Q)s + \omega_o^2}$$

Since both the numerator and denominator contain second order terms in 's', this function is also known as a bi-qudratic (biquad) transfer function. The numerator function decide the type of the filter i.e., for $a_2$, $a_1$ = 0, T(s) becomes a low- pass filter. The denominator determines the pole frequency $w_o$ and the frequency selectivity (i.e., narrowness of the transition band of the filter) in terms of $w_o$ and Q. Q is called the pole-Q (pole quantity factor). The two poles of T(s) (i.e. zeros of D(s), D(s) = 0)) are given by:

$$p_1, p_2 = -\omega_o / 2Q \pm j\omega_o \sqrt{1 - 1/4Q^2}$$

A graphical plot reveals that for Q > 0.5, the poles become complex conjugate pair in the two dimensional (Re- and Im- axes) s-plane. This implies frequency selectivity. $-w_o/2Q$ is the real part of the poles. When Q is high, the real part becomes smaller, the poles become closer to the jw axis – this implies higher frequency selectivity.



Note that the real part of the poles is negative. If the real part becomes > 0 (i.e. equivalently Q < 0), the poles move to the right-half of the complex S- plane. This implies a response that grows with time (← from inverse Laplace transform on S, producing terms of the form $e^{\alpha t}$) This represents an unstable system. In filter design this situation must be avoided.

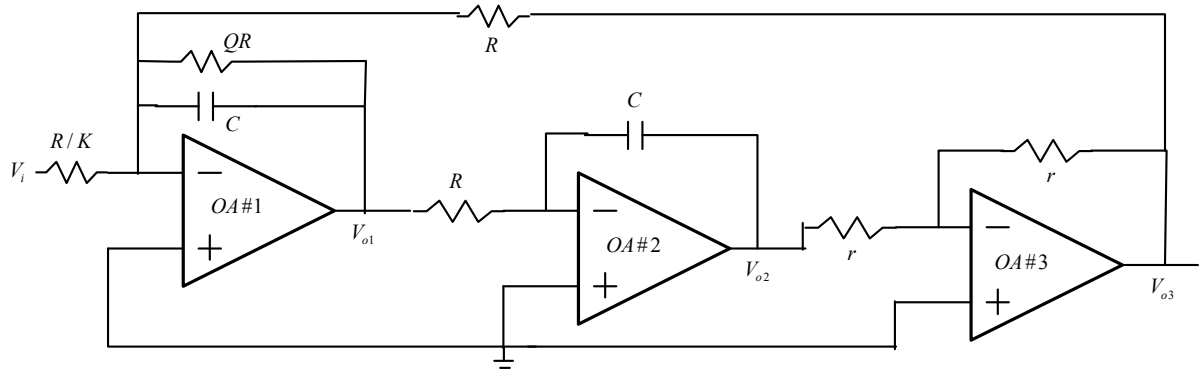
## 6.5 Standard Biqudratic filter functions

Seven possible types of second order filter can be defined for special values of the numerator coefficients. These are (i) Low-pass, (ii) High-pass, (iii) Band-pass, (iv) All-pass, (v) Low-pass notch, (vi) High-pass notch, and (vii) Notch filters.

*Further reading suggestion* (Sedra and Smith's book, 5th edn. p.1103-1105, 6th edn. 1276-1278).

### 6.5.1 Analysis of a typical second order filter network

Consider the network below, which uses three operational amplifiers (as VCVS elements). Two of the OP-AMPs are connected as integrators and one as an inverting amplifier. This is known as Tow-Thomas filter network (after the inventor's names) .




The OA#2 is an integrator with only one input. We can readily write: $V_{o2} = -V_{o1}/sCR$ .

Similarly, for OA#3, $V_{o3} = -\frac{r}{r}V_{o2} = -V_{o2}$. For OA#1, if one inspects carefully, it is possible to figure out that this stage is functioning as an integrator with several inputs. These inputs are from $V_i$, $V_{o1}$, and $V_{03}$. Then we can write:

$$V_{o1} = -V_i \frac{1}{sC(R/K)} - V_{o1}\frac{1}{sCQR} - V_{o3}\frac{1}{sCR}$$

On substituting for $V_{o2}$ and $V_{o3}$, $V_{o1} = -V_i \frac{K}{sCR} - V_{o1} \frac{1}{sCQR} - \frac{1}{sCR}(V_{o1} \frac{1}{sCR})$. Simplifying and changing sides, we get: $V_{o1}[1 + \frac{1}{sCQR} + \frac{1}{(sCR)^2}] = -\frac{KV_i}{sCR}$. On further simplification, we can get the voltage transfer function $T(s) = \frac{V_{o1}(s)}{V_i(s)} = -K \frac{s/CR}{s^2 + s/QCR + (1/CR)^2} \rightarrow H_{BP} \frac{s(\omega_o / Q)}{s^2 + s(\omega_o / Q) + \omega_o^2}$.

The above represents a band-pass filter function. Thus, if we let s = jw, w → 0, 1/CR and infinity successively, the magnitude | *T(s)* | becomes, respectively, zero, QK and zero. This response is that of a band pass filter.

If we calculate $V_{o3}$ / $V_i$, it will show a low-pass filter characteristic.

*Design Example*: Consider the design case for a second order band-pass filter with $f_o$=1 kHz, Q=5. Use *C* in microfarads range.

### 6.6 Tuned Amplifiers

Tuned amplifiers are amplifiers with a tuned circuit as its load. The tuned circuit is realized from a band-pass filter network. For high frequency application this is comprised of parallel LC elements.. The reason is that with small values (and hence small sizes) of L, C elements, the resonant frequency $\omega_o = 1/\sqrt{LC}$ can be very high i.e., 100 KHz – 100 MHz. Further the tuned load circuit does not consume any DC power.

The response of a tuned amplifier resembles a band-pass characteristic. The parallel L, C network imparts this band-pass filter characteristic. By virtue of amplification, one can achieve a band pass filtering function with enhancement of power in the desired signal frequency band.

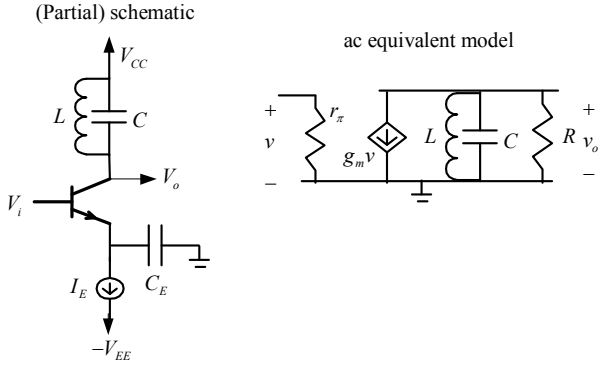
In studying tuned amplifiers, we shall assume that in the frequency range of tuning, the amplifying device (i.e. the BJT on MOS) is operating in the mind-band range. Thus the device ac equivalent circuit is purely resistive with a linear controlled source. Then, the voltage gain is given by the simple formula like $-g_m Z_L$ where $g_m$ is the transconductance of the device and $Z_L$ is the impedance of the tuned circuit load.

There are few special terms associated with a tuned amplifier. These are

a) Center frequency $w_o$ i.e. frequency at which gain vs. frequency curve shows maximum magnitude.
b) Bandwidth: B, the frequency values at which the gain is 3dB down relative to the gain at the center frequency. Quite often a selectivity factor is associated with a tuned amplifier response. This is designated by Q which is = $w_o$ /B .

c) Skirt selectivity: ratio of BW for -30 dB response to the BW for -3dB response relative to the response at $w_o$, the center frequency

*Example:* Consider a BJT CE amplifier stage with a tuned circuit as its load. The DC biasing arrangement has not been shown, but it exists in real practice.




In the equivalent circuit, R is the combination of the output resistance $r_o$ of the BJT and the resonant resistance $R_t$ of the tuned circuit. The voltage gain relative to the input signal v is $-g_m Z_L$, where $\frac{1}{Z_L} = sC + \frac{1}{sL} + \frac{1}{R} = \frac{s^2 LCR + sL + R}{sLR}$. Then, the gain function is:

$-g_m[\frac{s^2 LCR + sL + R}{sLR}]^{-1}$, which can be simplified to $T(s) = -g_m \frac{s/C}{s^2 + s/CR + 1/LC}$. This is a band-pass filter function. So the tuned amplifier will manifest a band-pass characteristic. The performance parameters are:

Center frequency $\omega_o = 1/\sqrt{LC}$, Bandwidth $B = \omega_o / Q = 1/CR$, Mid-band gain=$-g_m$R

## 6.7 Amplifier with Multiple tuned Circuits

Quite often a number of tuned circuits are need in a tuned amplifier to achieve either

a) a broader bandwidth than that of a single tuned LC network, or
b) a narrower bandwidth than that of a single LC turned circuit.

### 6.7.1 Synchronous tuning

In this, two or more tuned circuits, each having the 'same' center frequency is used. The resultant bandwidth shrinks relative to the bandwidth of either tuned circuit. For 'N' tuned circuits in the system, the overall bandwidth becomes: $B = \frac{\omega_o}{Q}\sqrt{2^{1/N} - 1} = B^{(1)}\sqrt{2^{1/N} - 1}$,

where $B^{(1)}$ is the bandwidth for a single tuned circuit. A typical schematic for a multi-tuned amplifier network is shown on p.109 (left). It is to be noted that $R_1$, $R_2$, and $R_E$ are biasing resistances, $C_{c1}$, $C_{c2}$ are coupling capacitances, and $C_E$ is the by-pass capacitance.

The two LC networks have some resonant frequency, i.e., $\omega_o = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$.

*Example:* Given $f_o$ = 10.7 MHz, two synchronous tuned stages. Overall 3 dB bandwidth is 200 kHz. L = 3μH. What will be C and R?

Use the relation $B = \frac{\omega_o}{Q}\sqrt{2^{1/N} - 1} = B^{(1)}\sqrt{2^{1/N} - 1}$, with B→200kHz, N=2, gives

$B^{(1)}$→310.83kHz. Since $f_o$=10.7MHz, $w_o = 2\pi f_o = \frac{1}{\sqrt{LC}}$. With L=3μH, C= $\frac{1}{L\omega_o^2}$ =73.7pF.

Then, since the stage bandwidth $B^{(1)} = \frac{1}{CR}$, and C=73.7pF. R=6.95 kΩ.

6.7.2. Stagger Tuned System

In this the two tuned circuits used have different center frequencies. As a result the overall response becomes more flat near the system center frequency. Consider the figure on p.113 (on left). Analysis shows that if 'B' is the system bandwidth and $w_o$ is the system center frequency, the center frequencies and BW of the constituent tuned circuit, for maximally flat band-pass response, are given by:

$$\omega_{o1} = \omega_o + \frac{B}{2\sqrt{2}}, \quad \omega_{o2} = \omega_o - \frac{B}{2\sqrt{2}}, \quad B_1 = \frac{B}{\sqrt{2}} = B_2, \quad Q_1 = \sqrt{2}\frac{\omega_o}{B} = Q_2$$

These formulae are used to determine the design of the constituent band-pass tuned circuits.

*Examples*: Sedra and Smith's book, 5th edn. p.1148-1152 Exercises :D12.35, D12.36

Sedra and Smith's book, 6th edn. p.1322-1327 Exercises :D16.35, D16.36

**6.8 Sinusoidal Oscillators**

6.8.1 Berkhausen Conditions for Oscillation

In an oscillator an amplifier is connected with a feedback network in much the same way as in negative feedback system. But the difference is that now the feedback is positive. Thus, considering the feedback system diagram, one deduces, the feedback gain

$A_f = \frac{A}{1 - A\beta} = \frac{x_o}{x_s}$.

Considering frequency dependence of A and β and letting

L(s) = A(s) β(s), the loop gain, oscillation will occur when

L(s) = 0, i.e., $A_f$→ infinite. Thus, A(s) β(s) = 1 i.e. | A($j\omega$)β($j\omega$) | = 1, and

$\mathrm{ATan}[(A(j\omega)\beta(j\omega)] = 0$.

Thus when the magnitude of the loop gain is unity and phase of loop gain is 0 degrees with positive feedback, the system will oscillate i.e. $x_o$ will be finite although $x_s = 0$.

On putting s = jw, there can be only one frequency $w = w_o$ where the network will simultaneously satisfy the two conditions . $|A(s)\beta(s)| = 1$, and $\angle A(s)\beta(s) = 0$ . These conditions are known as *Berkhausen* conditions. In this case, oscillation will occur at a single frequency $w_o$ and the wave shape will be sinusoidal. If the two conditions are not satisfied at a single frequency, there will be mixtures of frequencies in the oscillation and the oscillator wave form will be non-sinusoidal. It is convenient to assume that $|A(jw_o)| = A_m$ constant, so $\beta(w_o)$ will determine the frequency of oscillation.

6.8.2: Oscillation Amplitude Control

Attendant with the concept of infinite gain arises the question – will the amplitude of oscillation become infinite? It appears that the oscillation will grow beyond limits. But in reality no oscillator provides infinite output. The dilemma is solved by understanding that the concept of infinite gain arises under the assumption of a linear system with small signal input. As the signal level rises, the linearity assumption does not hold any more (why?, the transfer characteristic of a typical amplifier is non-linear). Thus, considering the devices that make up the amplifier, when signals are large, the operation goes into the non-linear region of the transfer characteristics. The result is a reduction in the gain which thus tends to slow down the increase in $|A\beta|$ thereby limiting it to remain close to unity. Apart from the basic amplifier additional limiter circuit or certain voltage dependent network element can be included in the feedback loop. This will facilitate $|A\beta| = 1$ when the amplitude of the signal goes up. In any case, each practical system operates with finite valued power supplies and the oscillation amplitude can never exceed these values. If it tends to do so, distortions will set in and the oscillating waveform will no longer remain sinusoidal.

6.9 Active RC Oscillators (OP-AMP Based)

*6.9.1. Wien-Bridge oscillator* ( Sedra and Smith's book, 5th edn., section 13.2, p.1171-1174; 6th edn., section 17.2, pp.1342-1344).

*Example:* Sedra and Smith's book, 5th edn. p.1174, Exercises :13.3
Sedra and Smith's book, 6th edn. p.1344, Exercises :17.3

Note that the loop gain L(s) is: $K\frac{Z_p}{Z_p + Z_s}$, where $K = 1 + \frac{R_2}{R_1}$. For oscillation, Berkhausen condition requires L(s)=1. That is $KZ_p = Z_p + Z_s$. Substituting for $Z_p$ and $Z_s$, we get:

$(K-1)\frac{R/sC}{R+1/sC} = R+1/sC.$ On simplifying, we get the quadratic equation $s^2C^2R^2 + sRC(2+1-K)+1=0$. The poles are the roots of the above equation, that is, $s_1, s_2 = \frac{-RC(3-K) \pm \sqrt{R^2C^2(3-K)^2 - 4R^2C^2}}{2R^2C^2} = \frac{K-3}{2RC} \pm \frac{1}{2RC}\sqrt{(3-K)^2-4}$. With K=1+(20.3/10)=3.03 and RC=10k.16.$10^{-9}$=16.$10^{-5}$, one can get $s_1, s_2 = \frac{.03}{32\times10^{-5}} \pm \frac{j}{16\times10^{-5}} = \frac{10^5}{16}(0.015 \pm j)$.

(a) Frequency of oscillation $\omega_o = \frac{1}{CR}$, giving $f_o$=994.718 Hz.

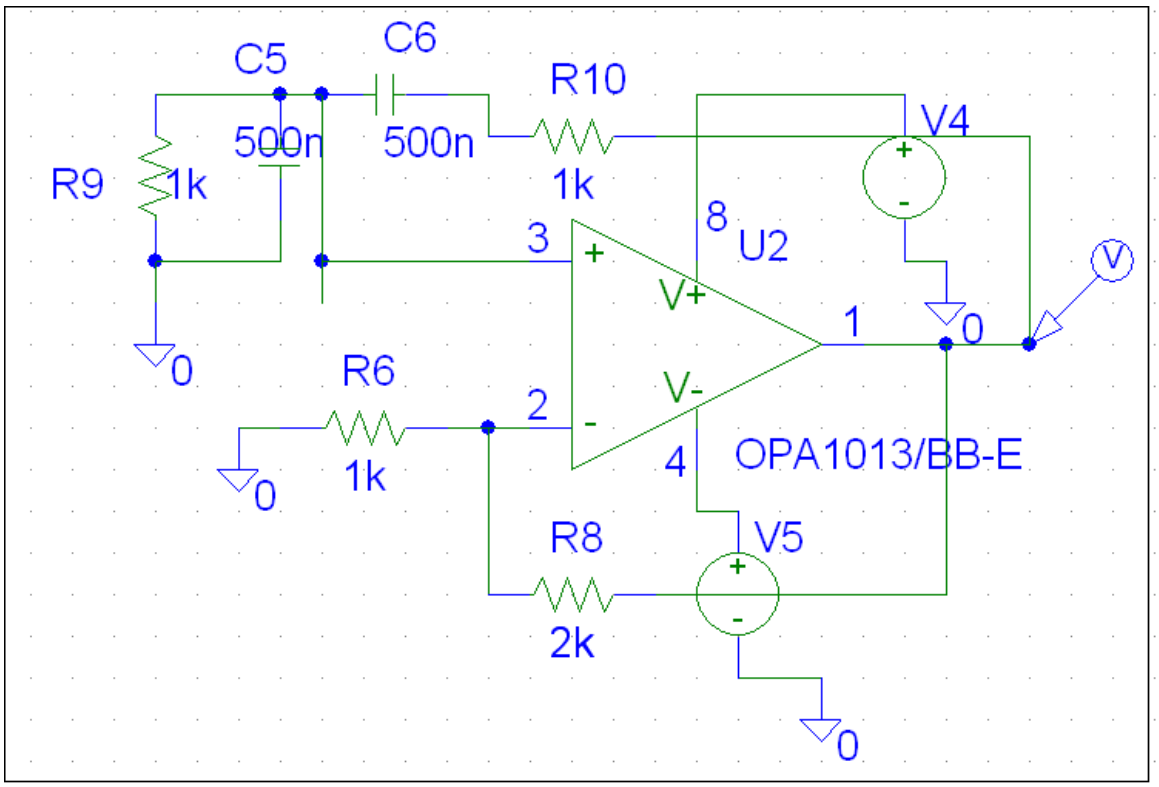
(b) At $v_a$ node, the KCL is: $\frac{v_1 - 0.7 - 15}{3K} + \frac{v_1 - 0.7 - 3.03v_1}{1K} = 0.$ This gives $v_1$=-3.36V. Then $v_o$=K$v_1$=3.03.(-3.36)V=-10.18 Volts.

(c)

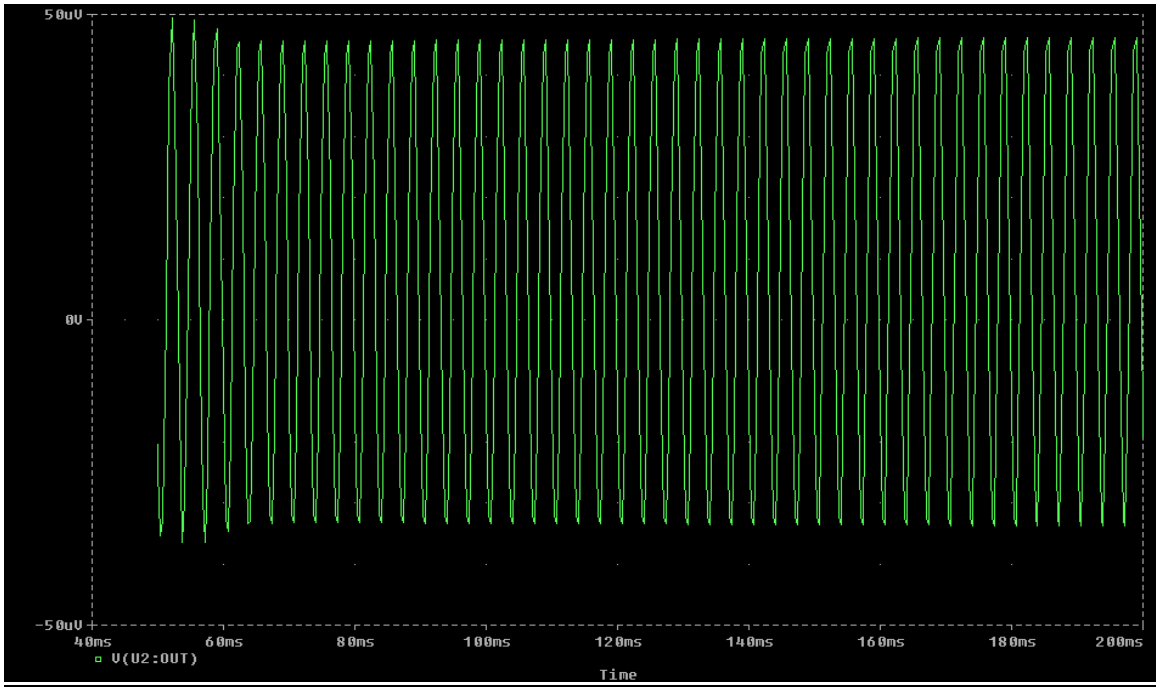
Demonstration by circuit simulation

Figure WB Osc.1(a) shows the PSpice schematic for the oscillator with an OP-AMP set for a gain of +3. Since this satisfies the condition of oscillation, oscillatory signal is generated (Fig. WB Osc. (b)) but with only a small amplitude (i.e., $\pm 50$ milli volts). This is because a gain of *K*=3 is just on the borderline of making the system unstable, i.e., oscillatory.

In figure WB Osc.2(a), the OP-AMP is arranged to provide a non-inverting gain of +3.3. The growth of oscillation from a small value (~ noise floor level) to about the DC supply

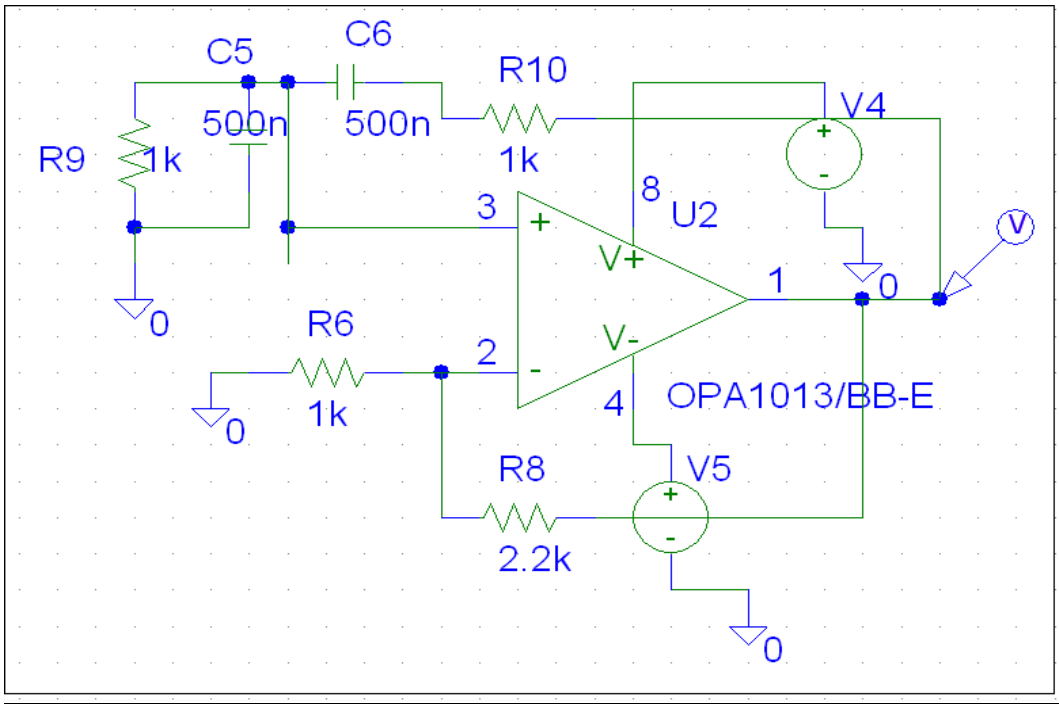



WB Osc 1(a)

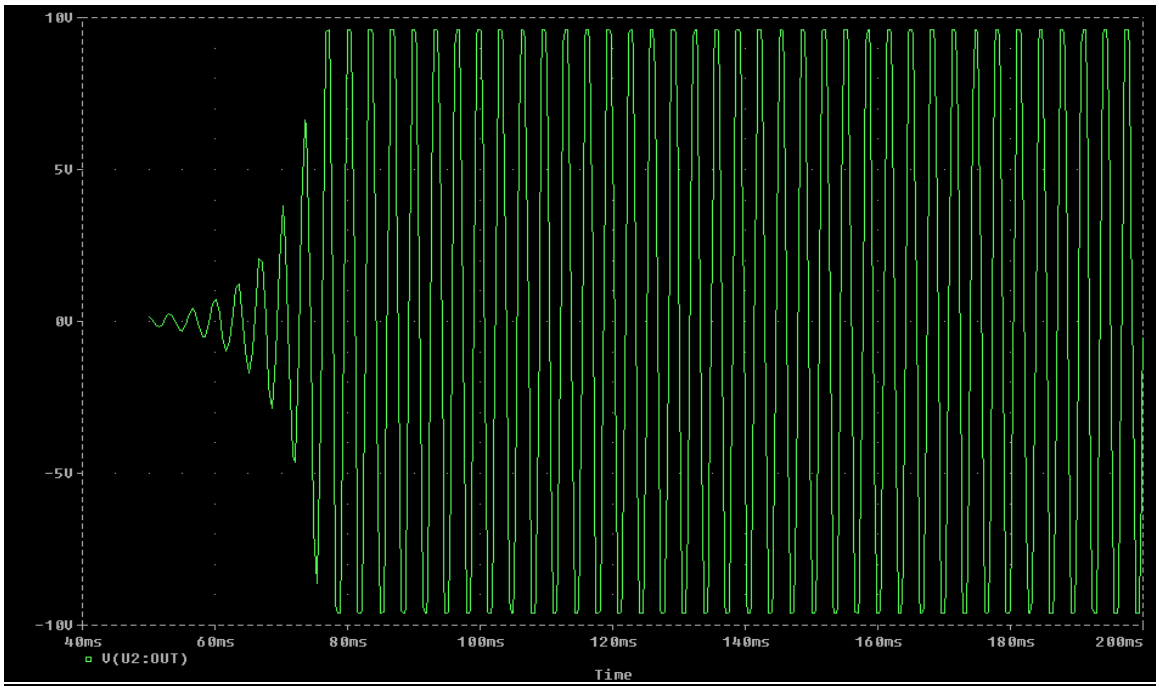



WB Osc. 1(b)

rail values of ±10 V is visible (Fig. WB Osc.2(b)).




WB Osc. 2(a)




WB Osc. 2(b)

*6.9.2. Phase Shift Oscillator*
(Sedra and Smith's book, 5th edn., section 13.2.2, p.1174-1175)
(Sedra and Smith's book, 6th edn., section 17.2.2, p.1344-1346)

The fundamental principle behind the operation of phase shift oscillator is the phase shift of $180^o$ produced by several L-sections of R,C elements followed by an inverting gain amplifier (i.e., phase shift of $180^o$) which compensates for the attenuation produced in the signal by the chain of R,C elements. Thus the loop gain magnitude becomes *unity* while the total phase shift around the loop becomes $360^o$.

Since a single L-section of R,C elements can produce a phase shift of at most $90^o$ only when the frequency is infinite, while the *infinite* frequency is of no practical significance (it is just a *mathematical* concept), it is not possible to build any practical oscillator with two L-section of R,C elements, and an inverting amplifier. In practice, a minimum of *three* L-sections of R,C elements are employed to build the simplest possible oscillator. Figure *PS Osc*.1 shows this configuration, where a VCVS (i.e., a voltage amplifier) of gain –K is used to enable the total phase shift of $360^o$ (equivalently *zero* degree) around the positive feedback loop.

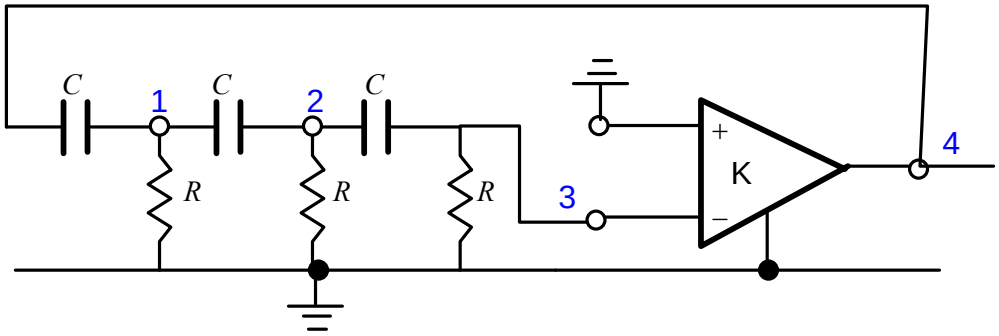



Figure: PS Osc 1

Analysis using nodal admittance matrix (NAM):

If we carefully review the results of analysis using NAM, it becomes clear that the transfer (i.e., gain) function for any of the nodal voltages (which are the objects of evaluation) has a denominator which is the determinant of the admittance matrix pertaining to the circuit on hand. For the same circuit, the denominator is fixed. From the principle of operation of an oscillator, which produces a signal without injection of any input signal (i.e., *zero* input signal), it is also understood that the voltage (or current) signal gain at any node of such system is *infinity* ,i.e., the denominator function in the gain expression as $T(s)=N(s)/D(s)$ is *zero*.

The above observation provides a straightforward method to investigate the frequency of oscillation and the gain requirement in an oscillator by using the NAM analysis technique. The method involves (i) setting up the NAM, and then (ii)equate the determinant of the admittance matrix to *zero*. Since the determinant is a function of the complex variable $s=j\omega$, equating the *real* part and the *imaginary* part of the expression of the determinant to *zero* will lead to results related to the frequency of oscillation and the required gain of the amplifier to generate and sustain an oscillation.

Considering Fig. PS Osc 1, the NAM equation can be written as (using a dummy source $I_x$ at node 1, and $G=1/R$)

$$\begin{bmatrix} 2sC+G & -sC & 0 & -sC \\ -sC & 2sC+G & -sC & 0 \\ 0 & -sC & G+sC & 0 \\ -sC & 0 & 0 & sC \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} I_X \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad \text{..PS Osc (1)}$$

It is also understood that each row (say row#1) of the NAM equation represents the KCL at that node (i.e., node#1). Further the presence of the voltage amplifier forces a *constraint equation* between the input and output nodes of the amplifier. Thus, in case of Fig. PS Osc 1, we have $V_4=-KV_3$. Incorporation of the *constraint* equation facilitates elimination of the dependent variable, which, in this case is the voltage at node 3 or at node 4. Using this information we can deduce an algorithm to re-write PS Osc (1) in a more compact form. The *algorithm* is (considering $Y_{ij}$ as the admittance element in row $i$ and column $j$) :

$$Y_{i3}|_{current} = Y_{i3}|_{old} + \mu Y_{i4}|_{old} \text{ for al } i=1,2,3,4 \text{ where } \mu = V_4/V_3 = -K \text{ (in this case).}$$

Further, since the KCL at the output node of a voltage amplifier (i.e., *ideal* VCVS) is *arbitrary*, the *row* associated with that node can be discarded from the NAM equation written in PS OSC (1). Hence, the *reduced* (in size) NAM equation becomes

$$\begin{bmatrix} 2sC+G & -sC & KsC \\ -sC & 2sC+G & -sC \\ 0 & -sC & G+sC \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_X \\ 0 \\ 0 \end{bmatrix} \qquad \text{..PS Osc (2)}$$

The determinant of the matrix is

$$G^3 - 6G\omega^2C^2 + j(5G^2\omega C - \omega^3C^3 - \omega^3C^3K),\ j=\sqrt{-1}$$

Equating the *real* and *imaginary* parts to *zero* individually, we can get $\omega = \omega_o = \dfrac{1}{\sqrt{6}RC}$ as the frequency of oscillation, and $K=29$. This is the gain required of the inverting amplifier.

Demonstration by circuit simulation

Figure PD Osc 1(a) shows the schematic of a phase shift oscillator where the inverting gain (of 30, i.e., actual gain -30) amplifier made from an OP-AMP is isolated from the

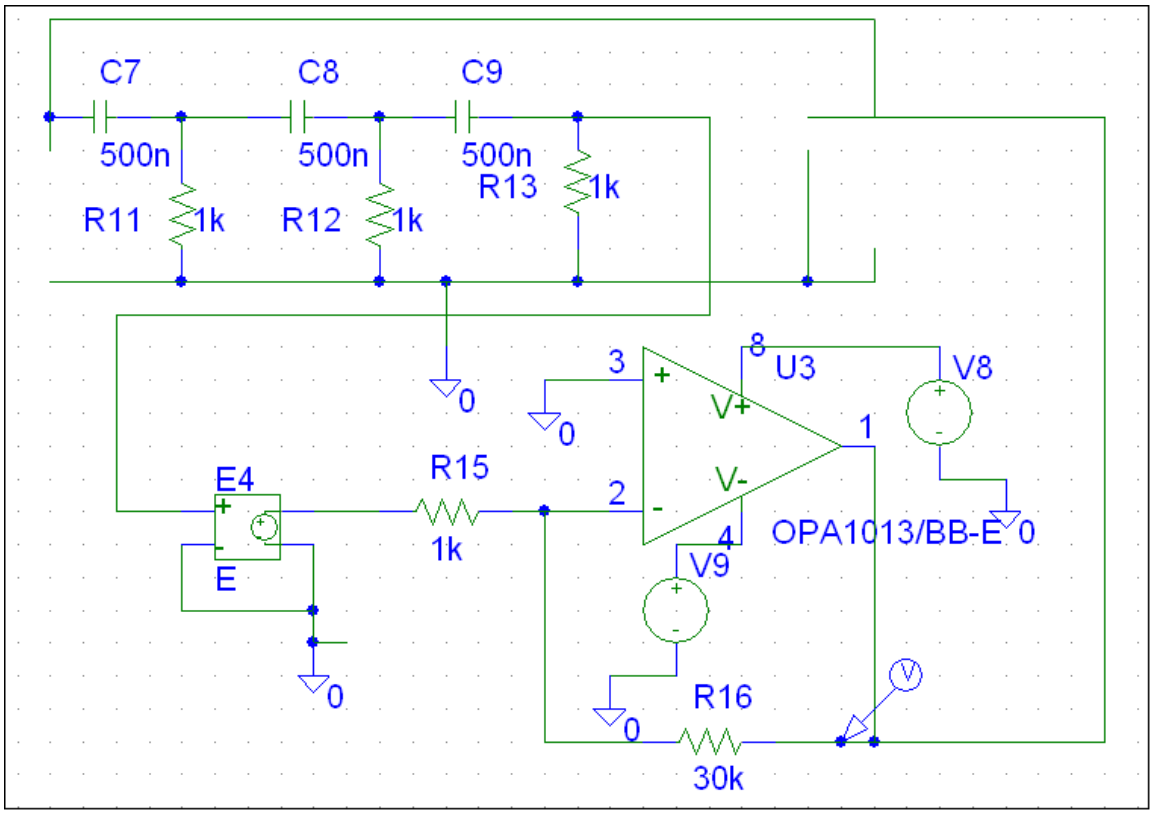



Figure: PS Osc 1(a)

R,C network by an *ideal* unity gain buffer stage. This isolation is necessary for proper validation of the theoretical analysis. Figure PS Osc 1(b) shows the gradual growth of the oscillatory signal.

Figure PS Osc 2(a) shows the circuit with an inverting gain of 33. Figure PS Osc 2(b) shows fully grown oscillation with amplitudes near the ±power supply values used for the OP-AMP.

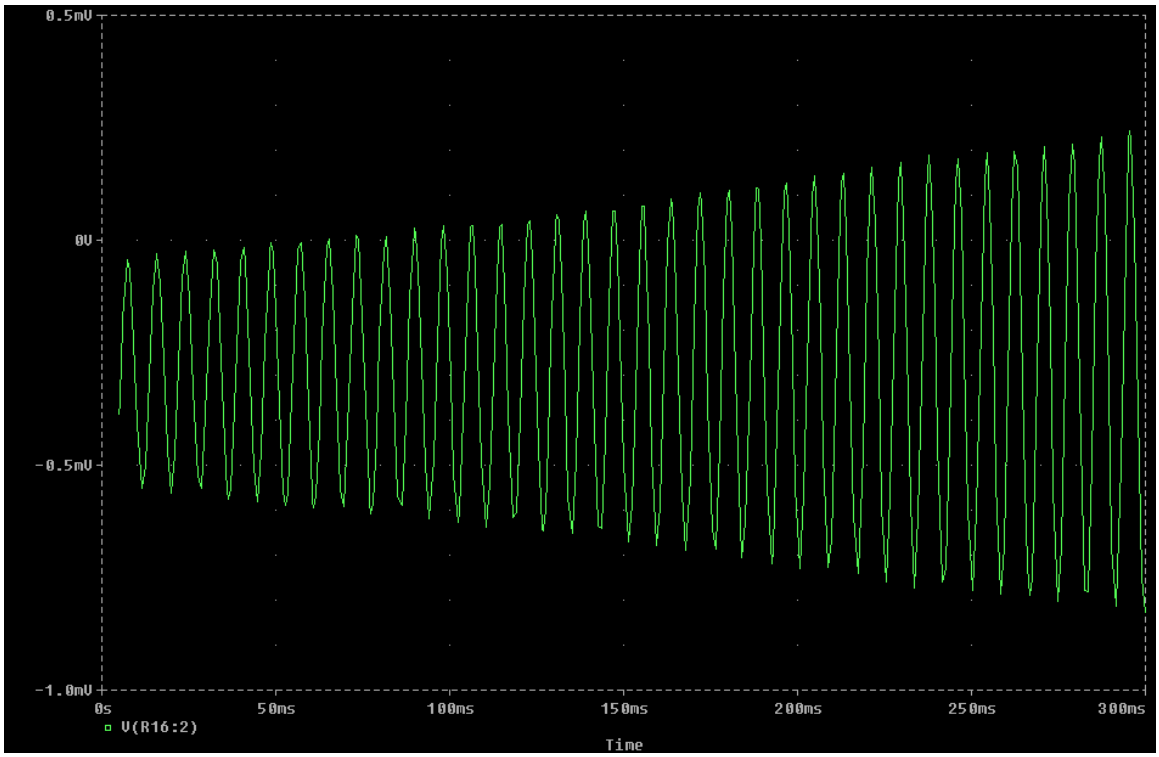



Figure PS Osc 1(b)

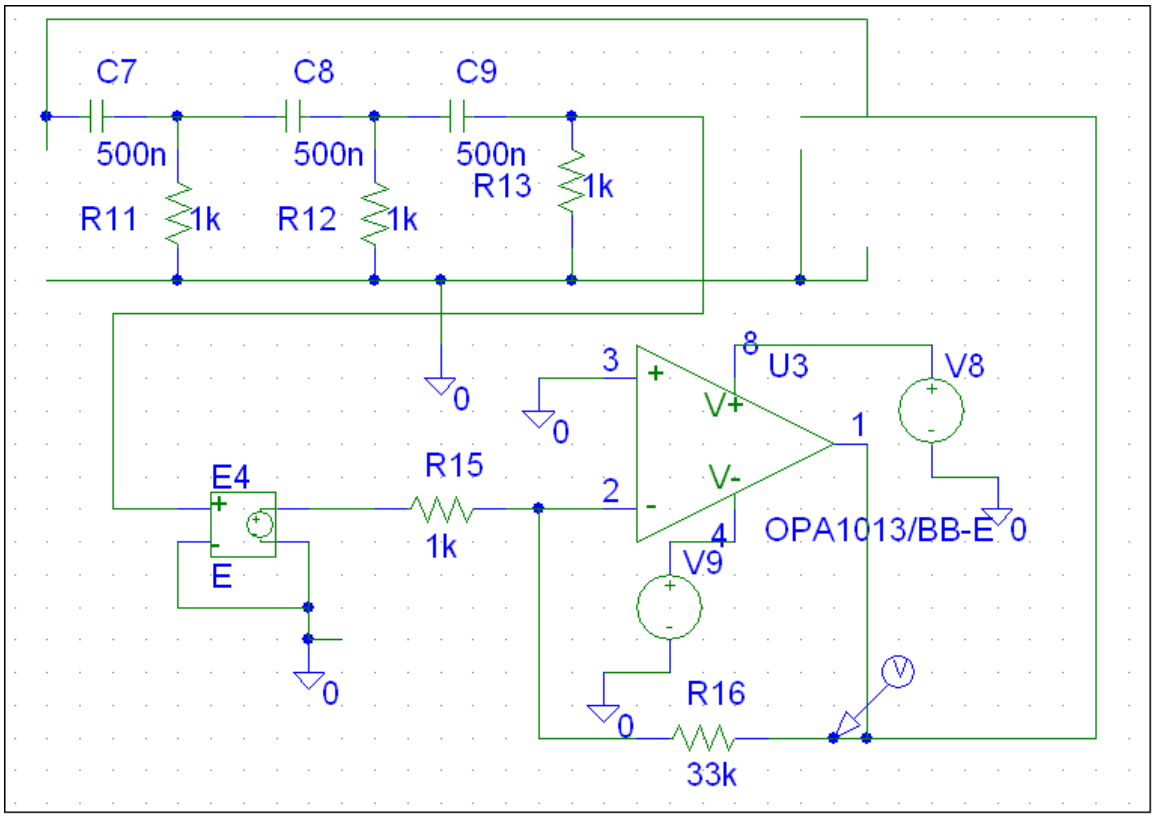



Figure PS Osc 2(a):

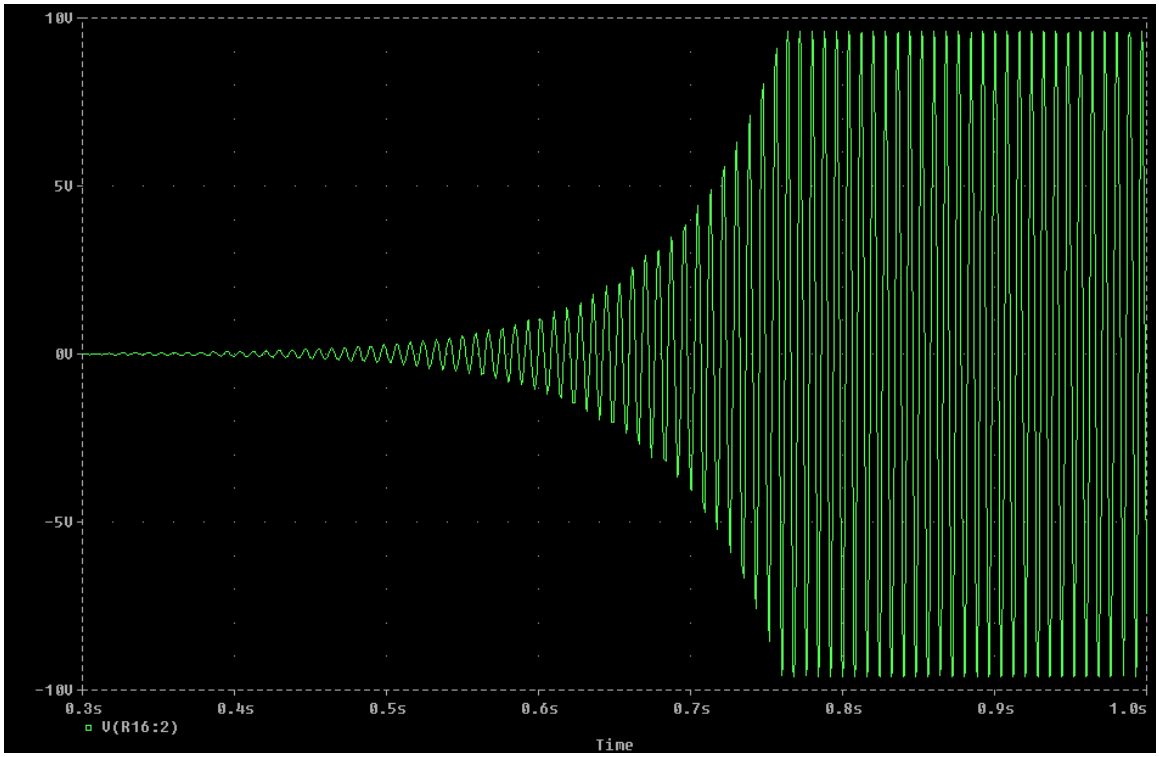



Figure PS Osc 2(b):

6.10 LC Oscillators (Hartley and Colpitts Oscillator)
(Sedra and Smith's book, 5th edn., section 13.3, p.1179-1182)
(Sedra and Smith's book, 6th edn., section 17.3, p.1349-1353)

Active R,C oscillators are efficient over a small range of frequencies (up to few kHz) especially because the active device (i.e., an OP-AMP) is severely limited in its high frequency response. At higher than few kHz, the parasitic capacitances of an OP-AMP can be included together with several resistances connected around the OP-AMP to build oscillators which are specifically known as *active R* oscillators. Oscillations in the range of few hundred kHz can be obtained from such systems, but the performance depends very much on the accuracy with which the internal characteristic of the OP-AMP is known to the designer.

For oscillators with applications in MHz to few hundred MHz frequencies, the efficient choice is a pair of reactive elements (L, C – the inductance and the capacitor, together with a wide band amplifier. The wideband amplifier can be built from one or several transistor amplifier stages.

*6.10.1 Colpitts Oscillators*

Colpitts oscillator is an L,C oscillator where the capacitor in the L,C tank circuit is split into two parts and the signal across one of the capacitors is fed back to compete the positive feedback loop. The active device is usually a single wide band transistor configured as a CE or CB BJT amplifier stage. Figures Colpit Osc 1(a)-(b) show two possible configurations using respectively a CE and a CB BJT amplifier.

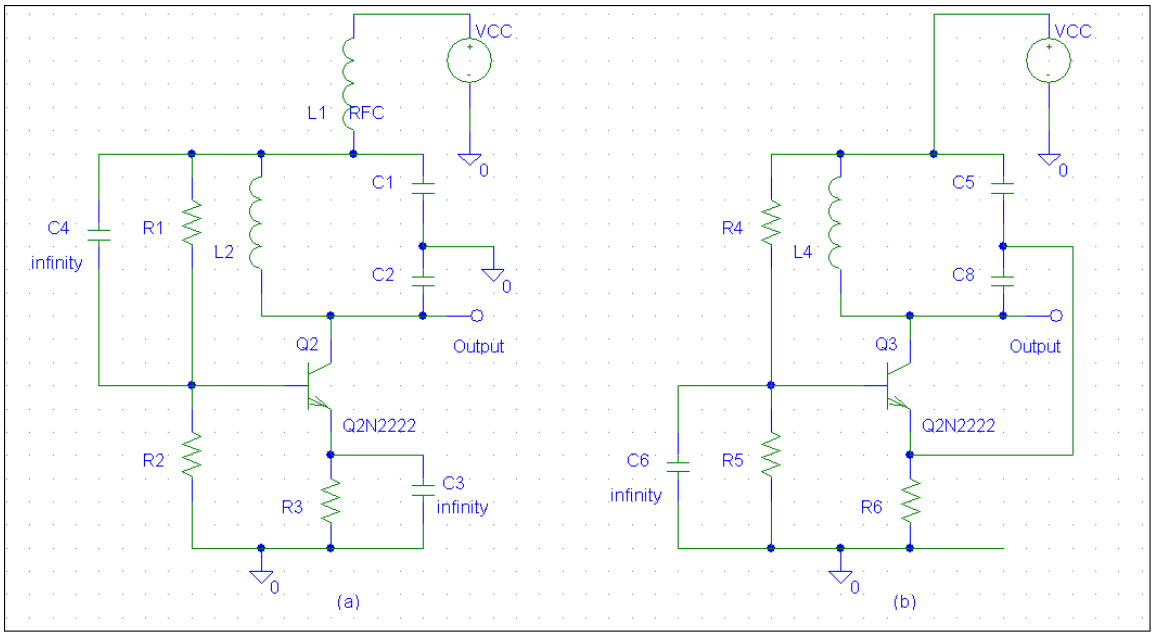



Figure Colpit Osc 1:

Analysis using nodal admittance matrix:

*6.10.1(a): Analysis for CE BJT-based Colpitts oscillator*

Consider the ac equivalent circuit, Fig. Colpit Osc 2, pertaining to the CE –Colpitts oscillator. The NAM (by inspection) equation is (with $I_X$ as a dummy source):

$$\begin{bmatrix} g_o + \frac{1}{sL_2} + sC_2 & -\frac{1}{sL_2} \\ -\frac{1}{sL_2} & sC_1 + \frac{1}{sL_2} + G_2 + g_\pi \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_X - g_m V_2 \\ 0 \end{bmatrix} \qquad \text{..Colpit Osc (1)}$$

After re-arranging the dependent source $g_m V_2$, the NAM equation becomes

$$\begin{bmatrix} g_o + \frac{1}{sL_2} + sC_2 & -\frac{1}{sL_2} + g_m \\ -\frac{1}{sL_2} & sC_1 + \frac{1}{sL_2} + G_2 + g_\pi \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_X \\ 0 \end{bmatrix} \qquad \text{..Colpit Osc (2)}$$

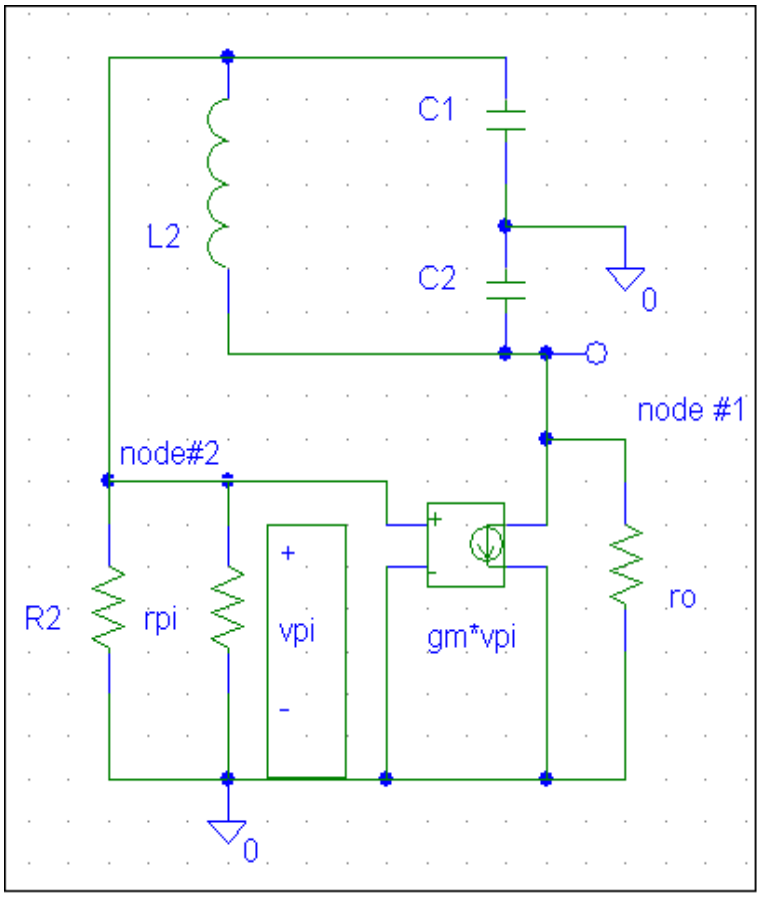



Figure Colpit Osc 2:

The determinant of the matrix is:

$$\omega[g_o G_2 L_2 + g_o g_\pi L_2 + C_1 - \omega^2 C_1 C_2 L_2 + C_2] + j[-g_o - G_2 + \omega^2 (C_2 L_2 G_2 + C_2 L_2 g_\pi + C_1 L_2 g_o) - g_\pi - g_m]$$

In the above expression $g_o = 1/r_o, G_2 = 1/R_2, g_\pi = 1/r_\pi$. The real part of the expression is $\omega[g_o G_2 L_2 + g_o g_\pi L_2 + C_1 - \omega^2 C_1 C_2 L_2 + C_2]$, while the imaginary part is $[-g_o - G_2 + \omega^2 (C_2 L_2 G_2 + C_2 L_2 g_\pi + C_1 L_2 g_o) - g_\pi - g_m]$.

The determinant of the matrix has to be *zero* for oscillations to occur. Equating the real part to *zero*, we can get the frequency of oscillation as:

$\omega = \omega_o = \sqrt{\dfrac{g_o L_2 G_2 + g_o L_2 g_\pi + C_1 + C_2}{L_2 C_1 C_2}}$ , which is (approximately) $= \sqrt{\dfrac{C_1 + C_2}{L_2 C_1 C_2}}$ , if we assume $g_o$ =0, i.e., $r_o$ = *infinity*.

Equating the imaginary part (i.e., coefficient of *j*) to *zero* and substituting $\omega=\omega_o$ will generate the design value of $g_m$ which will enable the oscillation to begin. On neglecting $g_o$ and $g_\pi$ in comparison with $g_m$, we can arrive at $g_m = \frac{C_2}{R_2 C_1}$ as a design equation (approximate) for the oscillation. This is *left as an exercise* to the student. Note that $g_m$ is related to the DC bias current in the BJT device.

*6.10.1(b): Analysis for CB BJT-based Colpitts oscillator*

Consider the ac equivalent circuit, Fig. Colpit Osc 3, pertaining to the CB –Colpitts oscillator. The NAM (by inspection) equation is (with $I_X$ as a dummy source):

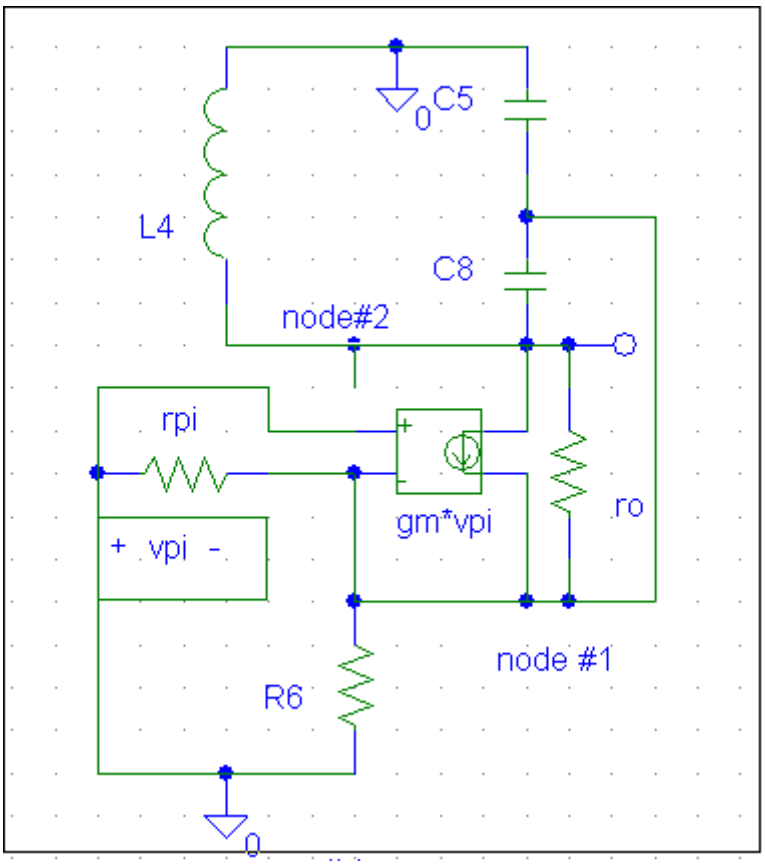



Figure Colpit Osc 3:

$$\begin{bmatrix} g_o + G_6 + g_\pi + sC_5 + sC_8 & -g_o - sC_8 \\ -g_o - sC_8 & g_o + sC_8 + \frac{1}{sL_4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_X + g_m v_\pi \\ -g_m v_\pi \end{bmatrix} \qquad \text{..Colpit Osc (3)}$$

Recognizing that $v_\pi = -V_1$, and rearranging the dependent source $g_m V_1$, the NAM equation becomes

$$\begin{bmatrix} g_o + G_6 + g_\pi + sC_5 + sC_8 + g_m & -g_o - sC_8 \\ -g_o - sC_8 - g_m & g_o + sC_8 + \dfrac{1}{sL_4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_X \\ 0 \end{bmatrix} \quad \text{..Colpit Osc (4)}$$

The determinant of the matrix is:

$$\omega[g_o g_\pi L_4 + g_o G_6 L_4 + C_8 - \omega^2 C_5 C_8 L_4 + C_5) + j[-G_6 + \omega^2 (G_6 C_8 L_4 + g_o C_5 L_4 + g_\pi C_8 L_4) - g_o - g_\pi - g_m]$$

In the above expression $g_o = 1/r_o, G_6 = 1/R_6, g_\pi = 1/r_\pi$. The determinant of the matrix has to be *zero* for oscillations to occur. The *real* part equated to *zero* gives the oscillation frequency

$\omega = \omega_o = \sqrt{\dfrac{g_\pi g_o L_4 + g_o G_6 L_4 + C_5 + C_8}{L_4 C_5 C_8}}$, which approximates to (assuming $g_o$ =0, i.e., $r_o$ = *infinity*) $\omega_o = \sqrt{\dfrac{C_5 + C_8}{L_4 C_5 C_8}}$.

The *imaginary* part equated to *zero* leads to
$-G_6 + \omega^2 (G_6 C_8 L_4 + g_o C_5 L_4 + g_\pi C_8 L_4) - g_o - g_\pi - g_m = 0$. On substitution for $\omega$=$\omega_o$, neglecting $g_o$ and $g_\pi$ in comparison with $g_m$, we can arrive at $g_m = \dfrac{C_8}{R_6 C_5}$ as a design equation (approximate) for the oscillator. Note that $g_m$ is related to the DC bias current in the BJT device.

6.11: Crystal Oscillator

(Reading suggestion: Sedra and Smith's book, 5th edn., section 13.3.2, p.1182-1184)
(Sedra and Smith's book, 6th edn., section 17.3.2, p.1353-1355)

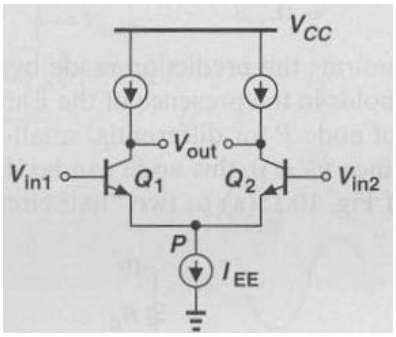
ELEC 312_Winter 2013 term

**ELEC 312: ELECTRONICS – II ASSIGNMENT** set 1

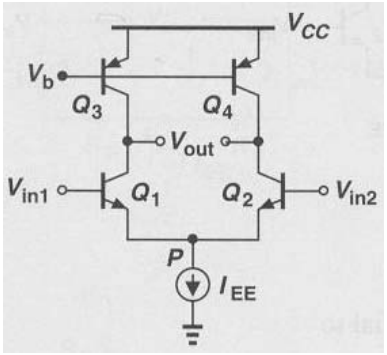
**Department of Electrical and Computer Engineering**

Winter 2013

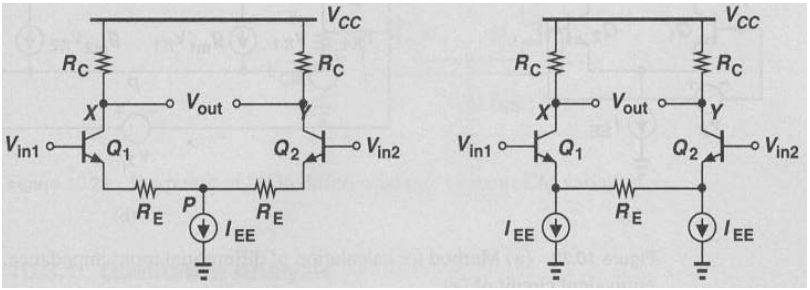
1. Find an expression for the differential gain of the following circuit, where ideal current sources are used as loads to maximize the gain. $V_{in1}$, $V_{in2}$ may be assumed to be balanced differential signals.



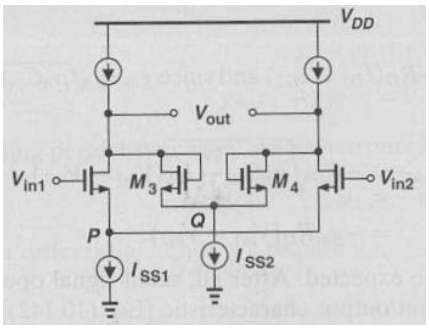

2. The following figure illustrates an implementation of a differential amplifier with active load using complementary BJT devices. Calculate the differential voltage gain $V_{out}/(V_{in1} - V_{in2})$.



3. Determine the gain of the emitter degenerated differential pairs shown in the following figure. Assume $V_A = \infty$.




4. Assuming $\lambda = 0$, compute the voltage gain of the following circuit. $I_{SS2}$ is used to bias the transistors $M_3$,$M_4$. Consider all I-sources as ideal.



5. Consider the basic current mirror in Figure 5 built with the NMOS-transistors M1, M2. For both the transistors L=0.5 microns ,W/L =8, $V_{THN}$ =0.5V, $\mu_n C_{oxn} = 300\,\mu A/V^2$ Further, $V_{DD}$=1.5V, and $I_{REF}$ =100 $\mu A$.

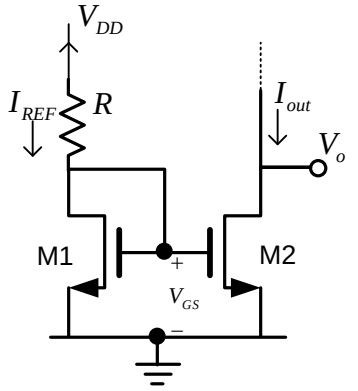



Figure 5

(i) Design *R* for $I_{out}$ =100 $\mu A$.
(ii) What is the lowest value that could be allowed for $V_o$ for proper operation of the system?
(iii) If the transistors have an *Early voltage* of 20V, what is the output resistance of the current source (i.e., at the location of $I_{out}$)?
(iv) How much (as a %) will $I_{out}$ change if $V_o$ changes by $\pm 0.5V$ ?

6. Consider the basic current mirror (Figure 6) implemented using *npn*-BJT devices (Q1,Q2). Derive an expression for the current transfer ratio $I_{out}/I_{in}$. If β of the transistors has a minimum value of 50, what will be the largest current transfer ratio?

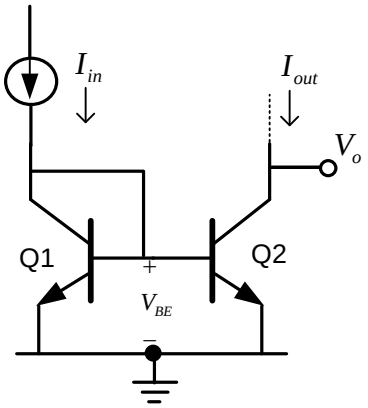


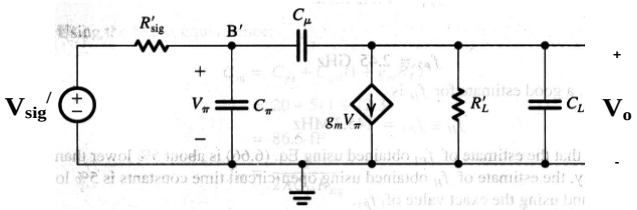

Figure 6

# ELEC 312: ELECTRONICS – II : ASSIGNMENT set-2

**Department of Electrical and Computer Engineering**

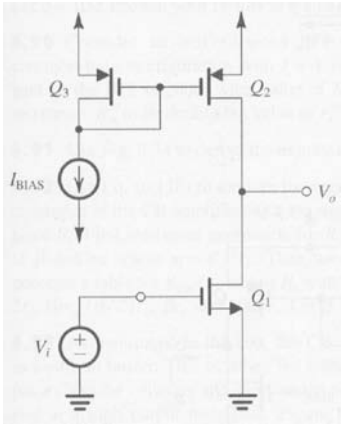
Winter 2013

1. A common-emitter amplifier that can be represented by the following equivalent circuit, has $C_\pi = 10$ pF, $C_\mu = 0.5$ pF, $C_L = 2$ pF, $g_m = 20$ mA/V, $\beta = 100$, $r_x = 200$ Ω, $R_L' = 5$ kΩ and $R_{sig} = 1$ kΩ. Find (i) the mid band gain $A_M$, (ii) the frequency of the zero $f_Z$, and (iii) the approximate values of the pole frequencies $f_{P1}$ and $f_{P2}$. Hence estimate the 3-dB frequency $f_H$. Note that $R'_{sig}$ is the equivalent Thevenin resistance looking towards the signal source and includes the effects of $R_{sig}$, $r_x$ and $r_\pi$. For approximate estimates, you may use OCTC method.




2. Analyze the high-frequency response of the CMOS amplifier shown below. The dc bias current is 100 μA. For $Q_1$, $\mu_n C_{ox} = 90$ μA/V$^2$, $V_A = 12.8$ V, W/L = 100 μm/1.6 μm, $C_{gs} = 0.2$ pF, $C_{gd} = 0.015$ pF. For $Q_2$, $C_{gd} = 0.015$ pF, $C_{gs} = 36$ fF and $|V_A| = 19.2$ V. Assume that the resistance of the input signal generator is negligibly small. Also, for simplicity assume that the signal voltage at the gate of $Q_2$ is zero. Find the low-frequency (i.e., at DC) gain, the frequency of the pole, and the frequency of the zero. You may use nodal analysis.

   *Note:* fF=$10^{-15}$ F, pF=$10^{-12}$ F.

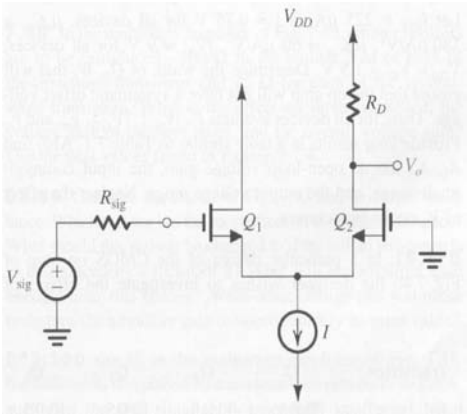



3. A CG amplifier is specified to have $C_{gs} = 2$ pF, $C_{gd} = 0.1$ pF, $C_L = 2$ pF, $g_m = 5$ mA/V, $\chi = 0.2$, $R_{sig} = 1$ kΩ and $R_L' = 20$ kΩ. Neglecting the effects of $r_o$, find the low-frequency gain $v_o/v_{sig}$, the frequencies of the poles $f_{P1}$ and $f_{P2}$ and hence an estimate of the 3-dB frequency $f_H$. For a CG amplifier you can use $g_{mb} = \chi g_m$. Use ac equivalent circuit.

4. (a) Consider a CS amplifier having $C_{gd}$ = 0.2 pF, $R_{sig}$ = $R_L$ = 20 kΩ, $g_m$ =5 mA/V, $C_{gs}$ = 2 pF, $C_L$ (including $C_{db}$) = 1 pF, and $r_o$ = 20 kΩ. Find (i) the low-frequency gain $A_M$, and (ii) estimate $f_H$ using open-circuit time constants.

   Hence determine the gain-bandwidth (GBW=mid-freq. gain *times* $f_H$).

5. Consider the following circuit for the case: I = 200 µA and $V_{OV}$ = 0.25 V, $R_{sig}$ = 200 kΩ, $R_D$ = 50 kΩ, $C_{gs}$ = $C_{gd}$ = 1 Pf (for both transistors). Find the dc (i.e., low-frequency) gain, the high-frequency poles, and an estimate of $f_H$. (hint: need to find $g_m$ from I and $V_{OV}$ data!).



6: (a) Consider a CS stage having $C_{gd}$ = 0.2 pF, $R_{sig}$ = 20 kΩ, $g_m$ =5 mA/V, $C_{gs}$ = 2 pF, and $r_o$ = 20 kΩ.

(b) A CG stage is connected in totem-pole configuration with the CS transistor in (a) to create a cascode amplifier. The ac parameters of this stage are identical with those of the CS stage. Regarding the body-effect in the CG stage assume $\chi$ = 0.2. Further $R_L$= 20 kΩ, and is shunted by a load capacitance $C_L$=1 pF.

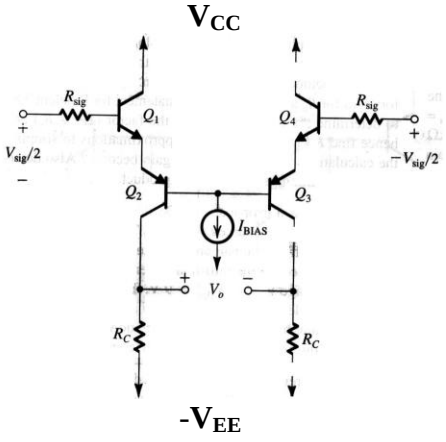
Show a schematic diagram of the system using NMOS transistors. Show the *ac* equivalent circuit.

Find (i) the low-frequency gain $A_{M,}$ and (ii) estimate the gain-bandwidth of the system. You may use OCTC method to determine the dominant high frequency pole $f_H$ of the system.

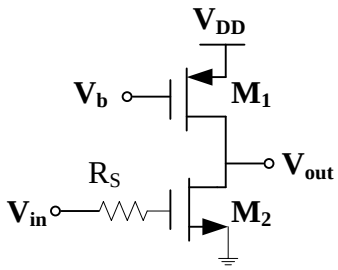
7: For the following circuit, let the bias be such that each transistor is operating at 100-$\mu A$ collector current. Let the BJTs have $h_{fe}$ = 200, $f_T$ = 600 MHz, and $C_\mu$ = 0.2 pF, and neglect $r_o$ and $r_x$. Also, $R_{sig} = R_C$ = 50 kΩ.

Show the *ac* equivalent circuit.

Find (i) the low-frequency gain, (ii) the high-frequency poles, and (iii) an estimate of the dominant high frequency pole $f_H$ of the system. Now find the GBW (gain-bandwidth) of the system. You may use half-circuit technique.



8: In the following circuit assume both transistors operate in saturation and $\lambda \neq 0$. For each transistor you can assume the parasitic capacitances as $C_{gsi}$, $C_{gdi}$, (i=1,2).




Draw the *ac* equivalent circuit, analyze and derive the expression for the dominant pole frequency.

ELEC 312, Winter 2013 term

**ELEC 312: ELECTRONICS – II : ASSIGNMENT-set-3**

**Department of Electrical and Computer Engineering**

Winter 2013

1. A series-series feedback circuit represented by Fig.1, transconductance amplifier operates with $V_s$ = 100 mV, $V_f$ = 95 mV, and $I_o$ = 10 mA. What are the corresponding values of A and β? Include the correct units for each.

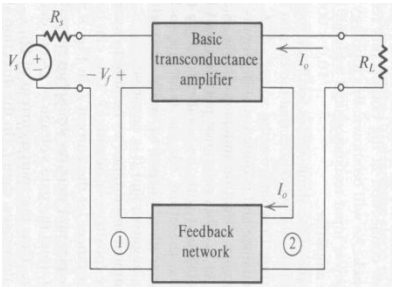



Figure 1:

2. For an amplifier connected in a negative feedback loop in which the output voltage is sampled (i.e., a shunt connection), measurement of the output resistance before and after the loop is connected shows a change by a factor of 80. Is the resistance with feedback higher or lower? What is the value of the loop gain Aβ? If $R_{of}$ is 100 Ω, what is $R_o$ without feedback?

3. The shunt-shunt feedback amplifier in the Figure 3 has I = 1 mA and $V_{GS}$ = 0.8 V. The MOSFET has $V_t$ = 0.6 V and $V_A$ = 30 V. For $R_S$ = 10 kΩ, $R_1$ =1MΩ, and $R_2$ = 4.7 MΩ, find the voltage gain $v_o/v_s$, the input resistance $R_{in}$ and the output resistance $R_{out}$. You need to figure out the *ac* parameters for the MOS device.

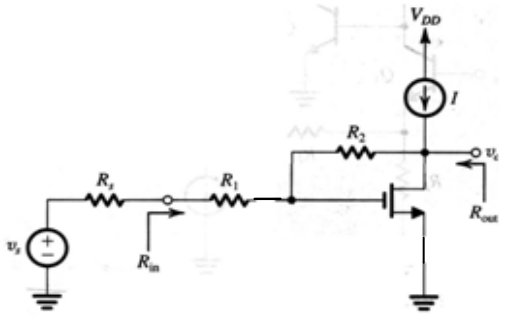



Figure 3:

4. An op amp having a low-frequency gain of $10^3$ and a single-pole transfer function with -3dB frequency of $10^4$ rad/s is connected in a negative feedback loop via a feedback network having a transmission $\beta(s)$ given by $\beta(s) = \frac{\beta_o}{(1 + s/10^4)^2}$. Find the value of $\beta_o$ above which the closed-loop amplifier becomes unstable.

5. A DC amplifier has an open-loop gain of 1000 and two poles, a dominant one at 1 kHz and a high-frequency one whose location can be controlled. It is required to connect this amplifier in a negative feedback loop that provides a dc closed-loop gain of 100 and a maximally flat response. The transfer function of the amplifier can be modeled as:

$$A(s) = \frac{1000}{(1 + s/\omega_1)(1 + s/\omega_2)}$$

In the above $\omega_1$ is the dominant pole frequency. It is required that under feedback, the amplifier will have a maximally flat response according to the model

$$A_f(s) = \frac{1000\omega_1\omega_2}{s^2 + (\omega_p / Q_p)s + \omega_p^2}$$ , with $Q_p$=0.707.

Calculate the required $\omega_2$.

**ELEC 312: ELECTRONICS – II : ASSIGNMENT-set-4**

**Department of Electrical and Computer Engineering**

Winter 2013

Q.1: Show the design of a class-A power amplifier using BJT devices, employed to deliver 10 W of ac signal power to a load of 10 ohms. Find the $V_{CC}$ required, the $I_Q$ required and design the active circuit to provide the required $I_Q$ . Comment on the heat dissipation limits of the BJT devices used in your design.

Q.2: Design an idealized class-B output stage as shown in Figure 2, to deliver an average power of 25 W to an 8 Ω speaker. The peak output voltage must be no larger than 80% of supply voltages $V_{CC}$. Assume that the input signal is sinusoidal.
Determine: (i) the required value of $V_{CC}$, (ii) the peak current in each transistor, (iii) the average power dissipated in each transistor, and (iv) the power conversion efficiency.

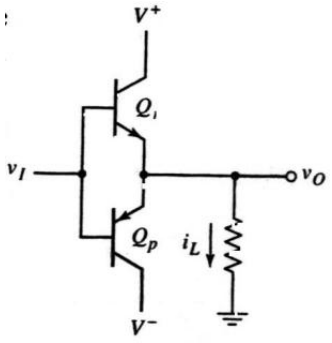



Figure 2: Basic class-B output stage

Q.3: Determine the required biasing in a MOSFET class-AB output stage. The circuit is shown in Figure 3. The parameters are $V_{DD}$ = 10 V and $R_L$ = 20 Ω. The transistors are matched, and the parameters are K = 0.20 A/V$^2$ and $|V_T|$ = 1 V. The quiescent drain current is to be 20% of the load current when $v_o$ = 5 V.
The I-V equation for either transistor is: $I_D = K(V_{GS} - |V_T|)^2$

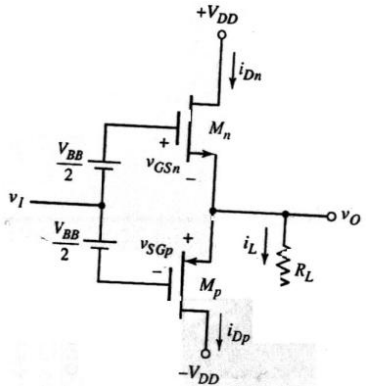



Figure 3: MOSFET class-AB output stage

**Winter 2012-2013**

**Tutorial problems set**

Chapter#2: 7.49,7.57,8.21,8.49
Chapter#2: 8.24,8.59,8.61
Chapter#3: 9.18,9.57,9.61,9.75,9.94,9.96,9.112
Chapter#4: 10.16,10.31,10.43,10.53,10.83,10.89,10.92
Cahpter#5: 11.9,11.11,11.15, E11.9, D11.19, D11.25
Chapter#6: 17.10,17.13,17.21(b)

(note: Chapters are according to the lecture note pack.
The problem numbers are according to the ref#1, i.e., the book by Sedra and Smith- 6th edn.)

| Column1 | Column12 | Column2 | Column22 | Column3 | Column4 |
|---|---|---|---|---|---|
| **Dates** | **Lectures & Tutorials** | **Topic** | **Citations from lecture note** | Quiz# | Assn# due |
| 09/01/2013 | **Lec#1** | Introduction, Review of ELEC 311 | | | |
| | | | | | |
| 11/01/2013 | **Lec#2** | Review (cont.), Current source | 2.1.1-2.1.4 | | |
| 16/01/2013 | **Lec#3** | Current mirror, non-idealities, tracking error | 2.1.1-2.1.4 | | |
| | | | | | |
| 18/01/2013 | **Lec#4** | calculations with current mirror, improved current mirror | 2.1.4, 2.1.5A-D | | |
| | | | see ref book#1 | | |
| 23/01/2013 | **Lec#5** | Active load, applications to amplifiers & current mirrors | 2.2.1-2.2.3 | | |
| 25/01/2013 | **Tut WA** | 7.49,7.57,8.21,8.49 | see ref book#1 | | |
| | | | | | |
| 25/01/2013 | **Lec#6** | Differential amplifier (DA), BJT, MOS, calculations | 2.3.1 | | |
| | | | see ref book#1 | | |
| 30/01/2013 | **Lec#7** | DA ac cacul (contd.), DA with active loads, analysis | 2.3.2 | | |
| 01/02/2013 | **Tut WA** | 8.24,8.59,8.61 | see ref book#1 | | |
| | | | | | |
| 01/02/2013 | **Lec#8** | Multistage/Integrated circuit amplifier, calculations, Review | 2.3.3 | | Assn#1 |
| | | | | | |
| 06/02/2013 | **Lec#9** | Frequency response of amplifiers, Bode plot, low freq. model | 3.2.1-2 | | |
| 08/02/2013 | **TUT WA** | 9.18,9.57 | see ref book#1 | Quiz#1 | |

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| 08/02/2013 | **Lec#10** | SCTC method, high freq.model of BJT & MOS, OCTC method | 3.3.1-2 | | |
| | | | | | |
| 13/02/2013 | **Lec#11** | High-frequency resp. of single-stage ampl., Miller's theorem | 3.4, 3.5.1-2 | | |
| 15/02/2013 | **Tut WA** | 9.61,9.75,9.94 | | | |
| | | | | | |
| **15/02/2013** | **MT test** | **Syllabus: Lectures # 2-7** | | | |
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| 15/02/2013 | **Lec#12** | Single stage amp. Resp. (contd.) | 3.5.3 | | |
| | | | | | |
| 27/02/2013 | **Lec#13** | Analysis with transfer function, dominant pole, gain bandwidt | | | |
| 01/03/2013 | **Tut WA** | 9.96,9.112 | see ref book#1 | Quiz#2 | |
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| 01/03/2013 | **Lec#14** | multi stage wide-band amplifiers, Cascode configuration | 3.6.1-2 | | Assn#2 |
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| 06/03/2013 | **Lec#15** | Wide-band DA (cont.), review | 3.6.3 | | |
| 08/03/2013 | **Tut WA** | 10.16,10.31,10.43 | | | |
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| 08/03/2013 | **Lec#16** | Negative feedback, basic configurations of feedback, two-port | 4.1, 4.2, 4.2.1-5 | | |
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| 13/03/2013 | **Lec#17** | loaded amplifier technique, calculation examples | 4.2.5-6, 4.3.1-2 | | |
| 15/03/2013 | **Tut WA** | 10.53,10.83 | see ref book#1 | Quiz#3 | |
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| 15/03/2013 | **Lec#18** | Calculations with feedback amp., | 4.3.2-4 | | |
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| 20/03/2013 | **Lec#19** | Stability, Nyquist criterion, gain & phase margin | 4.4,4.4.1-4.4.2 | | |
| 22/03/2013 | **Tut WA** | 10.89,10.92,11.9 | | | |
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| 22/03/2013 | **Lec#20** | calculations examples, freq. compensation | 4.4.3-4.4.5 | | Assn#3 |
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| 27/03/2013 | **Lec#21** | Output stage, class A operation | 5, 5.1.1 | | |
| 29/03/2013 | **Tut WA** | 11.11,11.15 | see ref book#1 | Quiz#4 | |
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| 29/03/2013 | **Lec#22** | Class B, class AB operations, calculation examples | 5.1.2-5.1.3 | | |
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| 03/04/2013 | **Lec#23** | class AB operations (cont.), alternative configurations | 5.1.3-5.2 | | |

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| 05/04/2013 | **Tut WA** | E11.9,D11.19,D11.25 | see ref book#1 | | |
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| 05/04/2013 | **Lec#24** | Power BJT/MOS, thermal considerations, Oscillators | 5.2-5.5, 6.8 | | Asn#4 |
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| 10/04/2013 | **Lec#25** | Oscillators, Wien Bridge, Phase shift oscillators | 6.8, 6.9 | | |
| 12/04/2013 | **Tut WA** | 17.10,17.13,17.21(b) | see ref book#1 | | |
| | | | | | |
| 12/04/2013 | **Lec#26** | LC oscillator, crystal oscillator, review class | 6.9, 6.10 | | |
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| **Final Exam** | **(Syllabus)** | | | | |

| Topic/Chapter of lecture note | Problem# | Answer/Note |
|---|---|---|
| DA,CM,multi-stage amp | 7.49 | 100 micro A, Vo,min=0.2V,Vo,nom=0.7V, 5 micro A |
| | 7.57 | 0.2 mA, 10% |
| | 8.21 | Ad=gm*RD/(1+gm*Rs/2), continue |
| (Ch.2) | 8.24 | ID(Q1,Q2)=50 micro A, find other ID values |
| | | Vov7=0.3, Vov6=-0.3 etc. |
| | | W/L=2*ID/(mu*Cox*Vov^2) etc. |
| | 8.49 | RC=6.19 k ohms, RE=235 ohms |
| | 8.59 | 50, 50.5*1E3 ohms |
| | 8.61 | diff pair:alpha*Rc/(2*re); cascade: same |
| Freq. resp. of amp. | 9.18 | routine analysis |
| | 9.57 | CI=200.2pF, fH=795kHz, fu=(1000/2*pi)*(1/CI*Rsig) |
| (Ch.3) | 9.61 | fH=652kHz, AM=-80; tau\|gs=16.4%, tau\|gd=67.2% etc |
| | 9.75 | gain=16, fp1=398MHz, fp2=3.79MHz, fH=3.79MHz (app) |
| | D9.81 | Vov=0.2V, ID=0.2mA,fH=56.7MHz, fT=284.2MHz, AM=-99 |
| | | fH=2.92MHz, fT remains about the same |
| | 9.94 | work with half circuit, assume ro=infinity |
| | | A(low freq)=-66.22, fH=452kHz, GBW=30MHz |
| | 9.96 | Ad=50, fp1=15.9MHz, fp2=1.6GHz, fz=3.2GHz |
| | 9.112 | (a)-(d) as follows |
| | (a) | A(DC)=10,000 |
| | (b) | Cin1=525fF |
| | (c ) | fp1=30.3MHz |
| | (d) | Cin2=530fF |
| Negative feedback | 10.16 | fL'=1Hz, fH'=1MHz |
| | 10.31 | AF=9.9, Rif=202, Rof=19.8 |
| (Ch.4) | 10.43 | Af=9.4 m mho, Rin=474.2 k ohms, Rout=1.76 Mega ohms |
| | 10.53 | Af=-9.87 k ohms, Rin=11.08 ohms, Rout=1.085 ohms |
| | 10.83 | w=1.1E5 rad/sec, beta>=0.0244 |
| | 10.89 | fc=1MHz, phase margin=90 deg |
| | 10.92 | fc=3.16E5, beta=49E-6, AcL=16.9E3 |
| Output stage | 11.9 | dead zone +-7 mV, slope (gain)=0.99, without feedback |
| (Ch.5) | | dead zone +-700 mV, slope (gain) =1 |
| | 11.11 | PL(max)=0.5W; Ps+=Ps-=0.318W; efficiency=78.5% |
| | | for half output: PL=1/8W; Ps(tot)=0.318W, eff=39.3% |
| | 11.15 | IQ=6.25mA; VBB=1.26V |
| | E11.9 | see ref book #1, p.935 |
| | D11.19 | n=relative size:1.25/0.1=12.5 |
| | D11.25 | RL/(RL+1/(2*gm)), gm=24.5 mA/V;n=12.25; IQ=1.225mA |
| Oscillator | 17.10 | frequency shift 15%; new freq. of osc.=1.15/(RC) |

(Ch.6) 17.13 L(s)=sCR/(1+3sCR+(sCR)^2); R2/R1>=2; w(freq)=1/(CR)

17.21 (b) gm+(1/R)+s(C1+C2)+(s^2*C2*L)/R+s^3*C1*C2*L=0

w(freq)=sqrt((C1+C2)/C1C2L); gm*R=C2/C1