**(For Graduate Students)**

**Modern Analog/IC Filter Design (ELEC 441/6081)**

**Mid-Term Test#2 (Winter 2009-2010)**

Electrical and Computer Engineering Department

Concordia University

March 31, 2010

Instructor: Dr. R. Raut **Student id#** **Time: 75 minutes**

Answer **All** questions Return the question paper with your answers

Q.1: Design a second-order band-pass filter using state-variable principle. The filter has *ωp*=1000 rad/sec, *Q*=5 and peak gain of 5. Use equal capacitors of 1µF each.

Q.2: Figure 2 presents a second order filter network built from two OTA devices. Find the voltage transfer function *V2/V1*, at low frequencies, assuming ideal OTA.



Figure 2:

Q.3: Design a low-pass switched capacitor filter with pass-band edge frequency *fc =*3.4 kHz, *Qp=*1.3 and DC gain of 0 dB. Use a clock frequency of 64 kHz. The largest capacitor must be less than 20 pF. You may use the general biquad structure provided in Figure 3.

You may adopt the voltage transfer function given below with suitable amendments.





Figure 3:





Q.4: Using leap-frog (operational simulation) technique design a third-order low-pass Chebyshev voltage transfer function with Ap = 1 dB. The cut-off frequency should be 5kHz, and the prototype source and load resistors should have a value of 100Ω. You may use the L,C,R structures provided with **Table B.2** . Show design of the whole system.



**(For Under-Graduate Students)**

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Q.2: Figure 2 presents a second order filter network built from two OTA devices. Find the voltage transfer function *V2/V1*, at low frequencies, assuming ideal OTA.



Figure 2:

Q.3: Analyze the given switched capacitor filter circuit (Fig.3), and derive the expression for Vo2(1)/Vi(1) in the sampled-data (i.e., z= exp (jΩT))-domain. What will be the response of this filter at DC. The given clock frequency is 64 kHz. The numbers 1 and 2 refer to switching clock signals at phases 1 and 2.



Figure 3:

Q.4: Using FDNR technique design a third-order low-pass Butterworth voltage transfer function. The cut-off frequency should be 5kHz and the prototype source and load resistors should have a value of 500Ω. All the resistors in the FDNR sections should be 5000Ω. You may use the L,C,R structures provided with **Table B.2** . Provide design for the whole system.

