Experiment – 1

MOSFET current mirror and CMOS amplifier

1. OBJECTIVES

- Test the current mirror and CMOS amplifier

2. PMOS current mirror

We would like to analyze the circuit given in Fig. 1. This circuit consists of two PMOS transistors in which one of them is in saturation. It is important that other remains in the saturation region for this mirror to work.

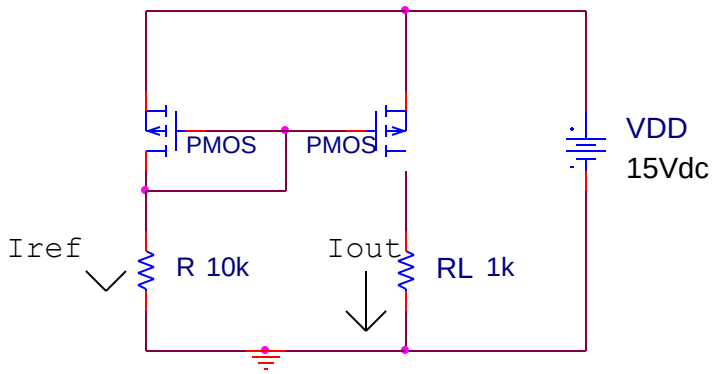


Fig. 1

3. CMOS amplifier-

The schematic shown in Fig. 2 works as a CMOS amplifier when properly biased. Here, you would recall that, VOFF stands for offset DC voltage and VAMPL is the amplitude of AC voltage that rides the DC voltage.

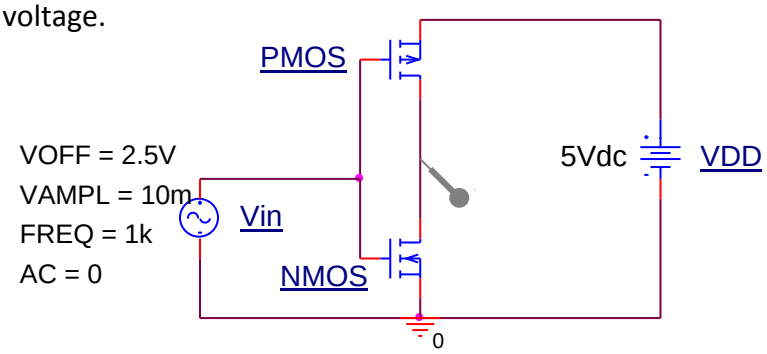


Fig. 2

It is not difficult to understand why it amplifies an input signal (Vin) when proper biasing is provided. In fact this circuit is none other than a logic inverter. Figure 3 shows the transfer characteristics for the CMOS amplifier. The gain of the amplifier is defined as

$$Gain = \frac{\Delta Vout}{\Delta Vin}$$

As you can see in Fig. 3, for a given ΔVin the value of ΔVout is quite large provided the right region in the transfer characteristic (i.e. operating point) is chosen. Hence we have amplification.

Transfer characteristic for CMOS amplifier

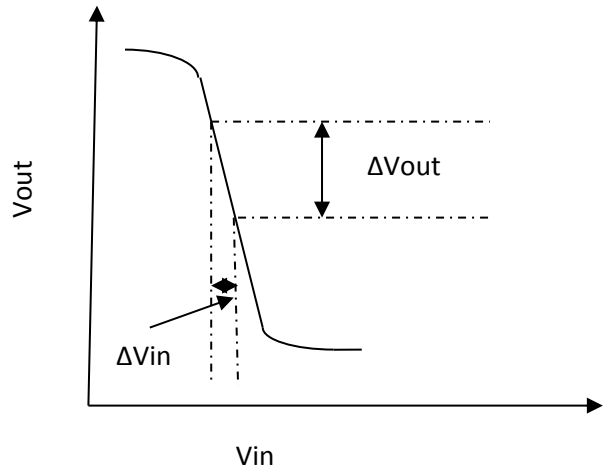


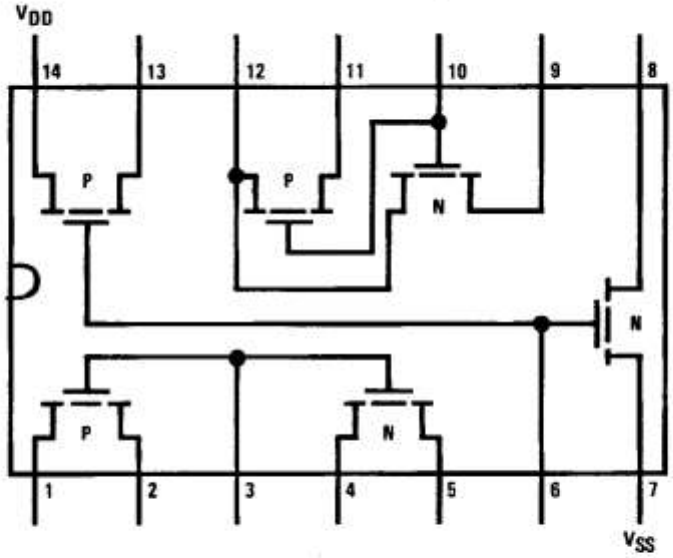
Fig. 3

Realization of Fig. 1 and Fig. 2

For the realization of the circuits discussed so far, we will use a MOSFET array (CD4007). It consists of 3 pairs of NMOS and PMOS transistors (complementary pair). The connection diagram of the chip CD4007 is given in Fig. 4.

Connection Diagram

Dual-In-Line Package



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Top View

Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS}.

Order Number CD4007

Fig. 4

Note the following points about this chip. First, the MOSFETs are symmetrical, meaning that the Source and the Drain terminals are identical. Secondly, pin 14 should be connected to the highest voltage in the circuit and pin 7 should be connected to the lowest voltage which is ground. Using 2-PMOS transistors assemble the circuit shown in Fig. 1. It will be easier to check the circuit if you use two transistors on the left side of the chip. For resistor R use a variable resistor.

1 Vary the resistor R so that Iref = 1 mA. Measure Iout.
2 Change RL to 10 KΩ and measure Iout. You would notice some difference.

Using CD4007 assemble the circuit shown in Fig. 2. Use any complementary pair. In other words use the two transistors whose gates are internally connected. It is best to use the pair that uses pin 14 and 7. That way you don't need to make separate connection for pin 14 and 7 and therefore you save time in wiring. Use the Functions generator to supply input voltage (Vin).

3 For Vin, choose VOFF = 2.5V, VAMP = 10mV and FREQ = 1KHz. Measure Vout on the oscilloscope and determine the Gain. Adjust VOFF suitably so that the gain is greater than 10. The idea behind changing VOFF is to locate a suitable point on the transfer characteristic (Fig. 3) so that the slope $\frac{dV_{out}}{dV_{in}}$ is large. That way you would get a decent amplification. Be ready to reduce input amplitude (VAMP) if Vout saturates on the oscilloscope.

4 Increase frequency so that the maximum Gain reduces by 0.707 and determine the upper 3dB frequency.

5 By observing the input (Vin) and output (Vout) simultaneously on the oscilloscope determine if the two signals are in phase or out of phase. (Observe this a lower frequency, such as 1 kHz).

6. Questions and discussion

1. Explain how the transistor on the left in fig. 1 remains in saturation.
2. Explain how the circuit in Fig. 1 works as a current mirror. What conditions should the two PMOS transistors satisfy for the mirror to work?
3. Increasing RL beyond a certain point leads to substantial reduction in Iout (Step-1). Explain why.
4. Iout measured in steps 1 and 2 are different. Generally one would expect them to be within a few percentage points of each other. Can you explain the reason? (Hint – When the MOS transistor length L is small, the channel-length modulation would be significant.)
5. In step 4 how do you explain the change in the gain?
6.
7. In step- 5, you have found the input signal and the output signal (Vout) have a particular phase relationship. With the help of Fig. 3, explain why this is the case?