SIMULATION 2

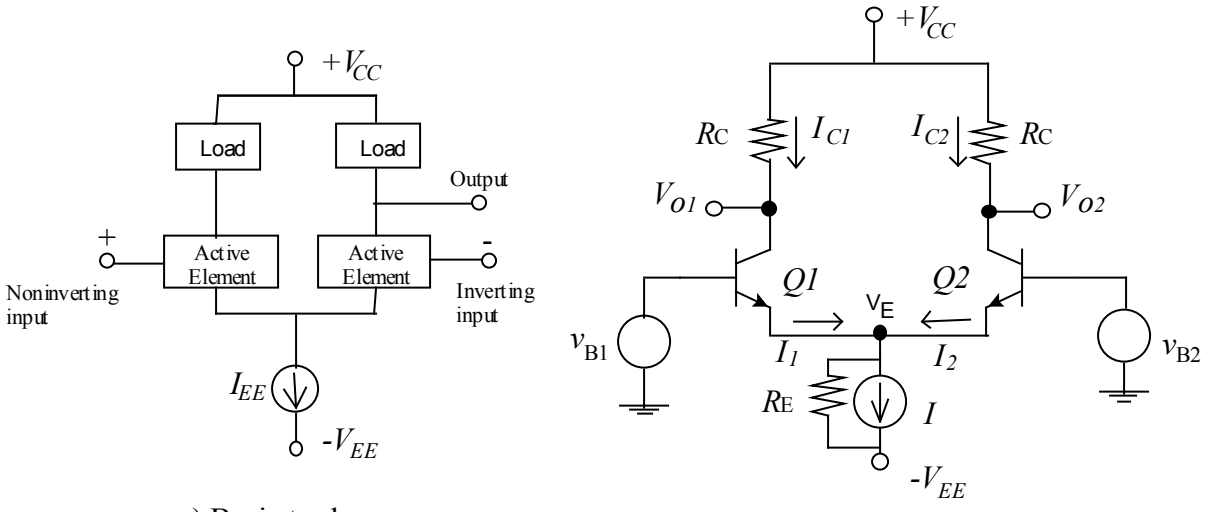
DIFFERENTIAL AMPLIFIER

OBJECTIVES

-To determine via simulation the electrical parameters of the transistor POWER NMOS.
-To determine the gain and CMRR for the MOS differential amplifier.

II. INTRODUCTION AND THEORY

The differential amplifier, or differential pair, is an essential building block in all integrated amplifiers (basic structure is shown in figure 1-a). In general, the input stage of any analog integrated circuit with more than one input consists of a differential pair or differential amplifier. The basic differential pair circuit consists of two-matched transistors $Q1$ and $Q2$, whose emitters are joined together and biased a constant current source I as shown in figure (1-b). The operation mode of the differential amplifier is defined according to the type of the input signal, for example large or small input signal, polarity of the input signals.



a) Basic toplogy b) Implementation

Figure 1

Three important characteristics of the differential input stage are: the common-mode rejection ratio *CMRR,* the input differential resistance R_{id}, and the differential-mode gain A_{DM}.

THE DIFFERENTIAL –MODE GAIN

Let $v_{B1} = v_{DM}$, $v_{B2} = -v_{DM}$, then $V_{01} = A_{DM} v_{DM}$ and $V_{02} = -A_{DM} v_{DM}$. In this case the difference between the collector voltages is $V_{O1} - V_{O2} \neq 0$. For perfectly matched transistors pair with $r_b = 0$, and source resistance $R_S = 0$, the differential gain is given by

$A_{DM} = \dfrac{V_{O1}}{V_{DM}} = \dfrac{-h_{fe} R_C}{r_\pi} = -g_m R_C$ (Hint the above equation is obtained using half-circuit concept that is one half of the circuit was used to conduct the small-signal analysis).

Note that the trans-conductance of either transistor is $g_m = \frac{|I_{Cquiecent}|}{V_T}$, Where V_T is the thermal voltage ≅ 25 mV.

THE COMMON –MODE REJECTION RATIO

Let $v_{B1} = v_{B2} = v_{CM}$ in figure 1-a where the voltage v_{CM} is called common-mode voltage. Assume that the two transistors $Q1,2$ are perfectly matched with equal the base-spreading resistance $r_b = 0$. It follows that the current I is divided equally between the two transistors and remain so as long as the transistors are in active region. The voltage at each collector will be $V_{CC} - 0.5\alpha IR_C$, and the difference $V_{O1} - V_{O2} = 0$. Any change in v_{CM} will not affect the balance of the emitter current in both transistors and the collector voltages remain the same this means that the differential pair rejects common-mode input signal. The common-mode gain is given by

$$A_{CM} = \frac{v_{O1}}{v_{CM}} \approx -\frac{R_C}{2R_E}$$

Basically the differential amplifier is designed to amplify differential signal, this requires $A_{DM} >> A_{CM}$. The ideal differential amplifier has $A_{DM} \approx \infty,$ and $A_{CM} \approx 0$. The Common-Mode Rejection Ratio *CMRR* is used as a measure of the differential amplifier performance. It is defined as

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

Substitute the values of the differential and common gains in the above equation

$$CMRR = 1 + 2g_m R_E \approx 2g_m R_E$$

As we can see from the above equation increasing the value of R_E, the *CMRR* will increase, in other words the performance of the differential amplifier can be improved by simply increasing the emitter resistance. A common practice is to use a current source to replace R_E, the results will be high *CMRR*. To avoid dealing with large numbers the *CMRR* is expressed in dB as given below

$$(CMRR)_{dB} = 20\log\left|\frac{A_{DM}}{A_{CM}}\right|$$

PRACTICAL INPUT- OUTPUT SIGNALS

So far we have assumed that the input signal is present in either common-mode or differential-mode. In practice the input signals can be decomposed into common-mode and differential-mode components. The input signals v_{B1} and v_{B2} can be represented as the sum and the difference of two other signals v_{DM} and v_{CM}, that is

$$v_{B1} = v_{DM} + v_{CM} \quad ; \quad v_{B2} = v_{CM} - v_{DM}$$

Solving for v_{DM} and v_{CM}; $v_{DM} = \frac{v_{B1} - v_{B2}}{2} = \frac{v_d}{2}$ and $v_{CM} = \frac{v_{B1} + v_{B2}}{2}$

Similarly the output consists of two components. One component is due to the differential input signal, and the second is produced by the common-mode input as given below

$$V_{O1} = A_{DM} v_{DM} + A_{CM} v_{CM}$$
$$V_{O2} = -A_{DM} v_{DM} + A_{CM} v_{CM}$$

The differential amplifier is called single-ended if the output is taken from only one designated output. The case where both output terminals are used is called differential-output.

DIFFERENTIAL-MODE INPUT- OUTPUT RESISTANCE

Looking into the collector of either transistor and assuming that the transistor load is a passive load as shown in figure 1-b. The differential-mode output resistance $R_{O(DM)}$ is simply the output resistance of common-emitter stage and equals R_C. If R_C is replaced by an active load, the output resistance will be r_O which is small-signal output resistance of the transistor.

The differential–mode input resistance $R_{i(DM)}$ is the resistance seen by the differential signal v_d (i.e. looking into the base of the BJT) and is given by $R_{i(DM)} = 2r_\pi$, Where $r_\pi = \frac{h_{fe}}{g_m}$. Note that the signal source resistance R_S and the base-spread resistance r_b of the BJT are neglected in all calculations.

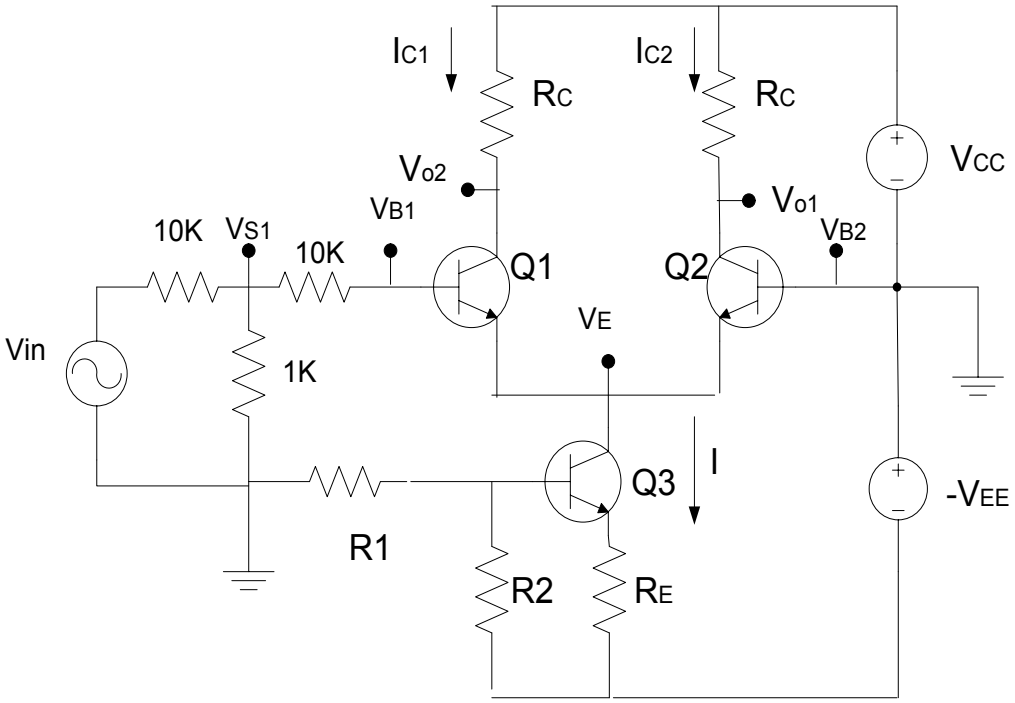


Figure 2

Please read appendix 1 before you come to the lab. In this experiment, we assume the previous knowledge of the PSPICE.

III. SIMULATION PROCEDURE

a) Device Characteristics

The MOSFET V-I characteristic curve is simply represented by the relationship between the drain-source voltage and the drain current at a constant gate voltage.

1- Draw the schematic shown in Fig**. 3.** Create a new simulation profile with name "transistor Characteristics". For the NMOS use the POWER NMOS that can be accessed by going to PLACE→PSPICE Components→Discrete→Power NMOS.

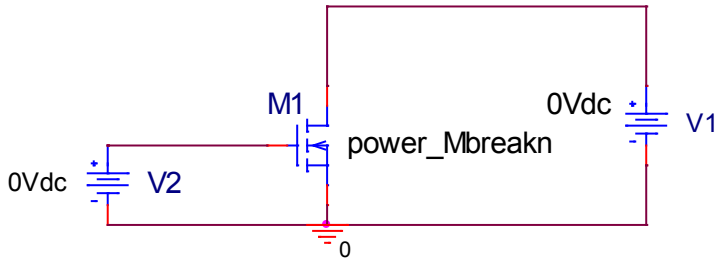


Fig. 3

2- Set the Simulation Setting as follows:

Analysis Type :	DC Sweep
Options:	Primary Sweep
Sweep Variable	Voltage Source, and Name V1
Sweep Type	Linear
Start Value= 0, End Value=12, Increment=0.1	

3- Select Secondary Sweep under Options menu, and then set the followings:

Sweep Variable	Voltage Source, and Name V2
Sweep Type	Linear
Start Value=3, End Value= 6, Increment=0.5	

4- Run the simulation, an empty graph window appears.

5- From the top menu of the graph window, select trace, and then add trace. Select ID(M1) and click on OK.

6- Label each curve with the v_{GS} values.

7- From the $i_D - v_{DS}$ characteristic curves identify and estimate the following regions and parameters:

a) Saturation region.

b) Triode region.

c) Cutoff region.

d) Plot i_D versus v_{GS} with v_{DS} as a parameter (only one curve at single value of v_{DS} such that $v_{DS} \geq v_{GS} - V_t$). In this case, modify Fig. 3 so that V1=6 V. Set the simulation setting as follows:

Analysis Type :	DC Sweep
Options:	Primary Sweep
Sweep Variable	Voltage Source, and Name= V2

Sweep Type Linear
Start Value= 0, End Value=5, Increment=0.1

Run the simulation. You will see an empty black screen. From menu bar click TRACE and then ADD TRACE. Then select I_D(M1). Using this graph, estimate the threshold voltage V_{T0} and transconductance, g_m for this transistor? Now, on the left side of the output screen there is an icon that says "View Simulation Output File". Click on this file and you can see the properties of this MOSFET at the bottom. Read the threshold voltage (V_{T0}) from the device parameters and compare.

b) MOSFET Differential Amplifier

1- Draw MOSFET differential amplifier below.

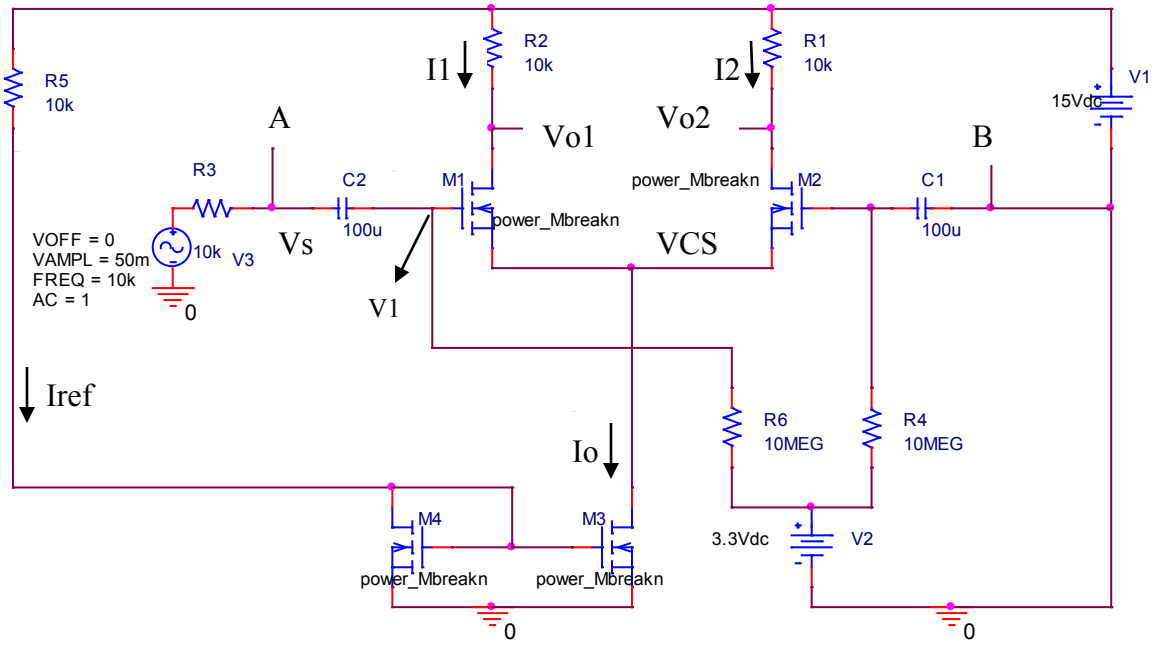


Fig. 4 (MOSFET differential amplifier)

2- Set the input signal source V3 parameters as follows:

-Offset	0	
-VAMPL	50	m
-Frequency	10	KHz
-AC	1	

3- Use the Bias Current display to read the following currents I_1, I_2, I_{ref}, and I_O. Also note the voltage VCS. You would need this information while answering question1.

4- Create a new simulation profile "Time Domain".

5- Set the simulation settings as follows: Analysis Type to "Time Domain (Transient), and Run to time 400 us. Make "Maximum step size=1us". Press OK to close the window.

6- Run the simulation.

7- Display the input and the output signals. Measure the peak-to-peak values of the followings. To get the values of various parameters (especially i_{D1} and i_{D2}) use the option "TRACE→ADD TRACE→choose particular output from the list" from the output window. For the voltage values you could use the marker.

v_1	v_{O1}	v_{O2}	i_{D1}	i_{D2}

Calculate the differential gain A_d and the input differential resistance R_{id}.

8- Create a new simulation profile "Frequency Domain".

9- Set the Simulation Settings to the following:

Analysis Type	AC Sweep/Noise
Start Frequency	1Hz
End Frequency	100K
Points/Decade	11
AC Sweep Type	Logarithmic

10- Attach "dB Magnitude of Voltage" marker to the output node (Pspice → Markers → Advanced → dB Magnitude of Voltage). The output node we choose is Vo1.

11- Run the simulation.

12- Use "Toggle Cursor" to determine the 3dB point. What is the BW of the differential amplifier? Obtain a graph for the magnitude and the phase response.

13- Modify the circuit connections as follows: disconnect the ground connection at point B and connect the points A and B. This circuit configuration is known as differential amplifier with a common-mode input signal. The analysis type would be "Time Domain (Transient)". Use the markers to obtain the peak-to-peak values of the voltage parameter. For the current parameters you need to use ADD TRACE option.

v_S	i_{D1}	i_{D2}	v_1	v_{O1}	v_{O2}

Calculate the common-mode gain A_{CM} and the common-mode input resistance R_{iCM}. What is the CMRR (dB)?

III. QUESTIONS

1- Employing hand calculations conduct a DC analysis for the circuit in Fig. 4. The DC analysis should be done for each transistor M1, M2, M3, and M4. You need to determine if
   - The transistor is on, and
   - If it is operating in the saturation region (active region).

   For this hand calculation you would need the values obtained in step 3 of part (b). You would also need V_{T0}. Use the value given in the Output file. In other words use the value PSPICE uses for simulation.
2- What is the purpose of voltage source V2 in the circuit given in Fig. 4?
3- The gate and the drain of the transistor M4 are shorted. What is the reason?