SIMULATION 3

CASCODE BJT AMPLIFIER

(SIMULATION)

I. OBJECTIVES

- To study the behavior of single stage CE and CB amplifiers.
- To design and study the characteristics of the cascode amplifier using BJTs.
- To determine the upper 3dB frequency of the CE, CB and the cascode BJT amplifiers.

II. INTRODUCTION AND THEORY

a) SINGLE –STAGE BJT AMPLIFIER CONFIGURATIONS

Three different amplifier circuit configurations can be obtained by selecting one of the transistor terminals as a common between input circuit and output circuit. In the BJT circuits, figure 3 shows these configurations, which are known as Common Base (CB), Common Emitter (CE), and Common Collector (CC). These amplifier circuit configurations lead to significant changes in the amplifier characteristics. The most noticeable changes in CC (emitter follower) configurations are: the input resistance becomes very high and the gain is close to the unity. These specific characteristics are translated into a useful application known as buffer amplifier.

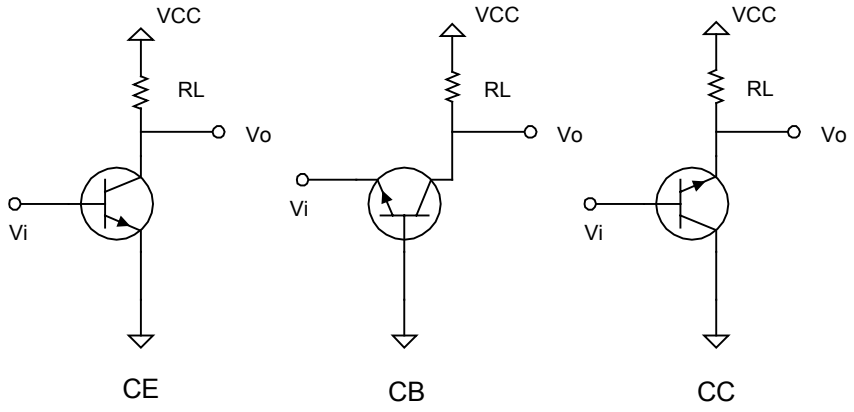

Figure **1**

Therefore amplifier configurations are employed to widen the scope of the amplifier circuit applications. Table1 summarizes the main characteristics of each configuration. The model used in the analysis is the T-model with transistor parameters, g_m: transconductance, r_e: emitter

resistance, β_{ac}: common-emitter current gain, and α: common-base current gain. R_c, R_e, R_L are the collector, the emitter, and the load resistors

Table 1

	CB	**CE** with R_e	**CC**
R_i	r_e	$\equiv (\beta_{ac}+1)(r_e+R_e)$	$\cong (\beta_{ac}+1)R_L$
R_o	R_c	R_c	$\cong r_e + \dfrac{R_s}{\beta_{ac}+1}$
A_v	$\cong g_m R_c$	$-\dfrac{R_i}{r_e+R_e}$	$\cong 1$
A_i	α	$-\beta_{ac}$	$\cong \beta_{ac}+1$

NOTICE THAT in CE configuration the presence of R_e has a very large impact on the input resistance and the voltage gain. Most device manufacturers specify β_{ac} as h_{fe} and r_i as h_{ie}. From table1 we observe that the input resistance of the CB configuration is much smaller than the input resistance of CE or CC configuration. The input and output resistances of the above amplifier configurations limit the use of the amplifier to certain applications. Figure 2 below shows a single stage CE and CB amplifiers. Notice the difference between the relative positions of the input-output signals in both configurations.

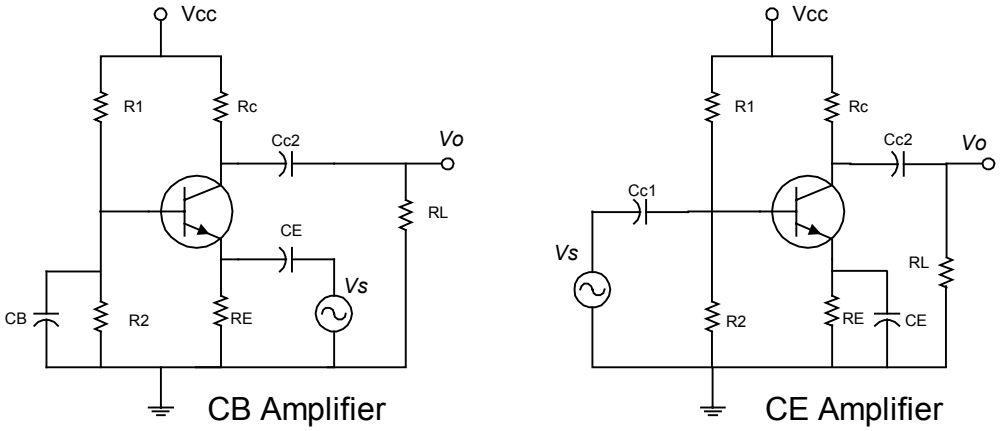

Figure **2**

b) THE CASCODE CONFIGURATION

An important amplifier configuration is known as cascode amplifier. It consists of a common-emitter (CE) stage followed by a common-base (CB) stage as shown in figure 3. The common-emitter configuration presents a relatively high input resistance $(\beta_{ac}+1)*r_e$ to the signal source.

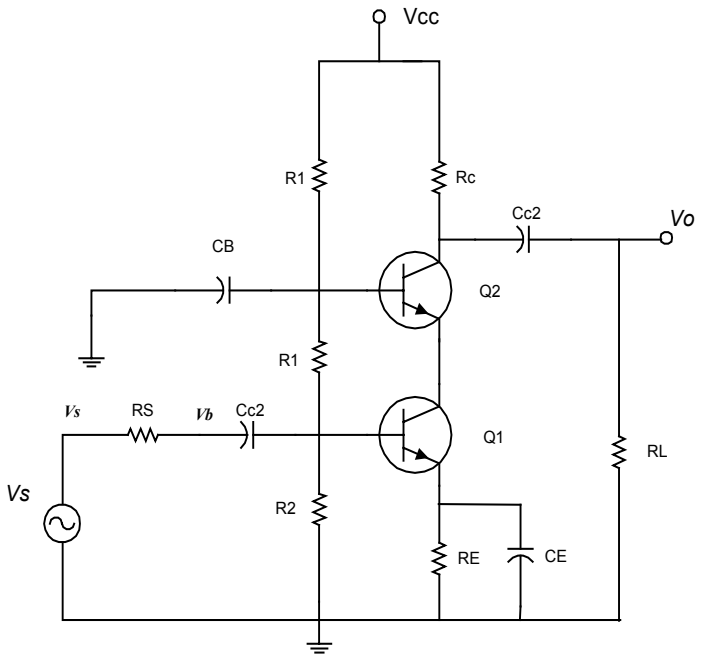

Figure **3**

The common-base configuration presents a very low input resistance, r_e. By replacing the collector resistance R_C in the CE amplifier stage with a common base CB amplifier stage, the CE-CB configuration virtually eliminates the Miller effect of C_{u1}. This will lead to higher 3dB frequency than is possible with a simple common-emitter amplifier. An extension in the upper cutoff frequency is achieved without reducing the midband gain (Gain-Bandwidth rule), since the collector of Q2 carries a current almost equal to the collector current of Q1. Another reason for extending the upper cutoff frequency is that, in the CB configuration the Miller effect does not exist and does not limit the high-frequency response. Notice that the effective load resistance seen by the CE transistor Q1 is very low and equal to the input resistance r_e of the CB transistor Q2. The transistor Q2 acts as a current buffer or an impedance transformer. Tables 2 and 3 show the summary of the theoretical formulas of the gain and the 3dB frequencies for CE and Cascode amplifiers.

Table 2 High-Frequency Response of the CE Amplifier

Midband Gain	Lower 3dB Frequency	Upper 3dB Frequency
$A = -\frac{R_{in}}{R_{in} + R_S} g_m R'_L$ Where $R_{in} = R_1 // R_2 // (r_\pi + r_x)$ $R'_L = R_C // R_L // r_o$	$w_L \approx \frac{1}{C_{C1} R_{C1}} + \frac{1}{C_E R'_E} + \frac{1}{C_{C2} R_{C2}}$ Where $R_{C1} = R_S + [R_2 // R_2 // (r_\pi + r_x)]$ $R'_E = R_E // \left(\frac{(R_1 // R_2 // R_S) + r_\pi + r_x}{\beta_{ac} + 1} \right)$ $R_{C2} = R_L + (R_C // r_o)$	$w_H \approx \frac{1}{(R_S // R_{in})[C_\pi + C_u (1 + g_m R'_L)]}$ Where $R_{in} = R_1 // R_2 // (r_\pi + r_x)$ $R'_L = R_C // R_L // r_o$

Table 3 High-Frequency Response of the Cascode Amplifier

Midband Gain	Lower 3dB Frequency	Upper 3dB Frequency
$A = -\frac{R_{in}}{R_i + R_S} g_m R'_L$ $\times \frac{r_\pi}{r_\pi + r_x + R_2 // R_3 // R_S}$ Where $R = R_2 // R_3$ $R'_L = R_C // R_L$	$w_L \approx \frac{1}{C_{C1} R_{C1}} + \frac{1}{C_E R'_E} + \frac{1}{C_{C2} R_{C2}}$ Where $R_{C1} = R_S + [R_2 // R_2 // (r_\pi + r_x)]$ $R'_E = R_E // \left(\frac{(R_1 // R_2 // R_S) + r_\pi + r_x}{\beta_{ac} + 1} \right)$ $R_{C2} = R_L + R_C$	$w_H \approx \frac{1}{R'_S (C_{\pi 1} + 2C_{u1})}$ Where $R_{in} = R_1 // R_2 // (r_\pi + r_x)$ $R'_L = R_C // R_L // r_o$

III. Input and Output Resistance

All the following measurmets must be taken at the midband frequency and the output signal must suffer no distortion.

a) Input resistance measurement

Measure the small-signal voltage gains $A_{v1} = \frac{v_o}{v_b}$ and $A_{v2} = \frac{v_o}{v_S}$ at the input points v_b and v_S respectively. The input resistance is given by the following equation

$$R_{in} = \frac{R_S}{([A_{v1} / A_{v2}] - 1)} \quad (1)$$

b) Output resistance measurement

Measure the open loop (disconnect R_L) voltage gain, $A_{v1} = \frac{v_o}{v_b}$. Connect R_L and measure the voltage gain, $A_{v2} = \frac{v_o}{v_b}$. The output resistance is given by the following equation

$$R_O = R_L([A_{v1} / A_{v2}] - 1) \quad (2)$$

DOWNLOADING THE SCHEMATICS

In this lab-session, you will download the schematics from the webpage: http://users.encs.concordia.ca/~shailesh/. Click on "ELEC-312-PSPICE-Schematics". Download this zipped folder (ELEC-312.zip) into your home directory (My Documents). Open this folder under Zip File Manager. You would see all the documents. From EDIT menu click on "SELECT ALL". Then click on EXTRACT. A new window opens asking you where to copy these files. Copy them in a new folder called "ELEC-312" of the directory "My Documents". Now you are all set. For the remainder of this semester, this is the only folder you would need for simulation.

VI. PROCEDURE

1- Open Capture Student and recall **CASCODE1** circuit**.**

2- For the signal source V2 set the value of the VOFF=0, the VAMPL=40mV, and FREQ=10 KHz. Conduct DC analysis for this circuit.

3- Use Enable Bias Voltage and Current Display to read the following currents and voltages for transistors Q1:

V_B	V_E	V_C	I_B	I_E	I_C	β_{dc}

4- From Pspice menu select "New Simulation Profile" with a name "time domain parameters".

5- Set the Simulation Settings as follows: Analysis Type to "Time domain (Transient)". Choose the suitable "Run to Time" to obtain 5 complete cycles of the input/output signals. Make "Maximum step size = 1u". Record all the necessary data to compute the gain, input resistance and output resistance of the amplifier. Vs and V_b are shown in Fig 3.

6- From Pspice menu select "New Simulation Profile" with a name "Frequency Domain Parameters".

7- Delete the signal source V2 (VSIN) and replace it by (VAC) from the SOURCE library.

8- Set the Simulation Settings to the following:

Analysis Type AC Sweep/Noise

Start Frequency	100Hz
End Frequency	1MEG
Points/Decade	11
AC Sweep type	Logarithmic.

Place dB magnitude of voltage at the output node and observe Vo. What is the BW of the amplifier? What is the figure of merit (Gain Bandwidth product) for this amplifier?

9- Open Capture Student and recall **CASCODE2** circuit**.**

10- Repeat step2 and record the data in the table below.

V_B	V_E	V_C	I_B	I_E	I_C	β_{dc}

11- Repeat steps 3-8 with frequency range 10Hz to 20MHz. Tabulate the gain, BW, input and output resistance obtained from CASCODE1 and CASCODE2 circuits. What are the main characteristics of each amplifier?

12- Open Capture Student and recall **CASCODE3** circuit**.**

13- Repeat step2 and record the data in the table shown below for transistors Q1 and Q2:

V_{B1}	V_{E1}	V_{C1}	V_{B2}	V_{E2}	V_{C2}	I_{B1}	I_{C1}	I_{B2}	I_{C2}	β_{dc1}	β_{dc2}

14- Repeat steps 3-8 with input signal frequency range 100Hz to 4MHz. What is the BW of the amplifier? What is the figure of merit (Gain Bandwidth product) for this amplifier? Compare these values with similar values obtained for the amplifier circuit CASCODE1 and CASCODE2. Write your explanation.

VII. QUESTIONS

1- What is the operating point (the quiescent point) of the amplifiers cascode1, cascode2 and cascode3?

2- Conduct a dc analysis for the circuits, cascode1, cascode2 and cascode3. Compare the theoretical and simulation values.