Simulation – 1

MOSFET current mirror and CMOS amplifier (Simulation)

1. OBJECTIVES

- Simulate a current mirror.
- Simulate a CMOS amplifier.

2. Simulation of PMOS current mirror

We would like to analyze the circuit given in Fig. 1. This circuit consists of two PMOS transistors in which one of them is in saturation. It is important that other remains in the saturation region for this mirror to work.

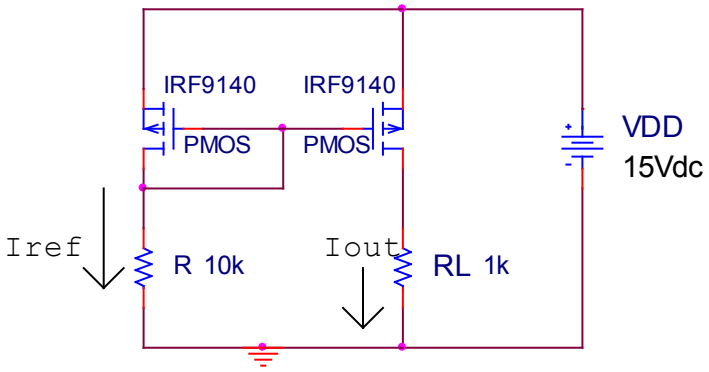

Fig. 1

Assemble the circuit below using PSPICE. The PMOS transistor can be found in EVALAA.olb library. IRF9140 is listed there. Using bias-point analyses determine Iref and Iout. You would notice that Iout is very close to Iref.

1 Now increase RL so that Iout decreases by a factor of 3 or more. Try to figure out why the current mirror stopped working. Note that the threshold voltage for the PMOS transistor is **-3.387 V**.

3. Simulation of a CMOS amplifier-

The schematic shown in Fig. 2 works as a CMOS amplifier when properly biased. Here, you would recall that in the language of PSPICE, VOFF stands for offset DC voltage and VAMPL is the amplitude of AC voltage that rides the DC voltage.

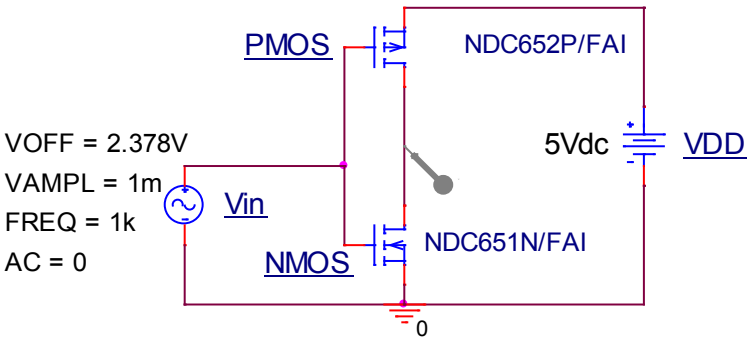

Fig. 2

It is not difficult to understand why it amplifies an input signal (Vin) when proper biasing is provided. In fact this circuit is none other than a logic inverter. Figure 3 shows the transfer characteristics for the CMOS amplifier. The gain of the amplifier is defined as

$$Gain = \frac{\Delta Vout}{\Delta Vin}$$

As you can see in Fig. 3, for a given ΔVin the value of ΔVout is quite large provided the right region in the transfer characteristic (i.e. operating point) is chosen. Hence we have amplification.

Transfer characteristic for CMOS amplifier

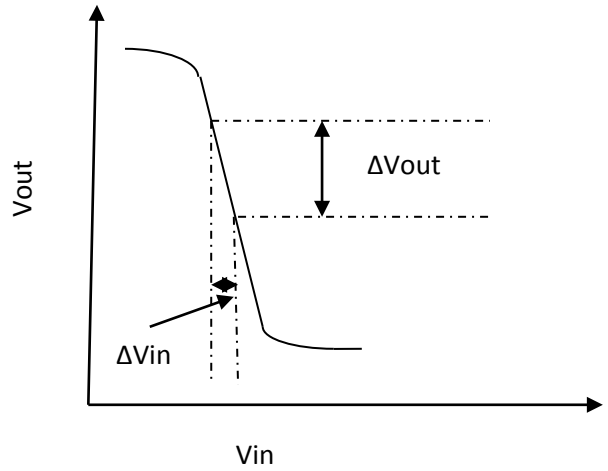

Fig. 3

Using PSPICE, assemble the schematic given in Fig. 2. Here, Vin and VDD are available in the SOURCE library. Vin is VSIN of the SOURCE library. The value of the parameter VOFF has been

carefully chosen to get a decent amplification. The transistors NMOS and PMOS are obtained from the Fairchild library of devices (Fairchild.olb). For PMOS, make sure that the bulk is connected to Source (VDD).

2 Using time-domain analysis in the PSPICE program, determine the gain of the CMOS amplifier. Use the following setting: Run to Time=5m; Maximum step size=1u.
3 Determine if Vin and Vout are in phase or out of phase.
4 Change the biasing voltage (VOFF) by 10 mV and observe the change in the gain.