Logic Synthesis with Synopsys Design Compiler

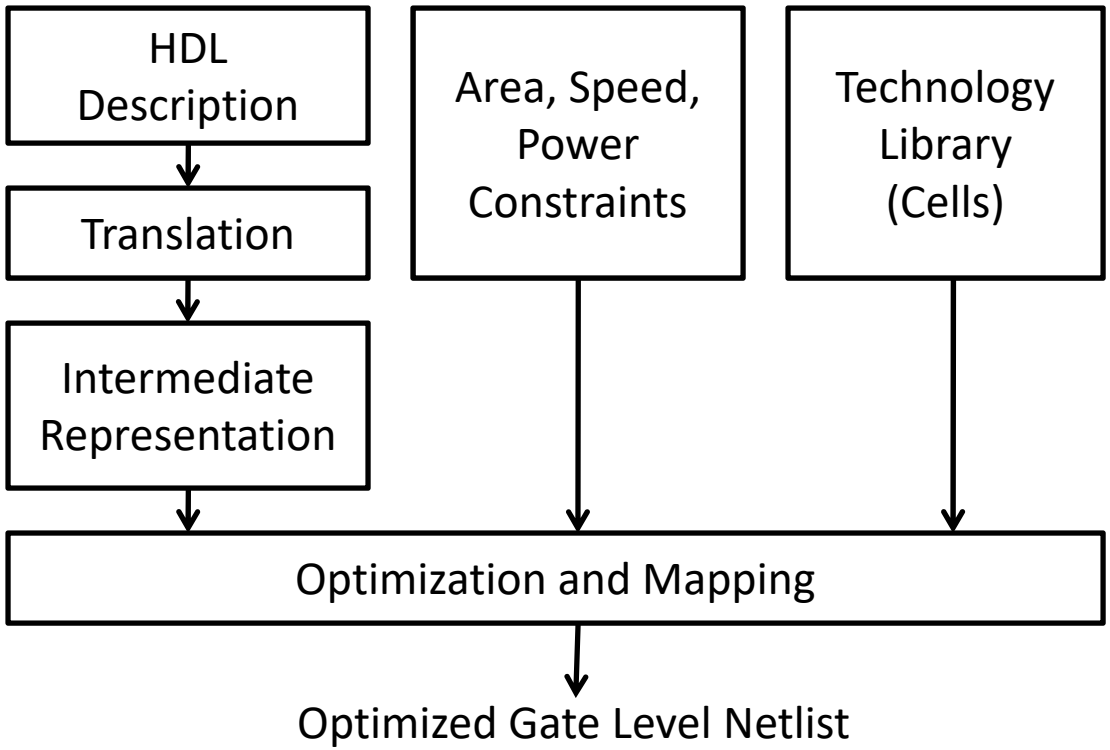
Formal Hardware Verification

(COEN6551)

Summer 2016

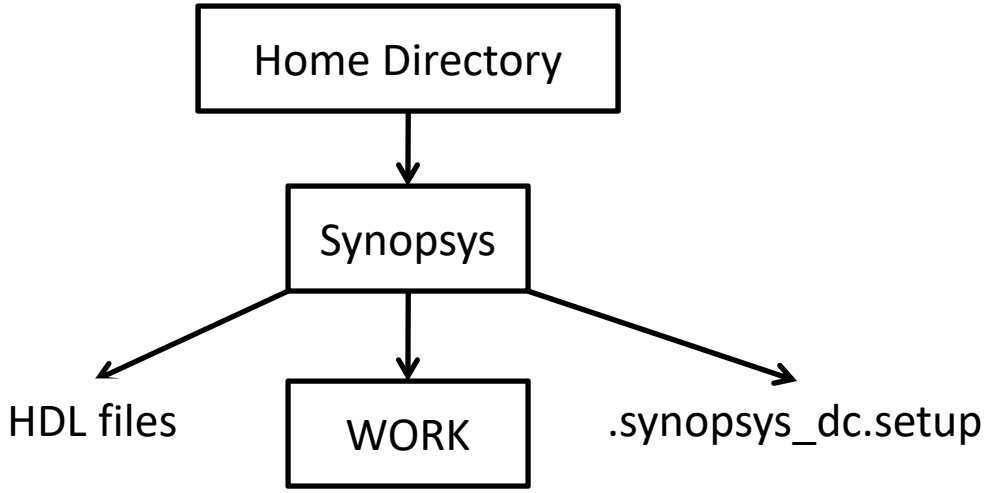
Synthesis = Faithful transformation from one description to another

RTL → Gate level



Setup

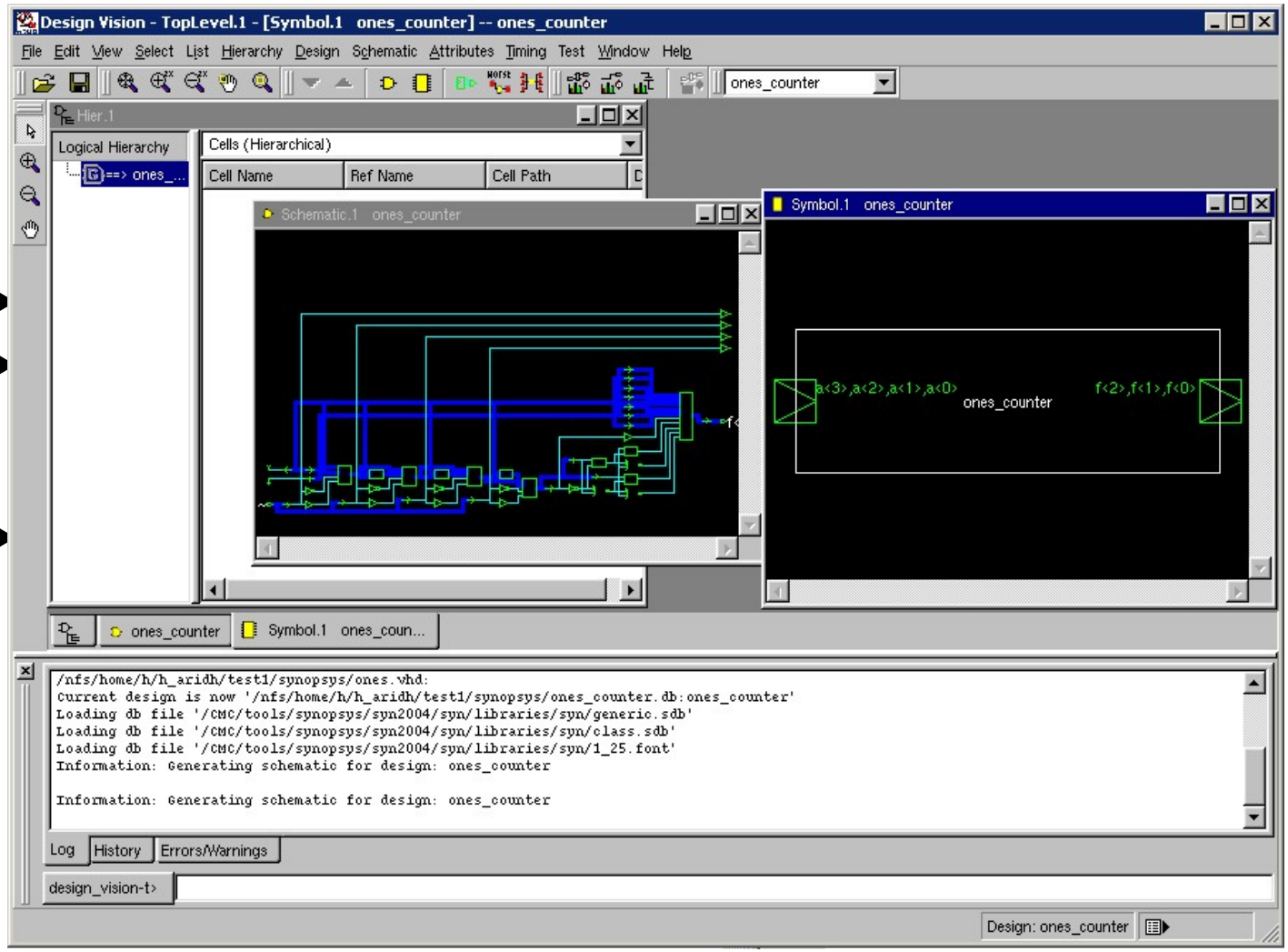
Make new directory : mkdir synopsys
Copy HDL and setup files: use UNIX copy command
Source the environment file: source /CMC/ENVIRONMENT/synopsys.env



design_analyzer &

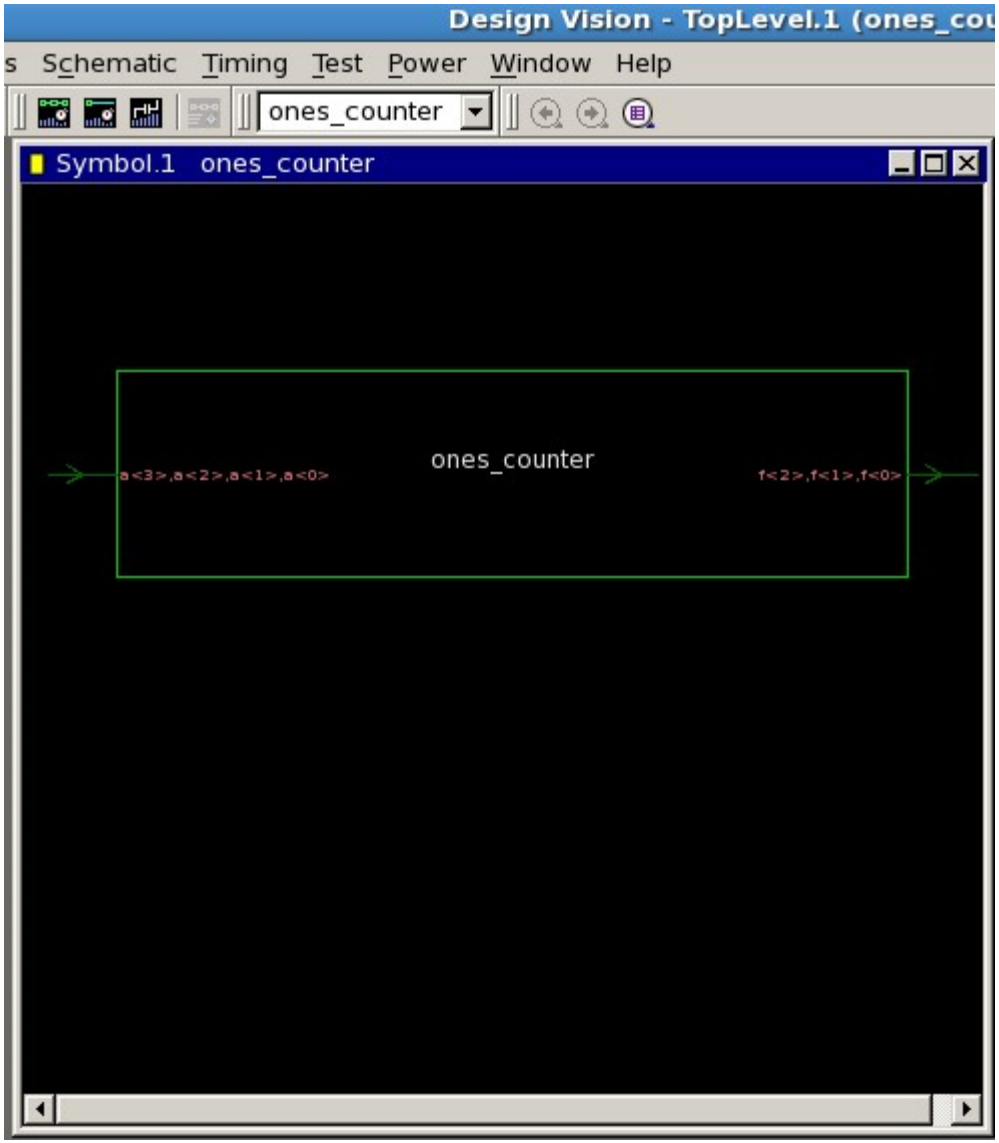
Schematic and Symbol Views

Move up and Down the hierarchy



fm_shell -f scriptfile

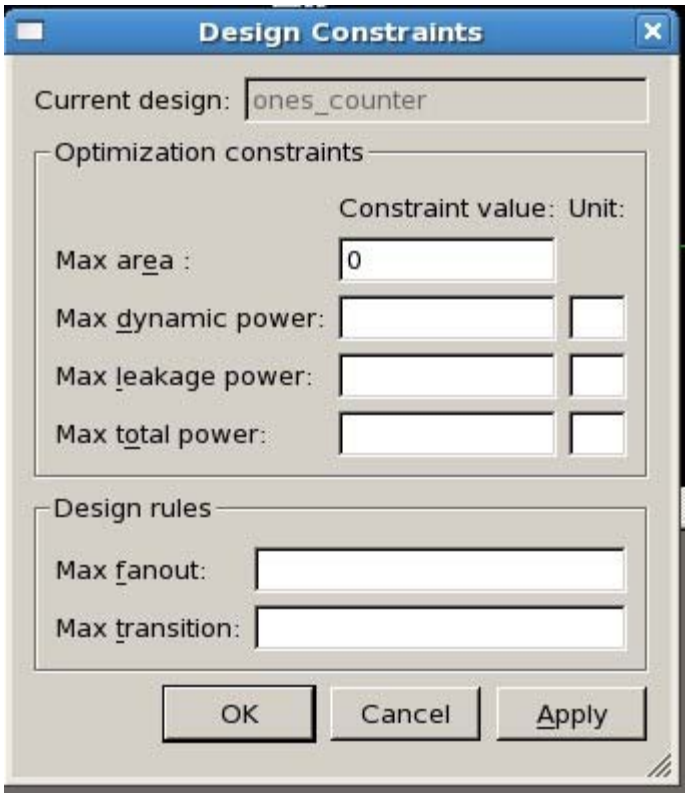
Symbolic View



Area and Power Constraints

Maximum area

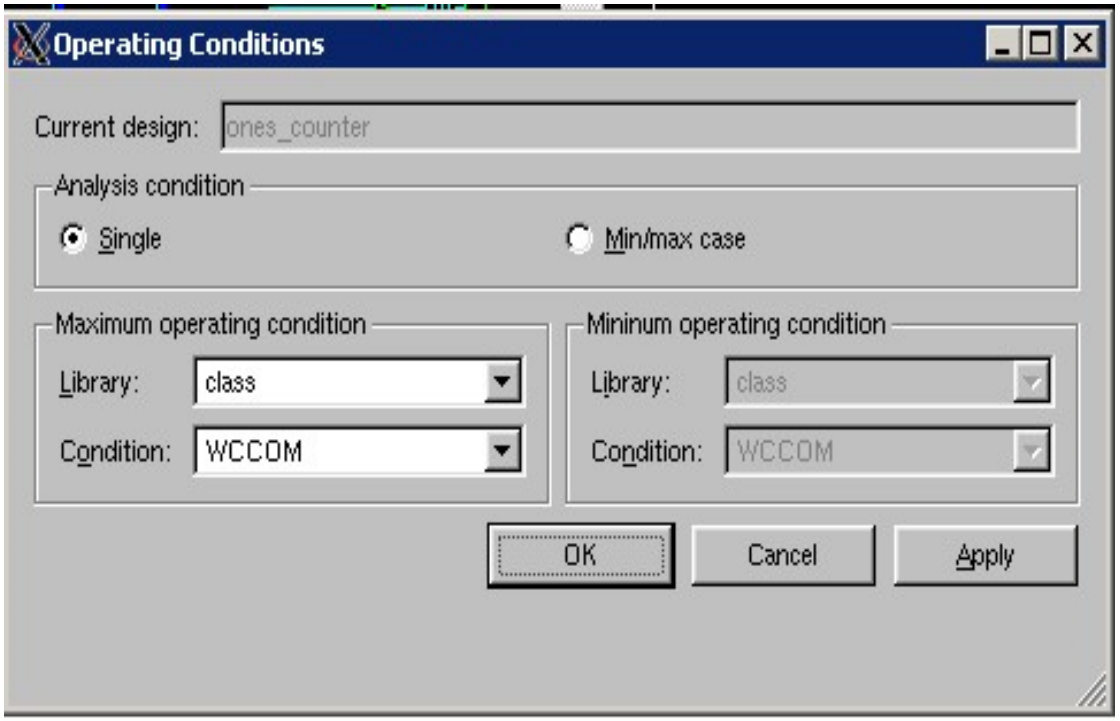
Dynamic and leakage power



Attributes ➔Optimization constraints ➔Design constraints

Operating Conditions

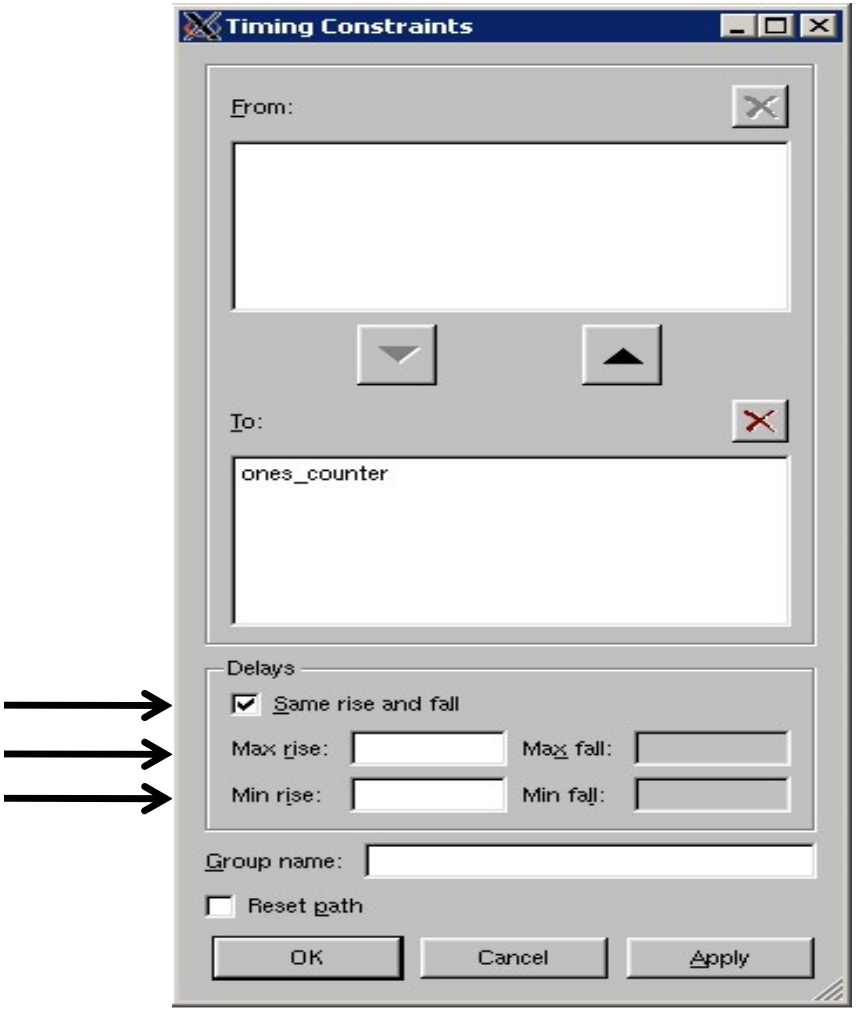
Commercial
Industrial
Military



Attributes ➔ Operating Environment ➔ Operating Conditions

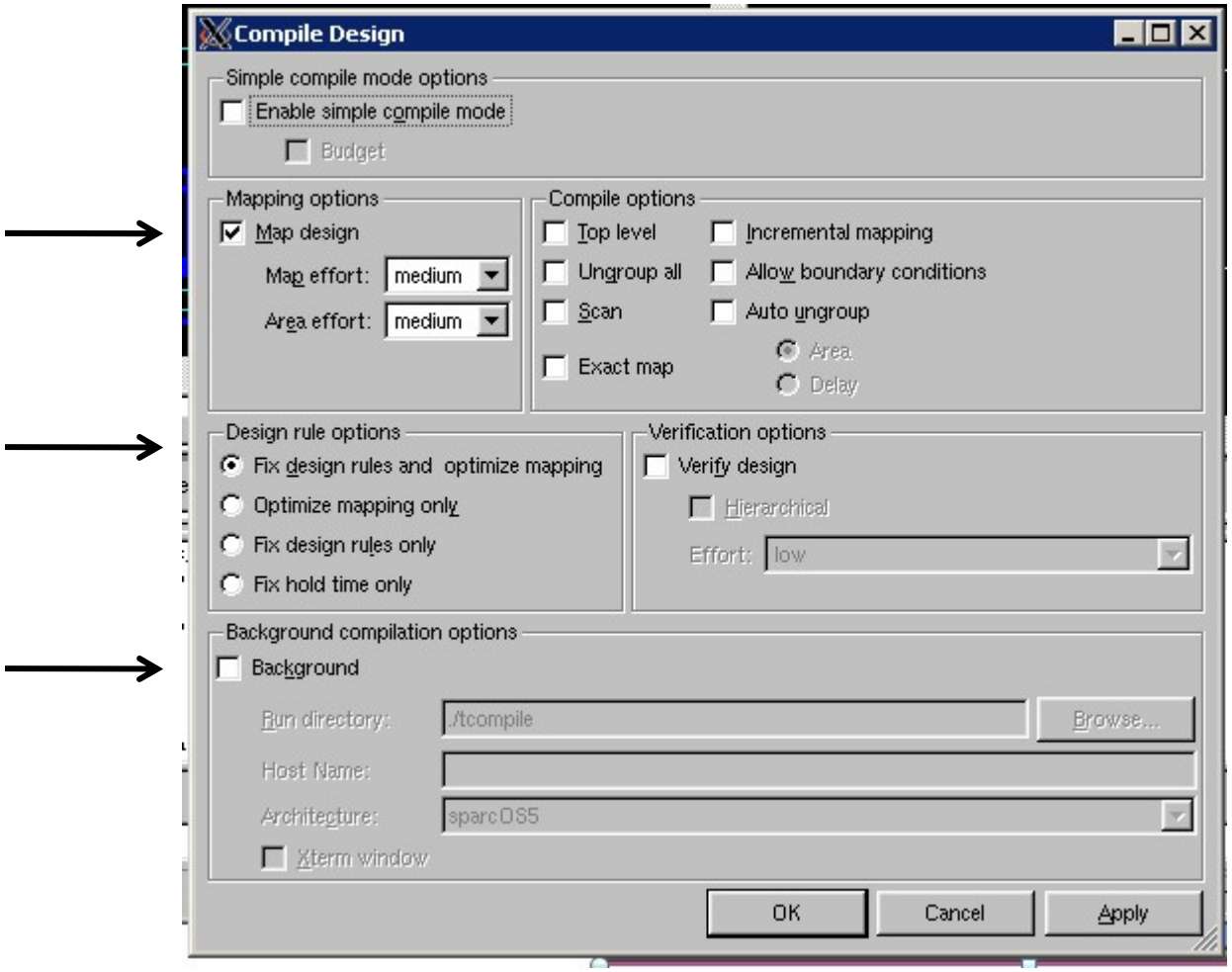
Timing Constraints

Rise and Fall Delay times



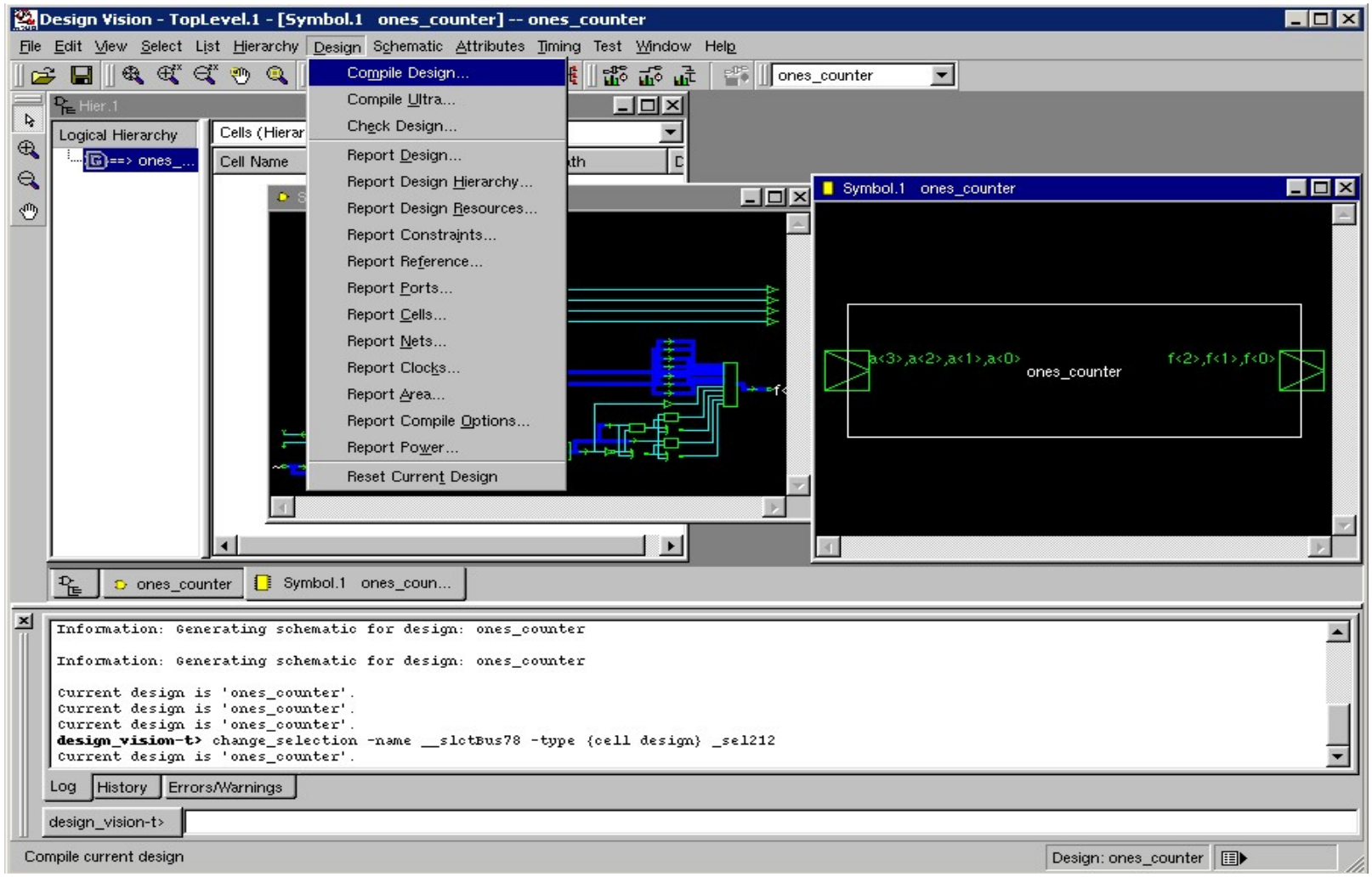
Attributes ➔Optimization constraints ➔Timing constraints

Logic Synthesis and Optimization



Tools ➔Design optimizations

Synthesis Report



Analysis ➔Report