

Equivalence Checking Using Synopsys Formality

Formal Hardware Verification

(COEN6551)

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The Reference and Implemented Design

```
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File Edit Options Buffers Tools VHDL Help

component EN
  port( A, B : in std_logic; Z : out std_logic);
end component;

signal n248, n249, n250, n251, n252 : std_logic;

begin
  U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
  U60 : E0 port map( A => n248, B => n251, Z => f(1));
  U62 : IV port map( A => a(3), Z => n250);
  -- U61 : ANDNA2 port map( A => n249, B => n250, Z => n251);
  -- U61 : NR2 port map( A => n249, B => n250, Z => n251);
  -- U61 : OR2 port map( A => n249, B => n250, Z => n251);
  U61 : E0 port map( A => n249, B => n250, Z => n251);
  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n251);
  U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n251);
  U65 : EN port map( A => n252, B => a(2), Z => n249);
  U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;

-- ** ones_syn1.vhd (VHDL/es) --L66--56%

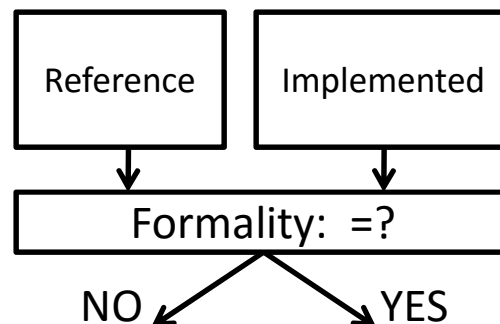
signal n248, n249, n250, n251, n252 : std_logic;

begin
  U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
  U60 : E0 port map( A => n248, B => n251, Z => f(1));
  U61 : NR2 port map( A => n249, B => n250, Z => n251);
  U62 : IV port map( A => a(3), Z => n250);
  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n251);
  U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n251);
  U65 : EN port map( A => n252, B => a(2), Z => n249);
  U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;

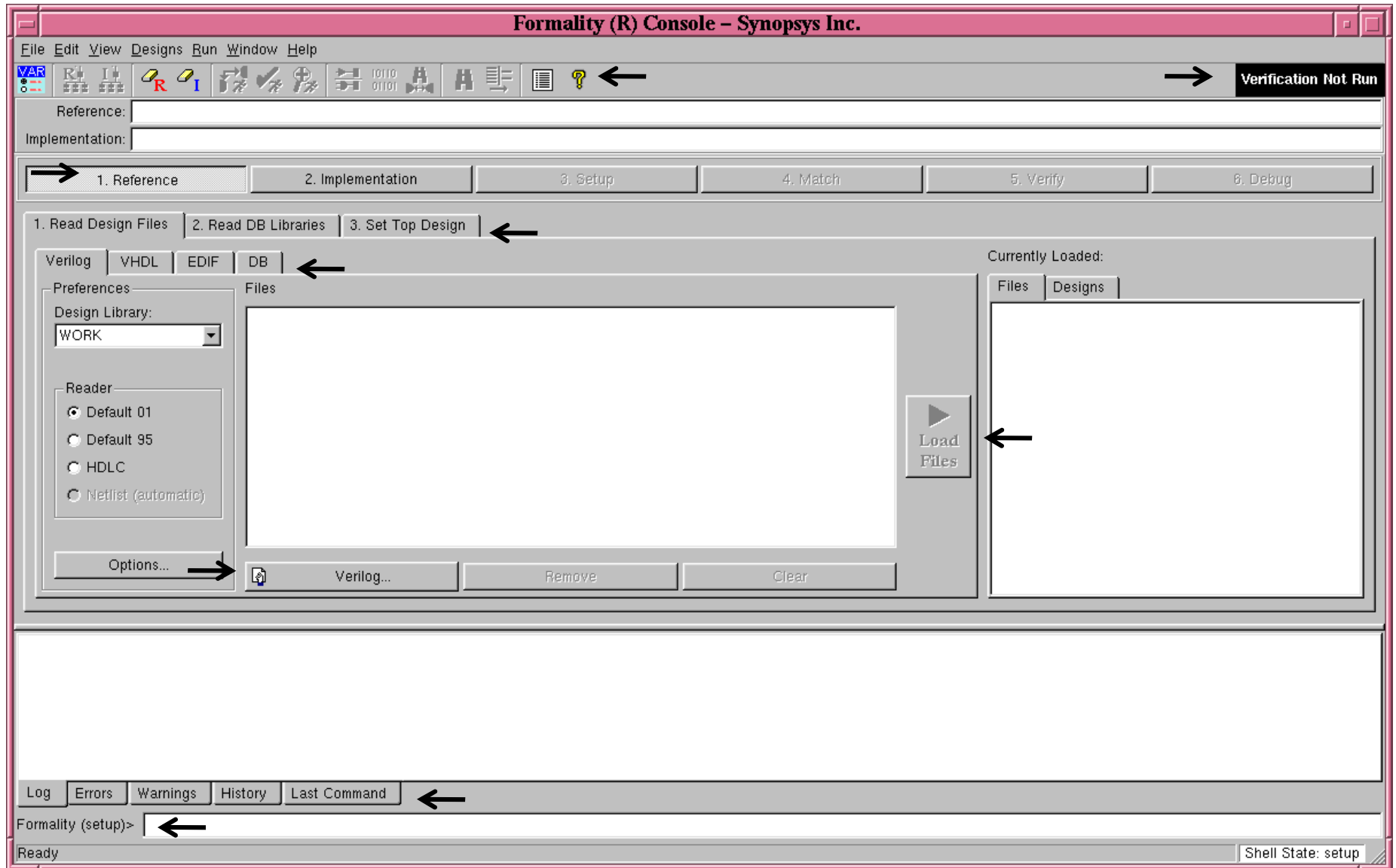
-- ** ones_syn.vhd (VHDL/es) --L73--Bot
```

Design with Bug

Reference Design



Formality Main Interface



Error Candidates

The screenshot shows the Formality (R) Console interface. At the top, the title bar reads "Formality (R) Console - Synopsys Inc.". Below the title bar is a menu bar with "File", "Edit", "View", "Designs", "Run", "Window", and "Help". A toolbar contains various icons for navigation and analysis. A status bar at the top right indicates "Diagnosis Complete".

The main workspace is divided into several sections. At the top, there are fields for "Reference: r:/WORK/ones_counter" and "Implementation: i:/WORK/ones_counter". Below these are six tabs: "0. Guidance", "1. Reference", "2. Implementation", "3. Setup", "4. Match", "5. Verify", and "6. Debug". The "1. Reference" and "2. Implementation" tabs are active, indicated by green checkmarks.

Below the tabs is a row of sub-tabs: "Failing Points", "Passing Points", "Aborted Points", "Unverified Points", "Probe Points", and "Analyses". An arrow points to the "Analyses" tab. The "Analyses" tab is active and displays a table of error candidates.

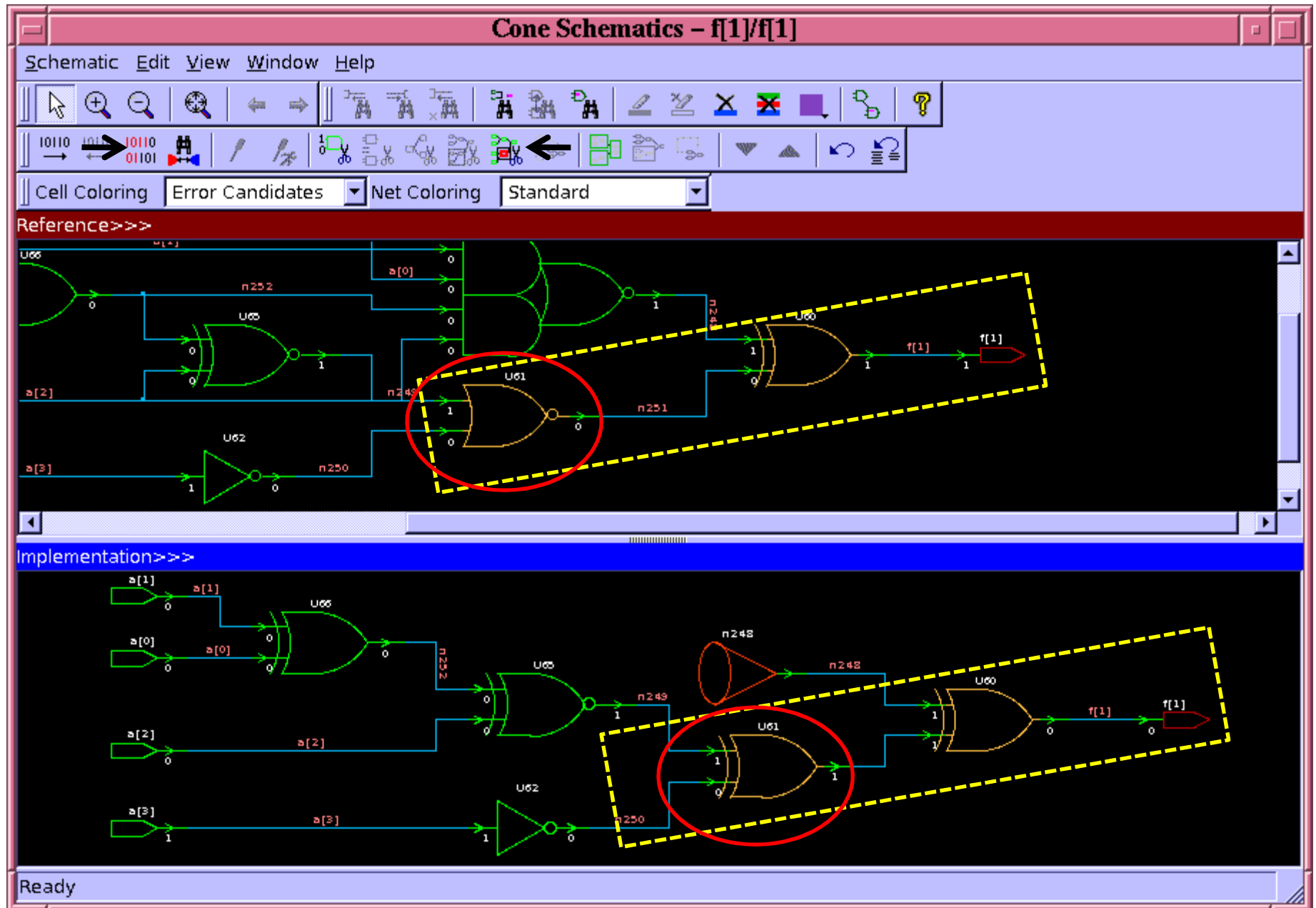
Possible Failure Causes		Error	Type	Related Failing Points
Diagnosis Error Candidates (2)		1 U61	cell	1
Candidate: 0				
Candidate: 1				

At the bottom of the console is a command prompt window. It shows the following text:

```
Info: Formality Guide Files (SVF) can improve verification success by automating setup.
0
Formality (verify)> diagnose
Status: Diagnosing i:/WORK/ones_counter vs r:/WORK/ones_counter...
Status: Diagnosis initializing...
Status: Analyzing patterns...
Single error detected in implementation design.
Number of error candidates: 2
Analysis completed
Status: Finding matching regions in reference design...
Single matching region detected in reference design.
Diagnosis completed
1
```

Arrows point to the "diagnose" command and the "Number of error candidates: 2" output. Below the command prompt are buttons for "Log", "Errors", "Warnings", "History", and "Last Command". The status bar at the bottom right shows "Shell State: verify".

Tracing the cause of Equivalence Failure



Patterns for which Equivalence Failed

Patterns - f[1]/f[1]

File Edit View Window Help

Compare point values for vector 1

R f[1] (Port) f[1] 1

I f[1] (Port) f[1] 0

Filter pruned cone schematic inputs

	Type	Reference	Implementation	1	2	3	4	5
1	Port	a[0]	a[0]	0	0	1	0	1
2	Port	a[1]	a[1]	0	0	1	1	0
3	Port	a[2]	a[2]	0	1	1	0	0
4	Port	a[3]	a[3]	1	0	0	0	0

Ready