Datorstödd Elektronikkkonstruktion
[Computer Aided Design of Electronics]

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http://www.ida.liu.se/~TDTS80

Electronics Systems

Design of Electronics Systems
Goals

- Basic principles of computer-aided design.
- Digital design at high levels of abstraction.
- Synthesis and testability techniques.
- The hardware description language VHDL and its use in the design/synthesis process.

Course Organization

- Lectures (Zebo and Petru):
  - Introduction and basic terminology.
  - VHDL: overview and simulation semantics.
  - Behavioral modeling with VHDL.
  - Structural modeling with VHDL.
  - High-level synthesis of digital systems.
  - Testing and design for test.
Course Organization (Cont’d)

- **Laboratory part (Gert):**
  - One seminar on the CAD system to be used.
  - Lab assignments with VHDL.

- **Literature:**
  - Lecture notes (www.ida.liu.se/~TDTS80).

Lecture I

- Trend in microelectronics
- The design process and tasks
- Different design paradigms
- Basic terminology
- The test problems
The Technological Trend

Moore’s Law

(# of transistors per chip would double every 1.5 years)

Intel Microprocessor Evolution

<table>
<thead>
<tr>
<th>Year/Month</th>
<th>Clock = 1/τc</th>
<th>Transistors</th>
<th>Micras</th>
</tr>
</thead>
<tbody>
<tr>
<td>I4004</td>
<td>1971/11</td>
<td>108 KHz.</td>
<td>2300</td>
</tr>
<tr>
<td>I8080</td>
<td>1974/04</td>
<td>2 MHz.</td>
<td>6000</td>
</tr>
<tr>
<td>I8086</td>
<td>1978/06</td>
<td>10 MHz.</td>
<td>29000</td>
</tr>
<tr>
<td>I80286</td>
<td>1982/02</td>
<td>12 MHz.</td>
<td>0.13 m.</td>
</tr>
<tr>
<td>I486DX</td>
<td>1989/04</td>
<td>25 MHz.</td>
<td>1.2 m.</td>
</tr>
<tr>
<td>Intel DX2</td>
<td>1992/03</td>
<td>100 MHz.</td>
<td>1.6 m.</td>
</tr>
<tr>
<td>Pentium</td>
<td>1993/03</td>
<td>60 MHz.</td>
<td>3.1 m.</td>
</tr>
<tr>
<td>Pentium Pro</td>
<td>1995/11</td>
<td>200 MHz.</td>
<td>5.5 m.</td>
</tr>
<tr>
<td>Pentium II</td>
<td>1998/11</td>
<td>450 MHz.</td>
<td>7.5 m.</td>
</tr>
<tr>
<td>Pentium III</td>
<td>2000/01</td>
<td>1000 MHz.</td>
<td>28 m.</td>
</tr>
<tr>
<td>P4</td>
<td>2000/09</td>
<td>1400 MHz.</td>
<td>82 m.</td>
</tr>
</tbody>
</table>
Intel Microprocessor Evolution

![Graph showing the evolution of Intel microprocessors over time, with key technology milestones indicated.]

Technology Directions: SIA Roadmap

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Feature size (nm)</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>Logic: trans/cm²</td>
<td>18M</td>
<td>44M</td>
<td>109M</td>
<td>269M</td>
<td>664M</td>
</tr>
<tr>
<td>Trans/chip</td>
<td>17.6M</td>
<td>190M</td>
<td>539M</td>
<td>1523M</td>
<td>4308M</td>
</tr>
<tr>
<td>#pads/chip</td>
<td>2553</td>
<td>3492</td>
<td>4776</td>
<td>6532</td>
<td>8935</td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>2100</td>
<td>3500</td>
<td>6000</td>
<td>10000</td>
<td>16900</td>
</tr>
<tr>
<td>Chip size (mm²)</td>
<td>430</td>
<td>520</td>
<td>620</td>
<td>750</td>
<td>900</td>
</tr>
<tr>
<td>Wiring levels</td>
<td>7</td>
<td>7.8</td>
<td>8.9</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>Power supply (V)</td>
<td>1.5</td>
<td>1.2</td>
<td>0.9</td>
<td>0.6</td>
<td>0.5</td>
</tr>
<tr>
<td>High-perf pow (W)</td>
<td>130</td>
<td>160</td>
<td>170</td>
<td>175</td>
<td>183</td>
</tr>
<tr>
<td>Battery pow (W)</td>
<td>2</td>
<td>2.4</td>
<td>2.8</td>
<td>3.2</td>
<td>3.7</td>
</tr>
</tbody>
</table>
**System on Chip (SoC)**

- Hardware
  - microprocessor
  - ASIC
  - Analog circuit
  - Sensor
- Software
  - Embedded memory
  - DSP
  - Network
  - High-speed electronics

**Design Requirements**

- **Technology-driven:**
  - Greater Complexity
  - Higher Density
  - Increased Performance
  - Lower Power Dissipation

- **Market-driven:**
  - Shorter Time-to-Market (TTM)
The Design Challenges

- Complexity implication:
  - 300 gates/person-week
  - 15,000 gates/person-year
  - For a 12-million gate system:
    - 800 designers for one year
    - $120 million design cost
      ($150K salary)

Mixed Technologies

- Embed in a single chip: Logic, Analog, DRAM blocks
- Embed advanced technology blocks:
  - FPGA, Flash, RF/Microwave
- Beyond Electronic
  - MEMS
  - Optical elements
What are the Solutions?

- Powerful design methodology and tools.
- Advanced architecture (modularity).
- Extensive design reuse.

Capture and Simulate

- The detailed design is captured in a model.
- The model is simulated.
- The results are used to guide the improvement of the design.
- All design decisions are made by the designers.
Abstraction Hierarchy

- **Layout/silicon level** — The physical layout of the integrated circuits is described.

- **Circuit level** — The detailed circuits of transistors, resistors, and capacitors are described.

- **Logic (gate) level** — The design is given as gates and their interconnections.

Abstraction Hierarchy (Cont’d)

- **Register-transfer level (RTL)** — Operations are described as transfers of values between registers.

- **Algorithmic level** — A system is described as a set of usually concurrent algorithms.

- **System level** — A system is described as a set of processors and communication channels.
The Three Domains

- **Structural domain** — A component is described in terms on an interconnection of more primitive components.

- **Behavioral domain** — A component is described by defining its input/output response.

- **Physical/geometrical domain** — A component is described in terms of its physical placement and characteristics (e.g., shape).
Describe and Synthesize

- Description of a design in terms of behavioral specification.
- Refinement of the design towards an implementation by adding structural details.
- Evaluation of the design in terms of a cost function and the design is optimized w.r.t. the cost function.

\[
\begin{align*}
\omega_1 &= (a + b)c + d; \\
\omega_2 &= (d + f)c; \\
\omega_3 &= (a + b)d + df;
\end{align*}
\]

High-Level
Describe and Synthesize

- Description of a design in terms of behavioral specification.
- Refinement of the design towards an implementation by adding structural details.
- Evaluation of the design in terms of a cost function and the design is optimized for the cost function.

For I=0 To 2 Loop
Wait until clk'event and clk=´1´;
If (rgb[I] < 248) Then
P=rgb[I] mod 8;
...
IP-Based Design

- Intellectual Property: pre-designed and pre-verified building blocks.
- Design reuse
- Hard v. soft IPs
- Interface synthesis
- Verification
- Testing

Source: VSI Alliance

Basic Terminology

- Design — A series of transformations from one representation to another until one exists that can be fabricated.
- Synthesis — Transforming one representation to another at a lower abstraction level or a behavioral representation into a structural representation at the same level.
- Analysis — Studying a representation to find out its behavior or checking for certain property of a given representation.
- Simulation — Use of a software model to study the response of a system to input stimuli.
- Verification — The process of determining that a system functions correctly.
- Optimization — The change of a design representation to a new form with improved features.
Design Activities

A Typical Top-Down Design Process
Testing and its Current Practice

- To meet users’ quality requirements.
- Testing aims at the detection of physical faults (production errors/defects and physical failures).

Automatic Test Equipment

Testing of Mixed Technologies

- How to test the mixed chip?
- Need **multiple** ATE for a single chip: Logic ATE, Memory ATE, Analog ATE.
- Need **SUPER** ATE with combined capabilities.
High Performance On Chip

- High speed ATE substantially more expensive.
- ATE vs chip technology discrepancy: Tester uses 5 year old technology - Chips move to next generation every 2 years.
- ATE accuracy degrading: Chip cycle time will crossover ATE accuracy.

![Graph showing ATE vs chip technology discrepancy.](source: SIA Roadmap)

High Complexity: Bandwidth

- # of transistors increases exponentially.
- # of access port remains stable.
- Implication:
  - # of transistors per pin (Testing Complexity Index) increases rapidly.

![Graph showing testing complexity index.](source: W. Malý, 1996)
Built-In Self Test (BIST)

- Solution: Dedicated built-in hardware for embedded test functions.
- No need for expensive ATE.
- At-speed testing.
- Current test possible.
- Support O&M.
- Support field test.

Challenges to the CAD Communities

- System specification with very high-level languages.
- Modeling techniques for heterogeneous system.
- Testing must be considered during the design process.
- Design verifications -> get the whole system right the first time!
- Very efficient power saving techniques.
- Global optimization.
The Electronics System Designer

- Low cost
- High perf.
- Low pow
- Good testability
- X-

Conclusion Remarks

- Much of design of digital systems is managing complexity.
- What is needed: new techniques and tools to help the designers in the design process, taking into account different aspects.
- We need especially design tools working at the higher levels of abstraction.
- If the complexity of the microelectronics technology will continue to grow, the migration towards higher abstraction level will continue.