

Equivalence Checking Using Cadence Conformal LEC

Formal Hardware Verification

(COEN 6551)

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The Golden and the Revised Designs

```
component EN
  port( A, B : in std_logic; Z : out std_logic);
end component;

signal n248, n249, n250, n251, n252 : std_logic;

begin
  U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
  U60 : E0 port map( A => n248, B => n251, Z => f(1));
  U62 : IV port map( A => a(3), Z => n250);
  -- U61 : ANDNA2 port map( A => n249, B => n250, Z => n251);
  -- U61 : NR2 port map( A => n249, B => n250, Z => n251);
  -- U61 : OR2 port map( A => n249, B => n250, Z => n251);
  U61 : E0 port map( A => n249, B => n250, Z => n251);
  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n252);
  U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n249);
  U65 : EN port map( A => n252, B => a(2), Z => n249);
  U66 : E0 port map( A => a(1), B => a(0), Z => n252);

end SYN_rtl;
```

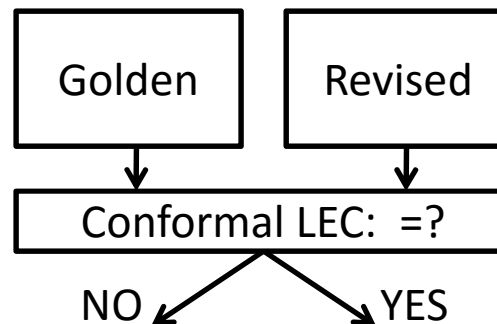
```
signal n248, n249, n250, n251, n252 : std_logic;

begin
  U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
  U60 : E0 port map( A => n248, B => n251, Z => f(1));
  U61 : NR2 port map( A => n249, B => n250, Z => n251);
  U62 : IV port map( A => a(3), Z => n250);
  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n252);
  U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n249);
  U65 : EN port map( A => n252, B => a(2), Z => n249);
  U66 : E0 port map( A => a(1), B => a(0), Z => n252);

end SYN_rtl;
```

Revised Design

Golden Design



The screenshot shows the CONFORMAL-LEC software interface. The main window is divided into two panes: 'Golden (ones_counter)' and 'Revised (ones_counter)'. Both panes show a tree view with 'ones_counter' and '8 library cells'. A 'Compare' dialog box is open in the foreground, featuring buttons for 'Compare', 'Cancel', and 'Help'. The dialog includes checkboxes for 'Stop After Mismatch', 'Stop After Abort', 'Display Non-equivalent Points', and 'Add All Compare Points' (which is checked). The main window's command-line area shows the following commands and output:

```

Mapped points: SYSTEM class
-----
Mapped points  PI  PO  Total
Golden         4   3   7
Revised        4   3   7
-----
LEC> add compared points -all
// Command: add compared points -all
// 3 compared points added to compare list
LEC> compare
// Command: compare
-----
Compared points  PO  Total
Equivalent       2   2
Non-equivalent   1   1
-----
SETUP> read design /disk/scratch/naeem/lec/ones_syn1.vhd -VHDL -Revised
SETUP> set system mode lec
LEC> add compared points -all
LEC> compare
LEC>

```

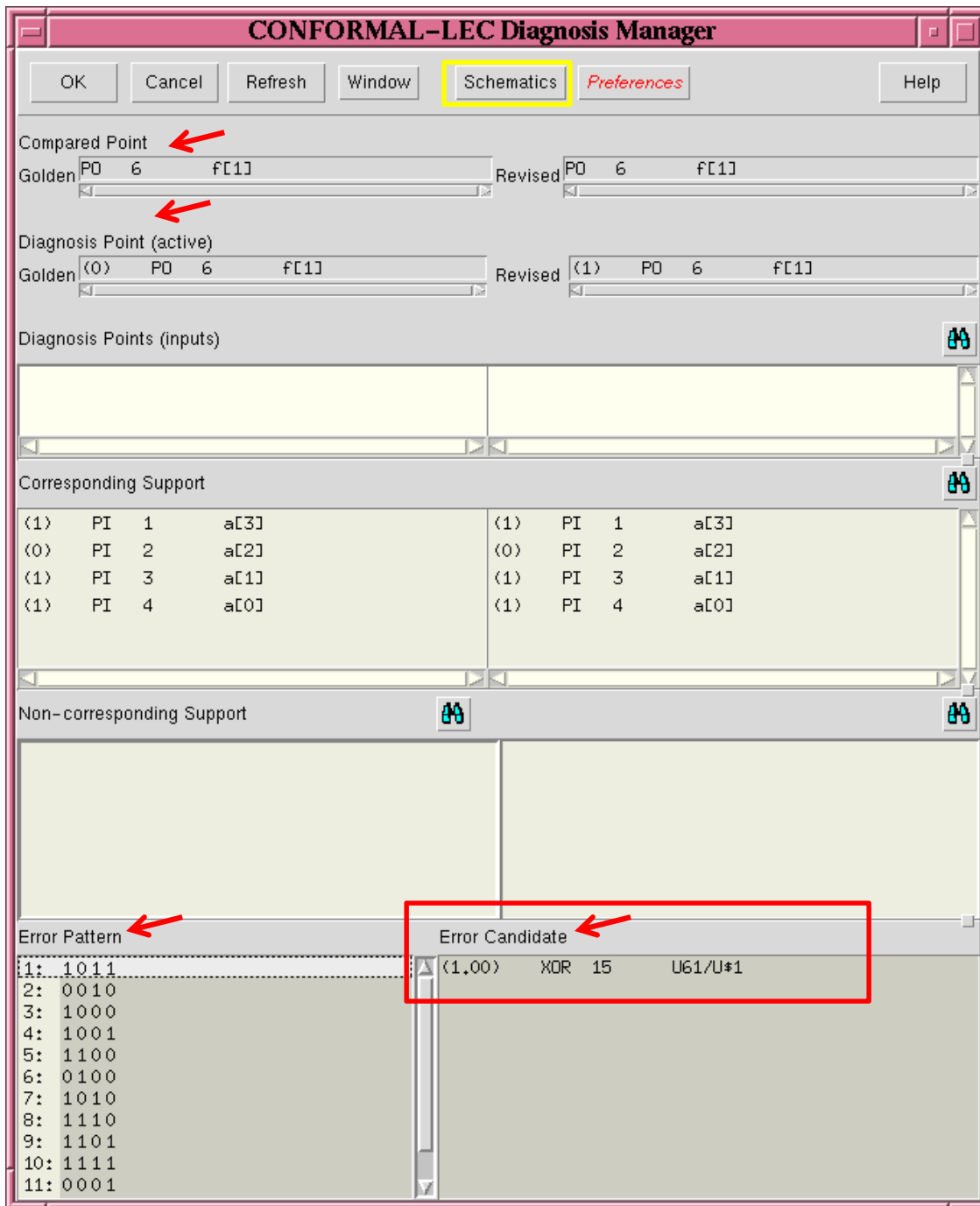
The status bar at the bottom indicates 'Compare done!' and '100% completed'.

1. In the SETUP mode, Load the Golden and Revised Designs
2. Change System Mode to LEC
3. Add all ports as compare points
4. Compare

Report → Mapped Points

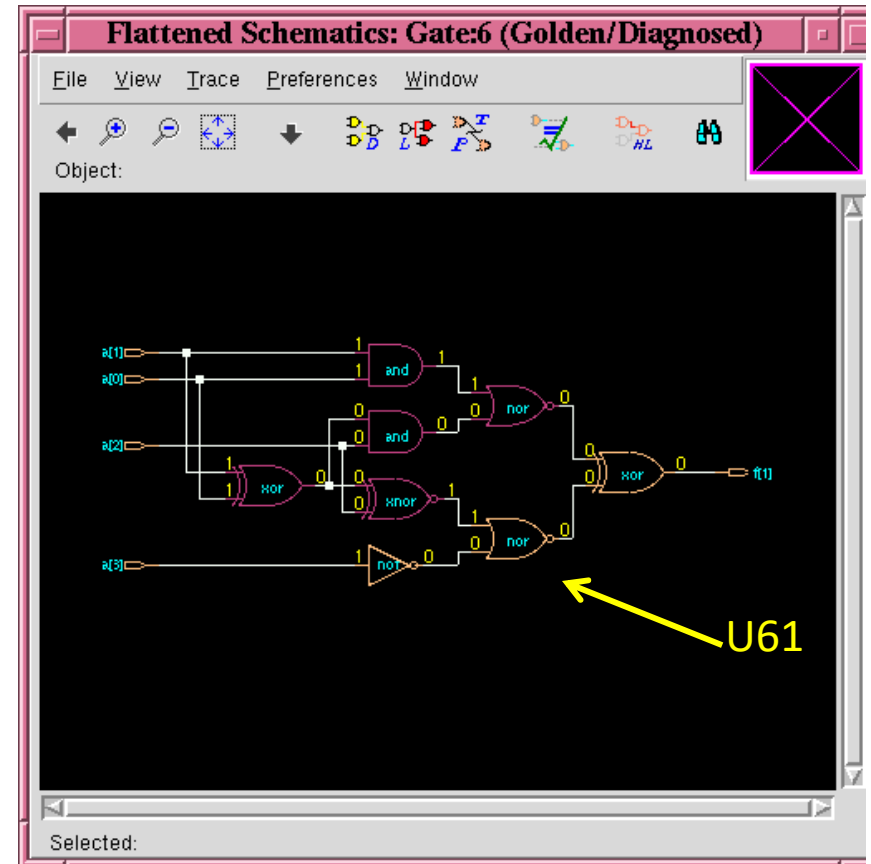
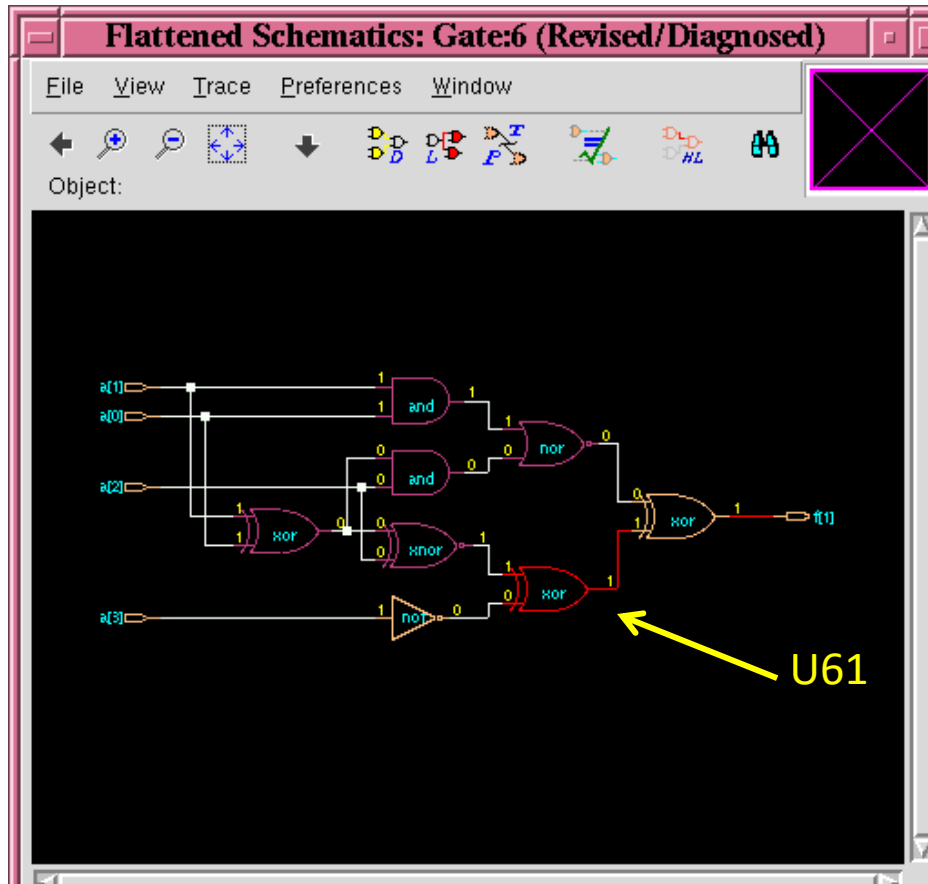
Diagnose →

| Compared Points | Support Size |
|-----------------|---------------|
| ● (+) PO 5 f[2] | (+) PO 5 f[2] |
| ● (+) PO 6 f[1] | (+) PO 6 f[1] |
| ● (+) PO 7 f[0] | (+) PO 7 f[0] |



LEC Diagnosis Manager
Lists the failed compare point

Golden and Revised Schematics



```
48  component IV
49      port( A : in std_logic; Z : out std_logic);
50  end component;
51
52  component A02
53      port( A, B, C, D : in std_logic; Z : out std_logic);
54  end component;
55
56  component EN
57      port( A, B : in std_logic; Z : out std_logic);
58  end component;
59
60  signal n248, n249, n250, n251, n252 : std_logic;
61
62  begin
63
64      U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
65      U60 : EO port map( A => n248, B => n251, Z => f(1));
66      U62 : IV port map( A => a(3), Z => n250);
67  --  U61 : ANDNA2 port map( A => n249, B => n250, Z => n251);
68  --  U61 : NR2 port map( A => n249, B => n250, Z => n251);
69  --  U61 : OR2 port map( A => n249, B => n250, Z => n251);
70  U61 : EO port map( A => n249, B => n250, Z => n251);
71  U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n248);
72  U64 : EO1 port map( A => a(3), B => n249, C => a(3), D => n249, Z => f(0));
73  U65 : EN port map( A => n252, B => a(2), Z => n249);
74  U66 : EO port map( A => a(1), B => a(0), Z => n252);
75
76  end SYN_rtl;
```

Fix the Code and Rerun the Verification