Equivalence Checking Using Cadence Conformal LEC

Formal Hardware Verification

(COEN 7501)

Summer 2010
The Golden and the Revised Designs

```
component EN
    port( A, B : in std_logic; Z : out std_logic);
end component;

signal n248, n249, n250, n251, n252 : std_logic;
begin
    U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
    U60 : E0 port map( A => n249, B => n251, Z => f(1));
    U61 : AND2 port map( A => n249, B => n250, Z => n251);
    U62 : INV port map( A => a(3), Z => n250);
    U63 : AO2 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n251);
    U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n252);
    U65 : EN port map( A => n252, B => a(2), Z => n249);
    U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;
```

signal n248, n249, n250, n251, n252 : std_logic:

begin
    U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
    U60 : E0 port map( A => n248, B => n251, Z => f(1));
    U61 : AND2 port map( A => n249, B => n250, Z => n251);
    U62 : INV port map( A => a(3), Z => n250);
    U63 : AO2 port map( A => a(1), B => a(0), C => n252, D => a(2), Z => n251);
    U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249, Z => n252);
    U65 : EN port map( A => n252, B => a(2), Z => n249);
    U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;
```
1. In the SETUP mode, Load the Golden and Revised Designs
2. Change System Mode to LEC
3. Add all ports as compare points
4. Compare
Report → Mapped Points

CONFORMAL–LEC Mapping Manager

Compared Points

- (+) P0 5 f[2]
- (+) P0 6 f[1]
- (+) P0 7 f[0]

Support Size

- (+) P0 5 f[2]
- (+) P0 6 f[1]
- (+) P0 7 f[0]

Diagnose →
LEC Diagnosis Manager
Lists the failed compare point
Golden and Revised Schematics

[Diagram of electrical schematics with labeled components U61]
Fix the Code and Rerun the Verification