Equivalence Checking Using Cadence Conformal LEC

Formal Hardware Verification
(COEN7501)
Summer 2012
The Golden and the Revised Designs

component EN
    port( A, B : in std_logic; Z : out std_logic);
end component;

signal n248, n249, n250, n251, n252 : std_logic;

begin
    U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
    U60 : E0 port map( A => n248, B => n251, Z => f(1));
    U61 : AND port map( A => n249, B => n250, Z => n251);
    U62 : OR3 port map( A => a(3), B => n250, Z => f(2));
    U63 : A02 port map( A => a(1), B => a(0), Z => n252, D => a(2));
    U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249);
    U65 : EN port map( A => n252, B => a(2), Z => n249);
    U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;

signal n248, n249, n250, n251, n252 : std_logic;

begin
    U59 : OR3 port map( A => n248, B => n249, C => n250, Z => f(2));
    U60 : E0 port map( A => n248, B => n251, Z => f(1));
    U61 : NR2 port map( A => n249, B => n250, Z => n251);
    U62 : IV port map( A => a(3), Z => n250);
    U63 : A02 port map( A => a(1), B => a(0), C => n252, D => a(2));
    U64 : E01 port map( A => a(3), B => n249, C => a(3), D => n249);
    U65 : EN port map( A => n252, B => a(2), Z => n249);
    U66 : E0 port map( A => a(1), B => a(0), Z => n252);
end SYN_rtl;

Revised Design

Golden Design

Conformal LEC: =?  

NO  YES
1. In the SETUP mode, Load the Golden and Revised Designs
2. Change System Mode to LEC
3. Add all ports as compare points
4. Compare

```plaintext
Mapped points: SYSTEM class

<table>
<thead>
<tr>
<th></th>
<th>PI</th>
<th>PO</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Golden</td>
<td>4</td>
<td>3</td>
<td>7</td>
</tr>
<tr>
<td>Revised</td>
<td>4</td>
<td>3</td>
<td>7</td>
</tr>
</tbody>
</table>

LEC> add compared points -all
// Command: add compared points -all
// 3 compared points added to compare list
LEC> compare
// Command: compare

Compared points | PO | Total
----------------|----|-------
Equivalent      | 2  | 2     
Non-equivalent  | 1  | 1     

SETUP> read design /disk/scratch/naem/lec/ones_syn1.vhd -VHDL -Revised
SETUP> set system mode lec
LEC> add compared points -all
LEC> compare
LEC>

Compare done! 100% completed
```
Report → Mapped Points

CONFORMAL–LEC Mapping Manager

Diagnose
LEC Diagnosis Manager
Lists the failed compare point
Golden and Revised Schematics
Fix the Code and Rerun the Verification