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# RTL Modeling of the RCMP Egress Routing Logic

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## Abstract

*In this paper, we present our results on the RTL modeling and simulation of an Egress traffic module, using both VHDL and Verilog. The design considered is a commercial product obtained from PMC-Sierra Inc. and is used by the RCMP (Routing, Cell counting, Monitoring, Policing) process in a network port interface for an ATM switch fabric. The Egress Routing logic of RCMP does header translation of ATM cells and aids multicasting. The behavioral specification of the Egress Routing logic was realized in an RTL VHDL and Verilog implementation. The work also involved the simulation of the RTL VHDL and Verilog models using Synopsys-VSS and Verilog-XL tools respectively. Improper synchronization between the processes leading the system to an indefinite "pause" state was discovered by simulation and later rectified.*

## 1 Introduction

ATM (Asynchronous Transfer Mode) provides a high-speed, low delay, multiplexing and switching network to support user traffic, such as, voice, data and video applications. In an ATM network, the RCMP [3] process both the Ingress and Egress cell traffic in a network port interface for an ATM switching fabric. The RCMP performs the following ATM layer functions: 1) Header translation and cell append for routing, 2) Policing, 3) Cell counting, and 4) Routing for 64K virtual channels. The RCMP also provides cell insert/extract through microprocessor interface and DMA access. Main application areas for the RCMP are in: 1) Edge switches, 2) Enterprise switches, 3) Core switches, and 4) Access Muxes and Residential Broad-band switches. The Egress Routing Logic of RCMP does header translation of ATM cells and aids multicasting, thereby avoids congesting the switch fabric.

This paper particularly deals with the RTL modeling of the Egress Routing Logic of RCMP using both VHDL and Verilog. Simulations were performed on the available Synopsys-VHDL code, first using Synopsys-VSS and then using Verilog-XL on the translated Verilog code. Using a symbolic model checking tool, VIS [1], property checking was also carried out on the Verilog RTL description. This paper proceeds as follows: in Section 2, the behavior of the Egress Routing logic is explained; in Section 3, the VHDL and Verilog implementations are discussed; in Section 4, we present the results of validation of the model and in Section 5, we conclude with the summary of the paper.

## 2 Egress Behavioral Specification

The Egress Routing Logic of RCMP discussed in this paper does only the header translation of ATM cells and does not perform traffic shaping and Resource Management cell insertion. The main function of this block is to route the cell traffic from the output of the RCMP to either the switch or one of the 32 Egress PHYsical ports, and to provide necessary control signals. The Egress Logic supports ATM cell size of 27 to 32 words (16-bit format). A typical Egress application is shown in Figure 1. In this figure, the RCMP is positioned on the Ingress side and the Egress cell traffic coming from the switch fabric are looped back into the input cell interface of the RCMP, which treats these cells as if they are sourced from another PHY port. The master-master logic uses a FIFO (First-In First-Out) buffer which can store and forward cells. This allows both the master interfaces (Switch fabric and the RCMP) to indepen-

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dently control when to write out and read in a cell using write-enable and read-enable signals respectively. The Egress Multi-PHY logic decodes the PHY address to generate the write-enable to the appropriate PHY port.

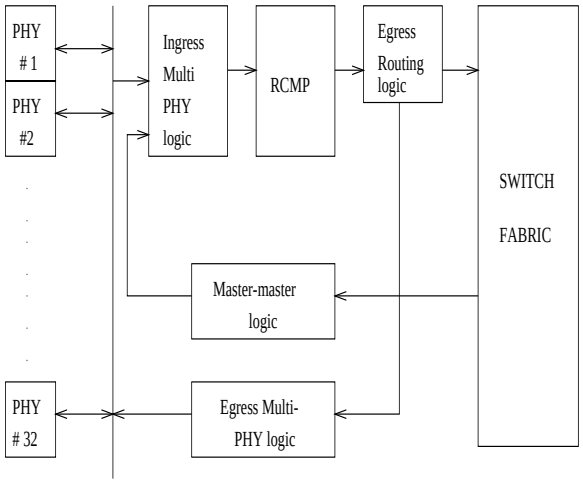


Figure 1: Block Diagram of the RCMP Egress Routing Logic

The RCMP takes care of the extended cell format used in the switch core by removing the appended cell octets and producing 53-octet ATM cells for the PHY layer. This is done by VC (Virtual Channel) table lookup and performing the address translation and multicasting if appropriate. The advantage of multicasting in Egress is that it avoids congesting the switch.

The Egress routing logic performs the routing function by using the first prepend word of a cell, which contains a routing bit that indicates whether the cell should be routed to the switch or back to the Egress direction. It also contains a 5-bit PHY address for the Egress cells. The Egress Multi-PHY logic decodes the PHY address to generate the write-enable signal to the appropriate PHY device. The reason for using the first prepend word is to allow the Egress logic to determine the routing of the cell before the remainder of the cell arrives, thus avoiding the need to buffer the cell.

The Egress Routing Logic should perform the following for every cell transfer [3]:

(1) It asserts the read-enable signal to the RCMP to read out the first prepend word, and then halts the cell read by deasserting the read-enable signal.

(2) It examines the routing bit to connect the control signals from either the Switch or the Egress Multi-PHY logic.

(3) It strips off the prepend word for Egress cells. The prepend word is stripped off to empty this word from the RCMP output FIFO but not actually transferring the data to the destination.

(4) It starts the cell transfer. If the cell is destined to the Switch, the Switch controls the read-enable signal to the RCMP. Otherwise, the Egress logic controls both the read-enable signal to RCMP and the write-enable signal to the PHY ports.

(5) The postpend word is required for other purposes and is not appended to the Egress cells by the RCMP. The Egress logic hence stops the cell transfer without postpend stripping and waits for the cell-availability signal from the RCMP.

The functional behavior of the Egress Routing logic can be represented as a state diagram as shown in Figure 2. In the initial "idle" state, it waits for the cell-available signal from the RCMP. Upon receiving it, it moves to the next state where it reads out the first prepend word from the RCMP. The routing tag contained in the prepend word is decoded and the destination of the cell is determined. If the cell transfer is destined to the switch, it moves to a state where it sets the word-counter to 27 and starts the cell transfer. Simultaneously the word-counter is decremented. After transferring all the words (i.e. word-counter = 0), it returns to "idle" state. If the cell transfer is to a PHY port, then it moves to a state where it waits for the ready-signal from the corresponding PHY port before initiating a similar cell transfer. Once again, after the transfer of the entire cell, the Egress logic returns to the the "idle" state.

The main features of the Egress Routing Logic are as follows [3]:

- Support of Backward Routing of cells from the RCMP output. Decoding the prepend word to determine whether a cell is destined to the switch fabric or one of the PHY devices in the Transmit direction.
- Support of either Direct Multi-PHY interface or Indirect-addressing Multi-PHY interface for up to 32 PHY devices.

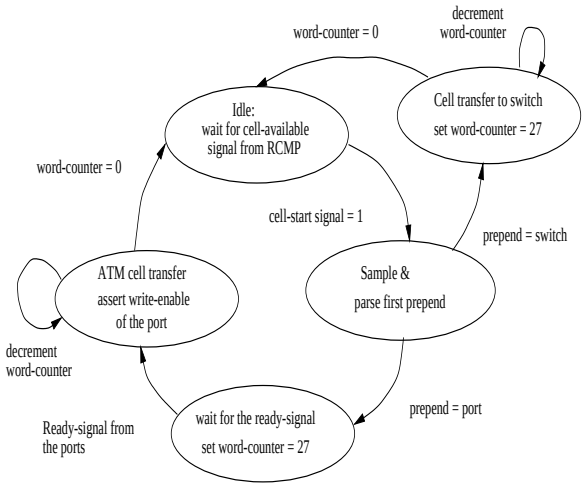


Figure 2: State Diagram Representation of Egress Routing Logic

- Support of cell format with one prepend and 27-words (16-bit wide). Prepend word is stripped off.
- Support of back-pressure flow control (referred as stuttering in following sections) from the switch.

The main assumptions made on the Egress logic are [3]:

- The same clock is used for the PHY interface and the switch interface. This is because the Egress routing logic does not perform synchronization between two different clock domains.
- Both the PHY interface and the Switch interface have the same data bus width (16-bit). This greatly simplifies the Egress Routing Logic.
- This design supports only one prepend. To support more prepend words, the counter initial value can be modified, and the Egress logic simply treats additional prepend words as part of the cell, assuming the first prepend word contains the routing information.
- Both the switch and the RCMP interfaces use cell-based handshake, where the switch can start the cell transfer when there is at least 27 words of space in the FIFO.

## 3 Egress Implementation

We first derived an RTL description of the whole Egress logic in VHDL. The logic was designed using six concurrent processes, doing the functions of output assignment, next-state transition and assignment, state decoding, PHY and switch interface decoding and the word-counting.

The Egress logic was implemented in Verilog in a similar way to that of the RTL VHDL model. The concurrent processes in the VHDL model were implemented using the "always" constructs with the respective sensitivity lists. Blocking assignments statements were used inside each Verilog process which model the sequential execution.

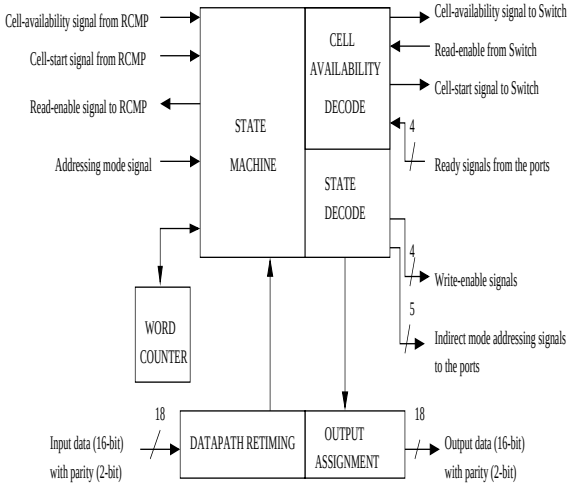


Figure 3: Block Diagram of the VHDL Implementation of the Egress Routing Logic

The block diagram in Figure 3 represents the VHDL implementation. The state machine handles the cell-transfer handshaking. The interface to the RCMP consists of the control signals which flag the cell availability, cell-start and read-enable, including 16-bit data and 2-bit parity. The cell-availability-decode block produces the cell-available signal and cell-start signal to the switch. It also senses the read-enable signal from the switch and the ready-signal from the PHY ports. The state-decode block generates write-enable signals to the four PHY ports and also a 5-bit address for the 32 ports connected through Egress Multi-PHY logic. The RCMP acts as a "slave" interface which receives the read-enable signal while the Switch fabric acts as a "master" sourcing the read-enable. The output data and the parity are connected to both the Switch and the PHY devices. The datapath retiming and output assignment block takes care of the transfer of input data to the output at the appropriate clock cycle by providing internal buffering.

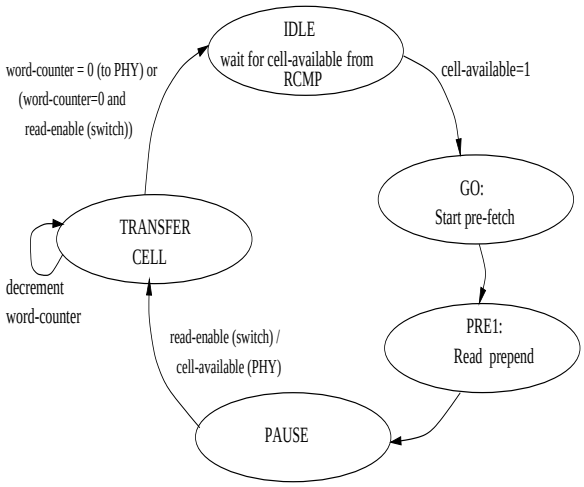


Figure 4: State Diagram of the VHDL Model

The state diagram in Figure 4 represents the sequence of operations of the state machine of the VHDL model for the Egress Routing Logic. The state machine starts off in the IDLE state, waiting for the cell-availability signal from the RCMP. Once the signal is sampled high, it reads out the prepend word and decodes the backward-routing tag in the next two states viz. the GO and PRE1 states. It then samples either the ready signal from the PHY devices or the read-enable signal from the switch according to the routing tag in the PAUSE state. Upon receiving either of the signals, it starts the cell transfer and once all the 27 words have been transferred, it resets itself to the IDLE state once again. The two modes of operation will be explained in the following subsections. Detailed timing specifications of these operation modes are given in [3].

### 3.1 Direct-mode Operation

In this operation mode, cell transfer occurs in the Egress direction to the four PHY devices connected directly to Egress Multi-PHY logic. With the cell-availability indication from RCMP in the first clock cycle, the Egress logic reads out the first prepend word within the next two clock cycles. The Routing tag is decoded in the next two clock cycles which indicate that the cell is destined to one of the four PHY devices. It waits for the corresponding PHY device to assert its cell-availability signal. If it is asserted, the read-enable signal continues to be asserted, and the rest of the cell is transferred to the device, by asserting the corresponding write-enable signal of the device. Otherwise, the read-enable signal is deasserted and remains in the wait state itself. After every cell transfer, the cell-availability signal from the RCMP is resampled and the word-counter is reseted.

### 3.2 Indirect-mode Operation

In the indirect addressing mode, up to 32 PHY devices can be interfaced with Egress Multi-PHY logic. It is identical to the direct mode operation. Only difference is that, instead of the write-enable signals, 5-bit PHY address is used to choose the devices. The PHY device samples this 5-bit address and the selected PHY device asserts the cell-availability signal in the next clock cycle. The cell-availability signals from the 32 PHY devices are multiplexed as only one signal is sampled by the Egress Logic. The remaining sequence of events for the cell transfer is identical to the direct mode operation.

At the Switch interface, after the decoding of the prepend word the Egress logic asserts the cell-availability signal and waits for the read-enable signal from the Switch fabric. With its assertion, the control is directly transferred to the Switch and the rest of the ATM cell is transferred. At any time during the cell transfer, the switch can deassert the read-enable signal to pause the transfer and resume it at a later time. The cell count will stop decrementing until the read-enable signal is asserted again. When the switch deasserts just after the first word or just after the last word, an internal buffering mechanism called stuttering is used which holds the data till the switch is ready again to read. This is done by sampling the input and output data in stuttering situation. The stuttering mechanism is only provided for the first and last words of a cell transfer in switch mode.

## 4 Egress Routing Model Validation

Simulation using Synopsys-VSS was carried out on the VHDL design by constructing test benches for each mode of operation. The Egress module was instantiated inside a test module and the test vectors were applied according to the timing diagram specification given in [3] for each mode of operation. For example, the cell-start signal is made synchronous with the first word in the output data. The stuttering mechanism is also taken care off by making it to appear only in the first and last word of cell transfer. In all the modes of operation, the parity bits were initialized to zero while inputting the data. The system entered irreversible "pause" state as the concurrent processes

were not able to detect the changes occurring in the inputs due to improper synchronization between them. With proper modification, the simulation results conformed to the timing diagram specifications [3]. The validation by simulation was also established against the timing diagrams using Verilog-XL on the translated Verilog code.

As a further validation step, the concurrent Verilog model was converted into BLIF (Berkeley Logic Interchange Format)-synthesizable Verilog set and symbolic model checking was carried out using VIS (Verification Interacting with Synthesis) tool [1]. The behavior of the module was expressed in CTL (Computational Tree Logic) properties comprising liveness and safety properties [1]. We were able to detect the design same error with property checking using VIS, where VIS produced the corresponding error trace. Interested readers can refer to [2] for more details on the functional verification of the RCMP Egress routing logic.

## 5 Conclusions

In this paper, we designed the RCMP Egress routing logic as an RTL model using both VHDL and Verilog. The model consist of six blocks, viz. State-machine, State-decode, Cell-availability-decode, Datapath-retiming, Output-assignment and Word-counter blocks. The Egress logic operated in two modes of operation, viz. Direct mode, in which the logic can be interfaced to 4 PHY ports and Indirect mode, in which it can be interfaced to 32 PHY ports.

The VHDL and Verilog models were simulated using Synopsys-VSS and Verilog-XL tools, respectively, by constructing appropriate test benches for different modes of operation. A design error which violated the timing diagram specifications and could lead the system to a indefinite "pause" state was detected and rectified. The obtained results can be corroborated further by carrying out sequential equivalence checking between a synthesized Verilog model and the behavioral Verilog model in VIS.

### Acknowledgments

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