

Hardware Modeling and Verification of an ATM Ring MAC Protocol

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Abstract— In this paper, we describe the modeling and verification of the register transfer level (RTL) design of an ATM ring (ATMR) media access control (MAC) protocol using a hardware verification model checking tool, VIS. We succeeded verifying a synchronous as well as an asynchronous design alternative of this MAC. Throughout the verification, we report the performance of hardware protocol verification in model checking, and discuss some modeling techniques we adopted in the verification.

I. INTRODUCTION

The VLSI design of finite-state concurrent hardware systems is today present in many fields, in particular in the design of digital and communication systems. Late detection of design errors in the design phase are very costly in any system development. These errors can delay the product deployment and even cause the failure of the product. The traditionally used simulation techniques cannot cover all design errors when the state space of the system is big. During the past years, model checking techniques [7] have established themselves as significant means for early detection of hardware design errors due to their ability of validation and conformance checking.

Generally, when a protocol is implemented in VLSI, it is difficult to be handled by a software (protocol) verification tool. The latter ones are based on an interleaving model and cannot reflect the synchronous concurrency aspects of a hardware implementation.

The aim of this paper is to describe the modeling and formal verification in VIS (Verification Interacting with Synthesis) [1] of the RTL hardware implementation of a single ATM ring (ATMR) MAC protocol [3]. A number of related work can be found in the open literature. These can be classified in three major categories: (1) formal verification of high layer software protocols [5]; (2) formal verification of synchronous hardware protocol [8]; and (3) formal verification of ATM hardware devices [6]. Our work distinguishes itself from these related publications by the fact that we verify the Verilog RTL hardware implementation of an asynchronous MAC. We present some techniques on how to simulate the asynchronous ATMR MAC design in a synchronous environment and also propose some abstraction and reduction approaches for the aimed verification. Furthermore, we analyze the performance of the source of the complexity in the verification with respect to the CPU time, memory usage and state space.

The rest of the paper is structured as follows. The next section introduces the ATMR MAC to be verified. Section 3 discusses the modeling techniques we used for the asynchronous MAC. Section 4 describes the verification of the

asynchronous and synchronous MAC hardware implementation against a set of CTL consistency properties. Section 5 finally concludes the paper.

II. A TMR MEDIA ACCESS CONTROL PROTOCOL

The ATMR MAC [3] is a new ISO standard based on a high speed shared medium bus connecting a number of access nodes by channels in a ring form. Figure 1 gives an example ring with five nodes connected via a channel transferring cells between the nodes. For controlling access

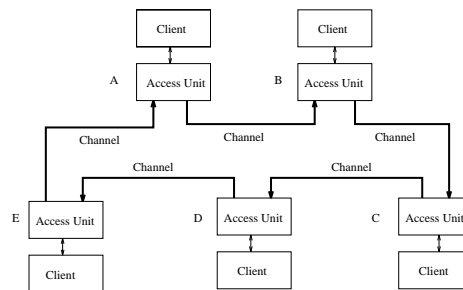


Fig. 1. A TMR structure with 5 nodes

to this type of shared medium, the ring is first initialized with a fixed number of ATM cells continuously circulating around the channel from one node to another. Within each access node there is an access unit which performs both the physical layer convergence function and the access control function. Access to the ring is requested by the client and controlled by a combination of a window mechanism and a reset procedure. The client can issue a sending request to the access unit and receive a data cell. The window mechanism limits the number of cells a node can transmit at a time, called the “credits” of this node. The reset procedure reinitializes the window in all access units to a predefined credit value. The format of an ATMR cell is shown in Figure 2. It contains an access control

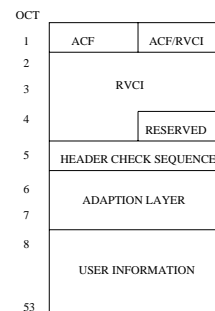


Fig. 2. Format of an ATMR cell

