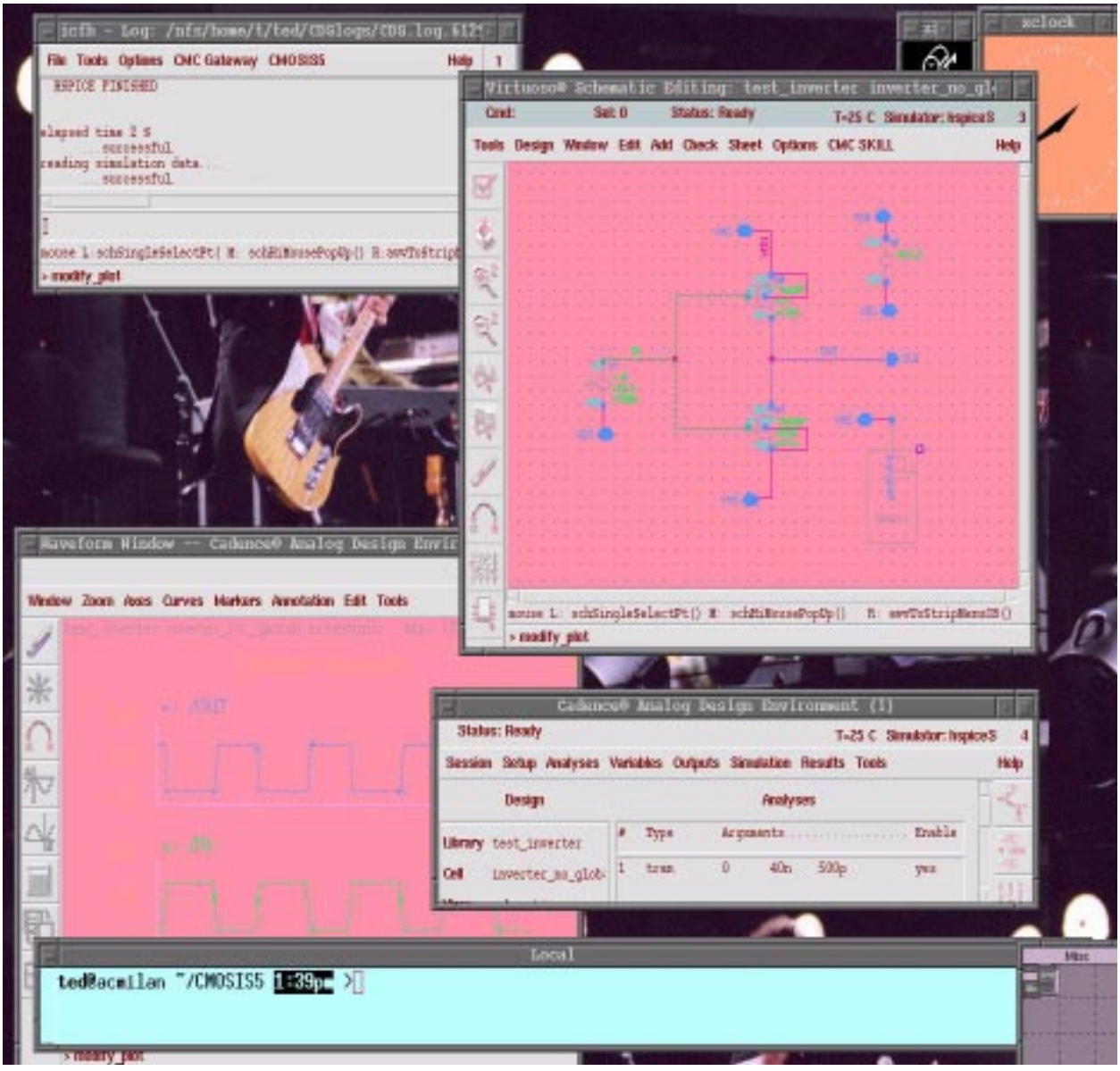
A Tutorial on Using the Cadence® Schematic Editor and Analog Environment to Create and Simulate a CMOS Inverter at the Transistor Level using CMOSIS5 Technology



Developed by
Ted Obuchowicz
VLSI/CAD Specialist, Dept. of Electrical and Computer Engineering
Concordia University

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Revision History

January 4, 2001: updated file naming conventions for naming libraries.

Sept. 4, 2003: updated to reflect the fact that the HPICE netlister in Cadence 2002a does no longer extract global VDD! and VSS! pins. Consequently, schematics must NOT make use of global (i.e. VDD! and VSS!) pins.

May 17, 2006: updated for Cadence 2004a, updated circuit diagrams to use VDD and VSS pins, updated inverter symbol to include external VDD and VSS pins (instead of using implicit globals)

INTRODUCTION

This tutorial is an introduction to the Schematic Editor and the Analog Artist simulation tools available from the Cadence package. The tutorial is based on Cadence 2004a using the CMOSIS5 technology. This is a 0.5 micron CMOS process from Hewlett-Packard. This tutorial will show how to use the Schematic Editor to create a schematic diagram (of a CMOS inverter), perform a simulation of the circuit using the Analog Artist Simulation tool, and create a Hspice netlist from the circuit diagram which can then be later simulated using Hspice and as a standalone tool.

EXAMPLE 1:Inverter Circuit from Schematic Editor.

I: USING THE COMPOSER SCHEMATIC EDITOR

In this section you will learn how to create a schematic view of the CMOS inverter design shown in Figure 1.

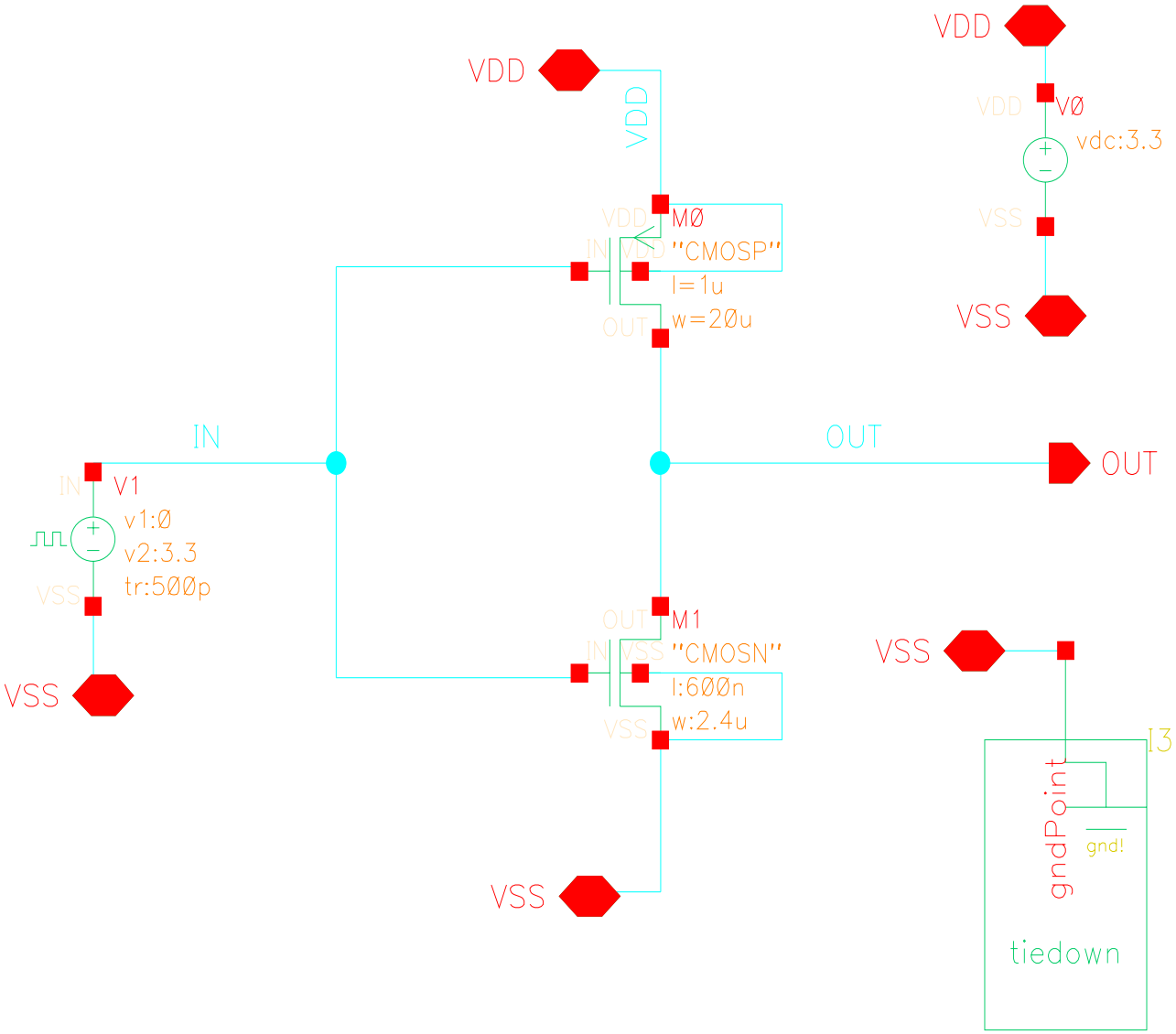

Figure 1: CMOS Inverter Schematic.

I: Creating the Schematic diagram for the inverter circuit.

1-1. Log in to a Unix terminal in Room H915 (or where you were given access to).

1-2. Create a working directory to store your files in.

```
% mkdir Test1
% cd Test1
```

Note: the % symbol refers to the UNIX prompt; it is not part of the command.

1-3. Start the Cadence software by issuing the following command from the UNIX prompt:

% cmosis5

This will create the following files in the working directory:

cds.lib icchspice.init

and will open up the CIW window shown in Figure 2. From this window, one may create a new library and design, open an existing library and design, invoke the Library Manager to edit libraries and designs (select Tools -> Library Manager). The first step is to create a new library which will be used to hold your work. This library must be attached to the technology being used, which in this case is the CMOSIS5 design kit made available by the Canadian Microelectronics Corporation.

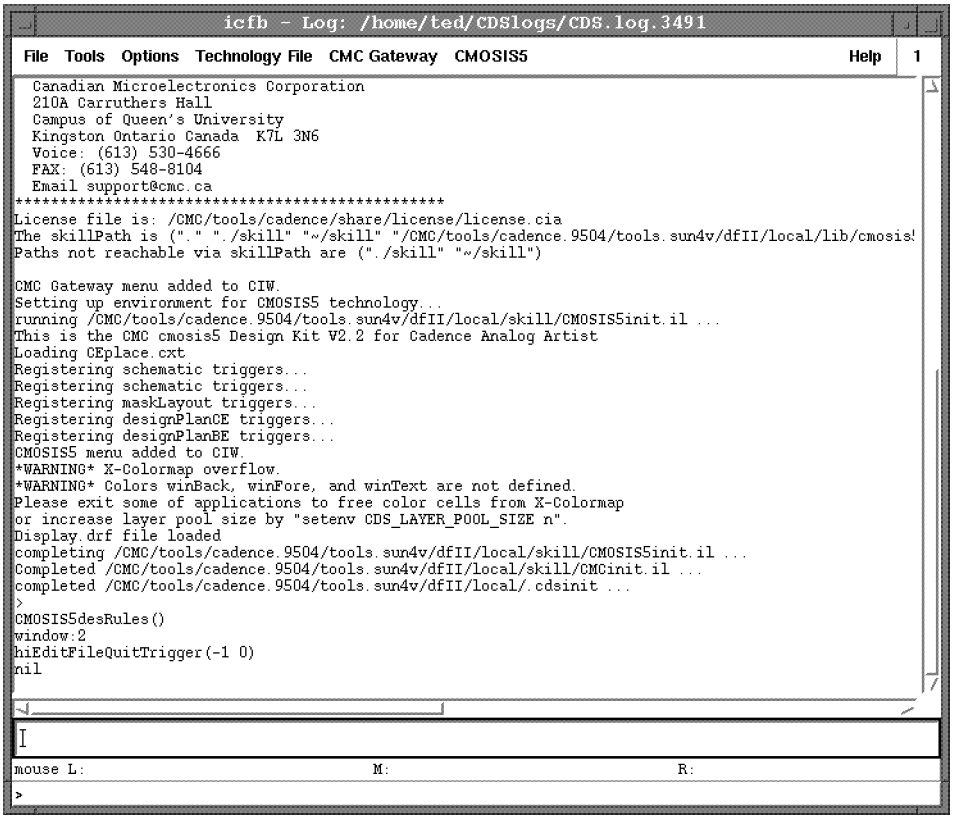

Figure 2: CIW window.

1-4. Left click with the mouse on the File option, this will bring up a popup menu with the following choices:

New
Open
Import
Export
Refresh
Make Read Only
What's New
Exit

Left click on New, another sub menu will appear:

New ----------> Library
(left click) Cell View

Left clicking on the Library choice will cause the New Library window (see Figure 3) to appear. In the New Library window form fill in the following choices:

Name: test_inverter (any suitable name for the library in which you will store your design in, use only conventional UNIX filenames. **It must begin with a letter, not a number!!!**).

In the portion of the form relating to Technology File, select the "Attach to an existing techfile" choice.

Leave the Design Manager as the default selected No Dm. Select OK.

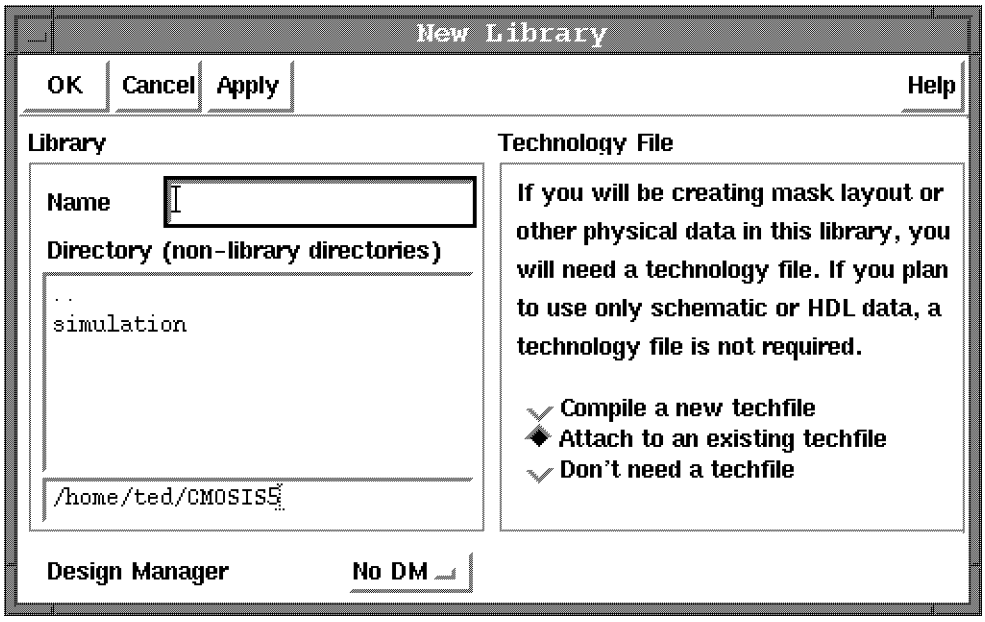

Figure 3: The New Library window.

1-5. To create a new cell, select File ---> New ----> Cell View from the CIW window (The main window that Cadence opens up when you invoke the cmosis5 script).

This will open the Create New File window (see Figure 4):

Library Name: Click on this button to select from a list of possible libraries, from the list which appears select the library you created in the above steps of this procedure.

Cell Name: in this area you enter the name of your cell, for example circ1.

View Name: Analog Artist works with a hierarchy of views : schematic, symbol, layout, extracted. For this example we will be working with the schematic view. NOTE: USE ONLY LOWER CASE LETTERS FOR THESE VIEW NAMES.

Tool: In order to draw the schematic diagram, we need to use the Composer - Schematic tool. click on this button and select Composer-Schematic from the list of possible tools.

Once you have filled in all the information in the Create New File window, click on the OK button at the top left of the window.

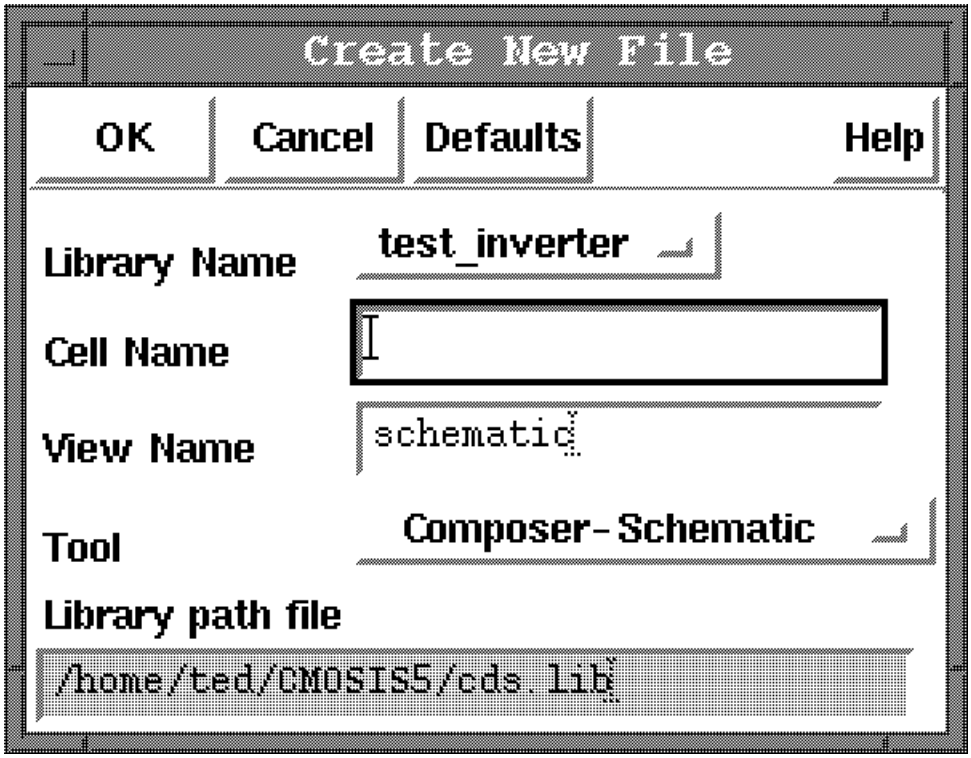

Figure 4: The Create New File Window.

1.6. The Composer-Schematic window will appear on your screen (see Figure 5). You will create your schematic circuit diagram in this window. The first step you may want to do is to change the default Snap Spacing. This determines the resolution that you can place your mouse cursor. In order to line up your circuit symbols you want to make the Snap Spacing half of the Grid spacing. To change the Snap Spacing click on :

Design ------> Options -----> Grid

In the Grid Options window, enter the desired Snap Spacing (make it equal to half the value of the Grid Spacing will allow you to locate components in the center of two grid points) and click on Apply followed by OK.

Figure 5: Composer Schematic Window.

1.7 You may now start to enter components. Click on the Add choice in the top of the Composer-Schematic window, followed by clicking on Component:

Add -----> Instance

Clicking on the Instancet button will cause the Add Instance window to appear (see Figure 6).

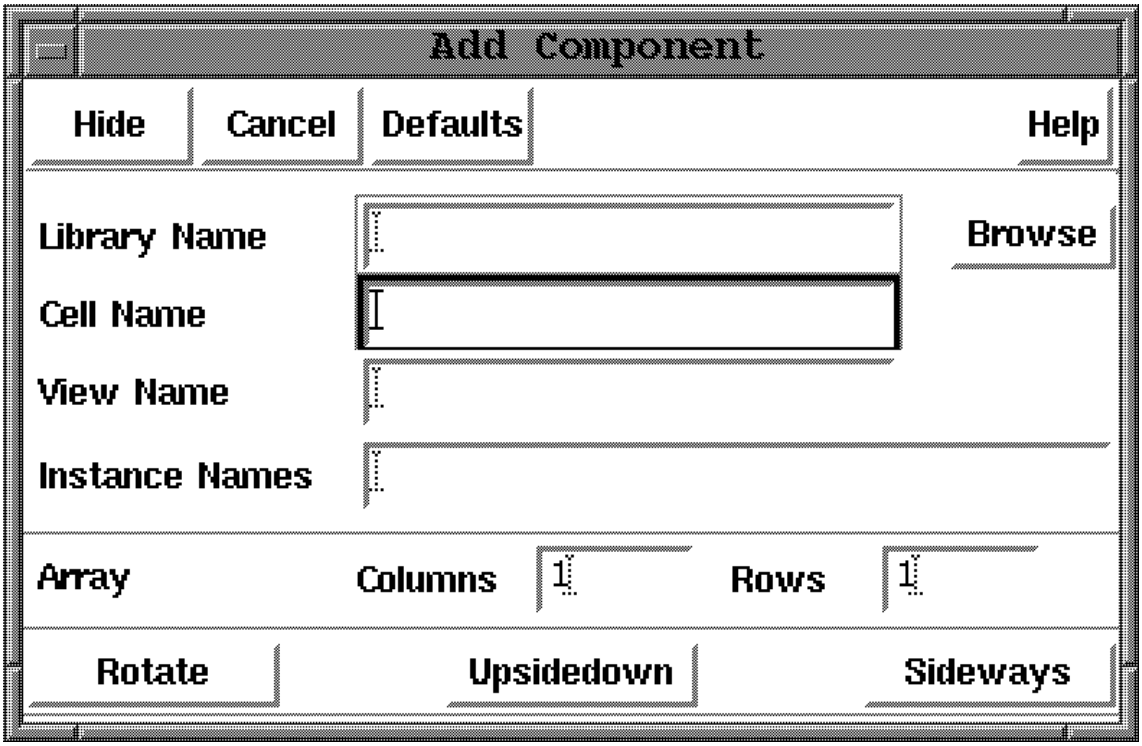

Figure 6: Add Component Window.

Click on the Browse button, the Library Browser window will appear (see Figure 7). From this window select the cmosis5 library from the list of available libraries. The cmosis5 library is a library of components such as nmos and pmos transistors, resistors, capacitors, etc.

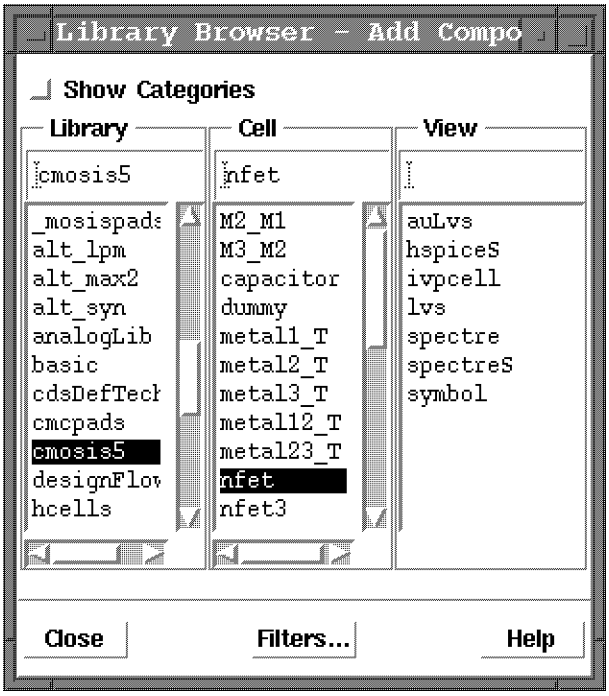

Figure 7: The Library Browser Window.

Each column has associated scrollbars, use the scrollbars to select cmosis5 from the Library column, pfet from the Cell column and symbol from the view column. Notice that now the Add component window has changed (see Figure 8) and it includes a portion in which you can specify several parameters for the component. Change the W and L parameters to suitable values (such as W= 20u M and L = 1u M) . Click Hide, the Add Component window will disappear from the screen and attached to the cursor will be a symbol for a 4 terminal ptype FET. Move the cursor to where you wish to place the transistor and left click. If you no longer wish to place any more instances of this transistor gate pressing the Escape key will clear the selected component from the cursor.

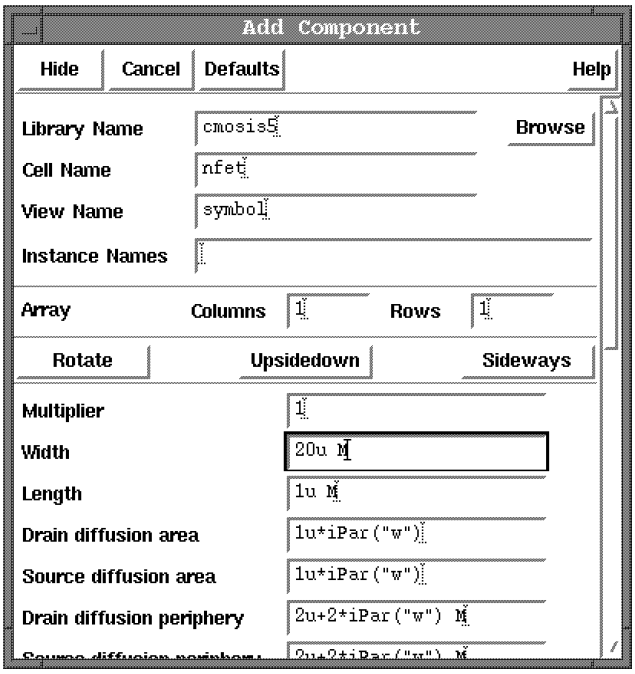

Figure 8: The Add Component Window with Fields to specify component parameters.

1-8. Repeat the above step, this time selecting nfet as the cell from the cmosis5 library. Place the nfet below the pfet then press Esc to stop adding instances of this selected cell.

Refer to Figure 1 as a guide to where the place the components.

AT THIS POINT, IT IS A WISE IDEA TO SAVE YOUR WORK. SELECT DESIGN ----> CHECK AND SAVE. You will probably receive some notice that your drawing has warnings in it.

Warnings and errors are reported in the CIW window and highlighted in yellow in your schematic diagram. Ignore any warnings for the time being, as we have not yet completed the drawing. SAVE YOUR WORK OFTEN and EARLY.

1-9. The next step is to join the two drains of the transistors together with wire. Select Add ---> Wire(narrow). The Add wire window will appear, leave the settings as they are and click the Hide button to lower this window and to allow continuation of the wire drawing step.

Move the cursor the drain of the pfet (the lower terminal) and left click, this will define the starting location of the wire, then move the cursor to the drain (upper terminal) of the nfet and left click again. This will define the ending point for the wire. The wire is first shown in yellow as you are defining its starting and ending points; it will change to its final color of blue once the path

is completely defined.

Repeat the above steps to add the other wires as shown in Figure 1.

1-10. Add an output pin to the output of the inverter circuit. Select Add ---> Pin and fill in the Pin Name field as OUT and set the pin's direction as output in the Add Pin window (see Figure 9).

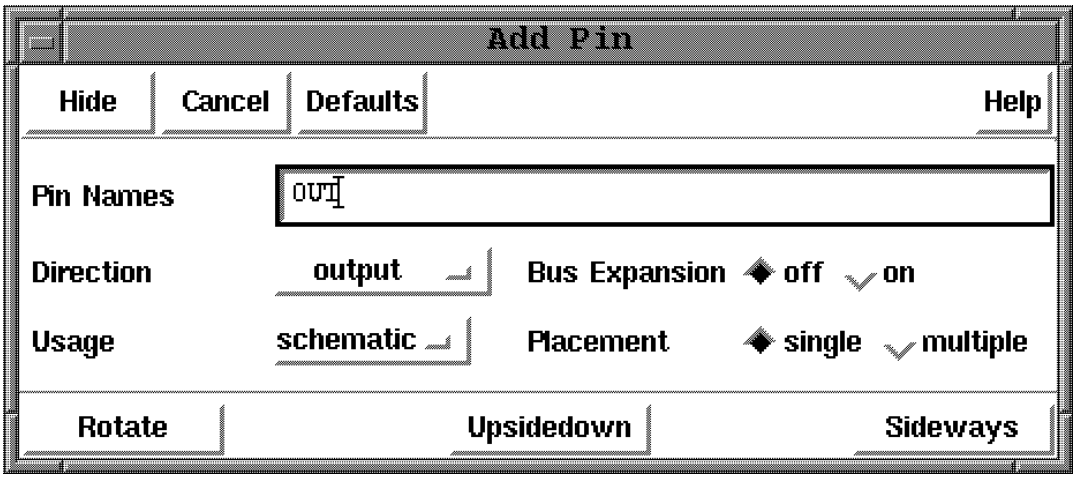

Figure 9: The Add Pin Window.

1-11. Add instances of a vpulse, vdc, and a tiedown from the cmosis5 library. You can edit the parameters of the vpulse to define suitable values for the pulse period and pulse duration.

1-12. Notice that the connections from the inverter to the power supply and ground point are made through pins called **VDD** and **VSS.** Connected to the positive terminal of the vdc component is a VDD pin. The dc power supply's negative terminal is connected to a VSS pin. The source of the pfet is connected to a VDD pin and the source of the nfet is connected to a VSS pin. The negative terminal of the vpulse component is connected to a VSS pin. Note that a ground point is established by connecting a VSS pin to the terminal of the tiedown component. The circuit behaves as if there are individual wires connecting all the VDD pins together and all the VSS pins together, but it is not necessary to actually draw these wires. To add a VDD pin, select ADD ---> Pin and select VDD as the pin name and inputoutput as the direction. A VSS pin is created in a similar manner. Alternatively, one may add only a VDD and a VSS pin to the vdc component and connect the appropriate nodes of the schematic to these two pins with wires.

1-13. This step is optional. We can name the wire segments connecting the vpulse to the inverter's input terminal and the output terminal to the output pin. This step is not necessary, but could make debugging the netlist easier, as well as allowing quick identification of the nodes in the netlist.

Select Add ---> Wire name

In the Add Wire Name window give the Name as IN and click Hide.

Attached to the cursor will be the name you selected and a small square: move this square to anywhere along the wire segment between the vpulse and the inverter's input and left click.

Repeat the procedure to name the output wire OUT.

1-13: Save and check your work:

Design ----> Check and Save

1-14: To obtain a print out of your circuit diagram:

Design ----> Plot -----> Submit (click here to open up submit plot window).

Turn off the Plot With # header # notes # index sheets #grid/axes in the Submit Plot window (see Figure 10) then click on the Plot Options in the extreme bottom right hand corner of the window (it may be necessary to move the window to the top of the screen in order to see the entire form).

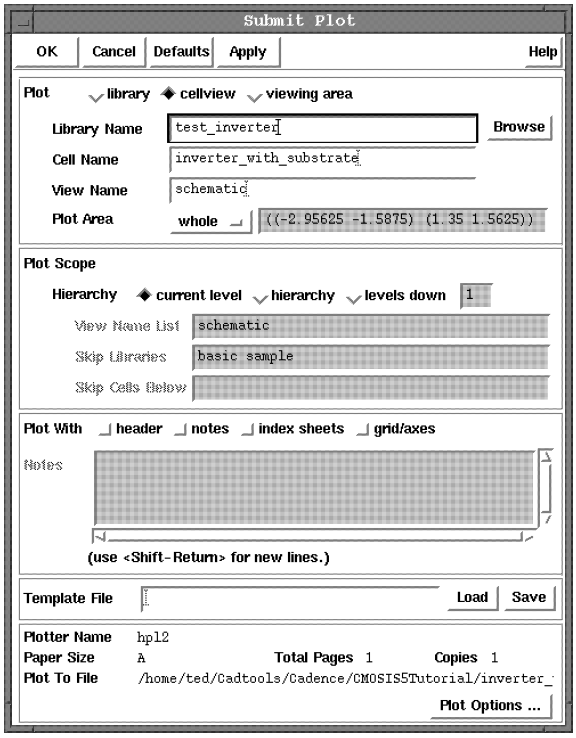

Figure 10: Submit Plot Window.

In the Plot Options window (see Figure 11):

Click on the Send Plot Only to file and specify the file name (for example circ1.ps) Turn off the Mail Log To selection (if this option is not off then you will receive mail informing yourself that you created a plot).

Click on OK. The file you specified as the Send Plot Only to file will be saved in your working directory.

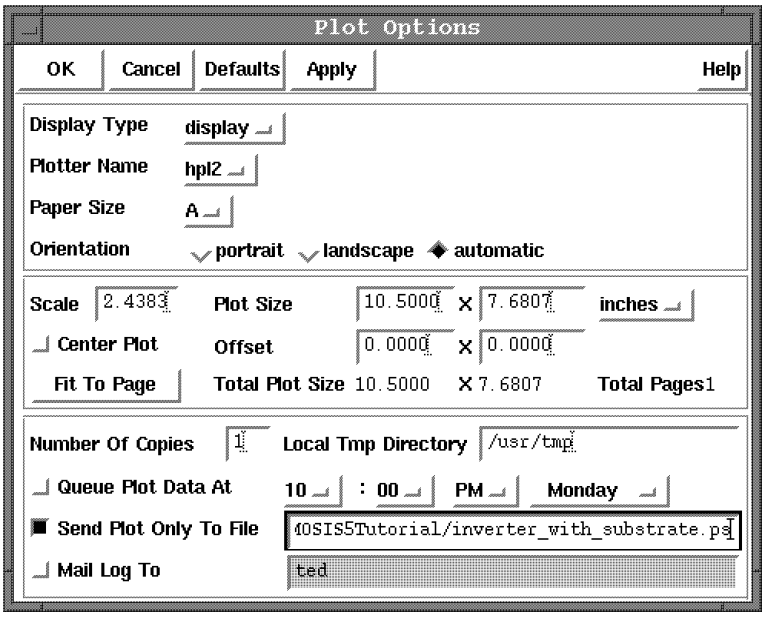

Figure 11: Plot Options Window.

You can PREVIEW the plot using ghostview: from a UNIX window in the working directory (the one you started the cmosis5 command from) type

% ghostview circ1.ps

If your plot is correct, you can print it using the lpr command

% lpr -Phpl2 circ1.ps

II: RUNNING THE ANALOG ARTIST SIMULATION

Now that we have constructed our test circuit, we are ready to run the simulation and observe the results. Prior to doing so, a few preliminary setup steps are required.

2-1. From the Composer-Schematic window select Tools ----> Analog Environment. The Analog Environment Simulation window will appear as shown in Figure 12. Select Setup ---> Simulator/ Directory/Host.

The Choosing Simulator/directory/host window will appear, from this window select the desired simulator to use to perform your simulation (see Figure 13). In this example, the chosen simulator

is hspiceS. Click on the OK button in this window.

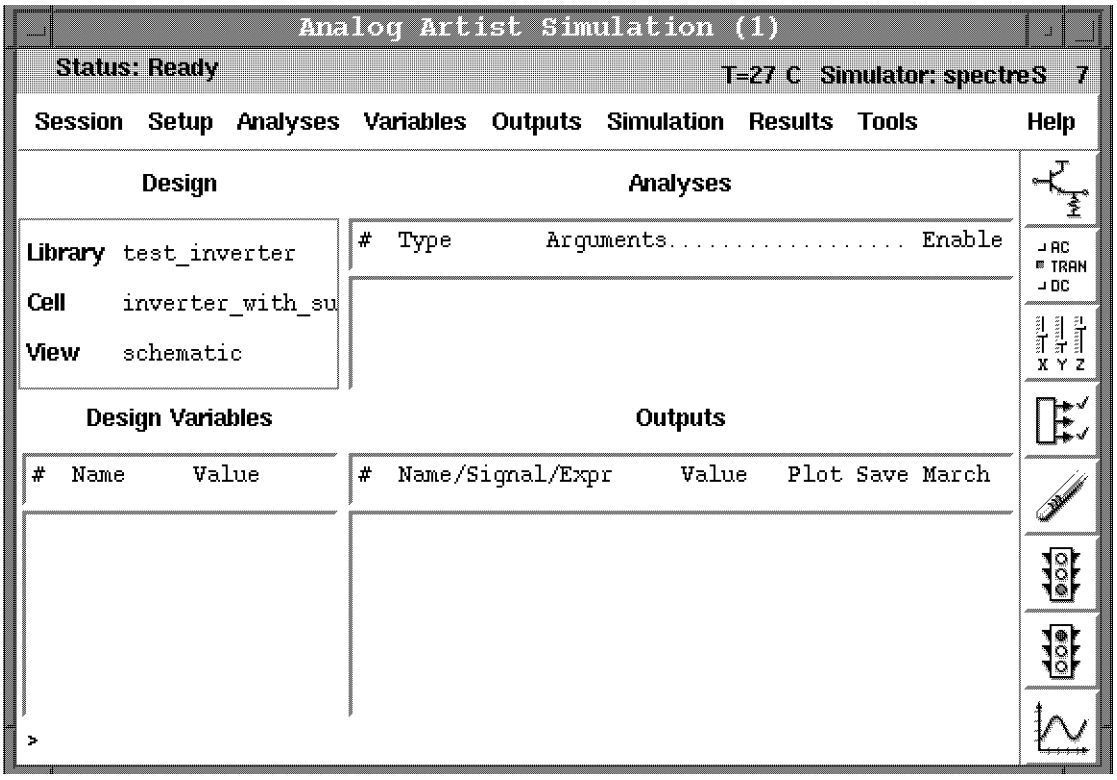

Figure 12: Analog Artist Simulation Window.

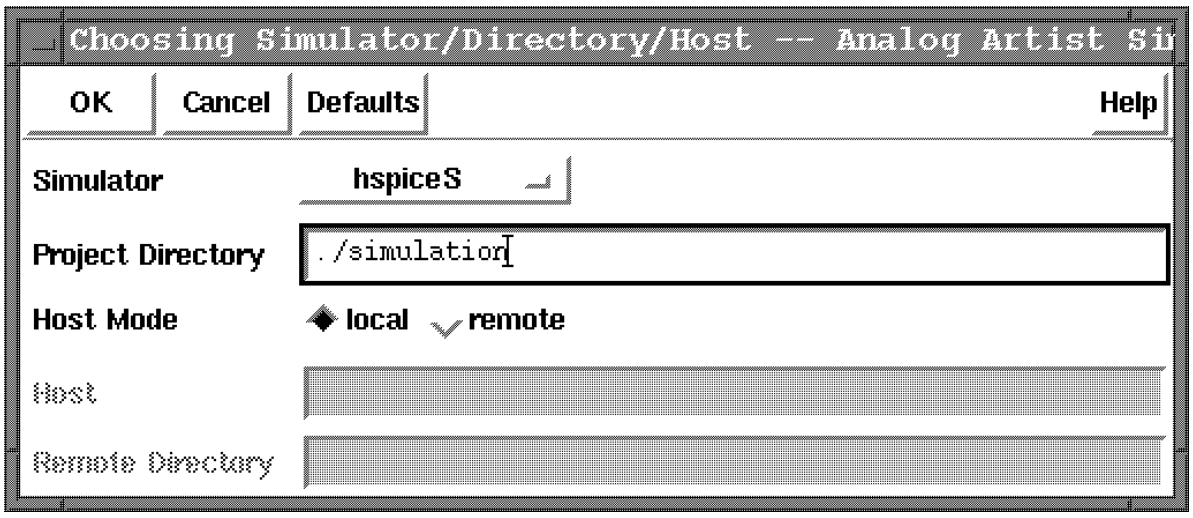

Figure 13: Choosing Simulator/Directory/Host window.

2-2. From the Analog Artist Simulation window select Setup ----> Environment. Make sure that hspice is selected as the Include/Stimulus File Syntax. Next, enter ./icchspice.init as the Include File at the bottom of the form (see Figure 14).. Click on OK.

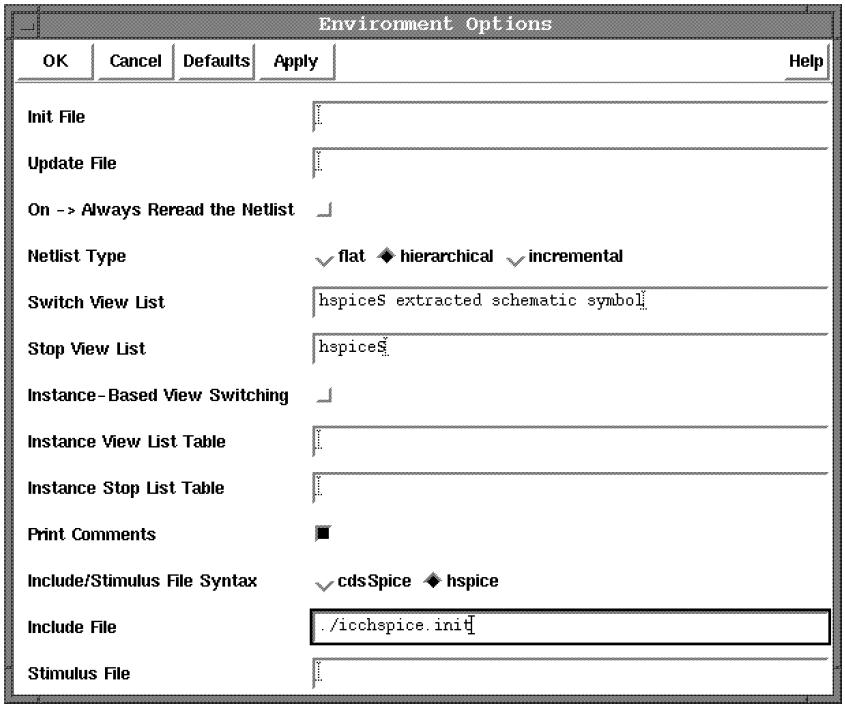

Figure 14: Environment Options window.

2-3. From the Analog Artist Simulation window, select Analyses ---> Choose ---> and set the type of analysis required (see Figure 15). For the purposes of this tutorial, a transient (tran) analysis will be performed. Set the From field to 0 and the To field as 60n, set the By field to 20p. This sets the start time to 0 seconds, the stop time to 60 nanoseconds with a time step of 20 picoseconds. Click Ok.

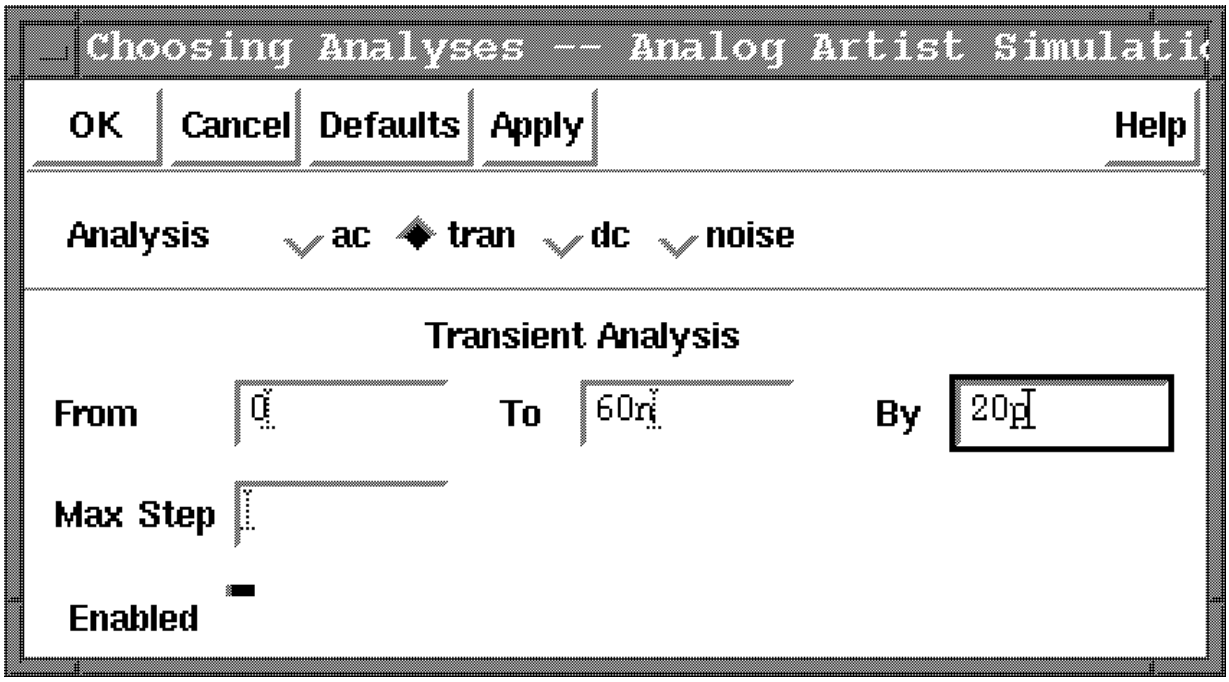

Figure 15: Choosing analysis window.

2-4. Select Outputs ----> To be Saved -----> Select on Schematic and then select the wires you wish to save the current values associated with in your schematic diagram. That is, go to the Schematic Editor window and click on the wires labelled IN and OUT.

NOTE; click on wires to plot node voltages, click on the square red pins associated with a component to plot the CURRENT.

As you select the pins, you will note that the pin names will appear in the Outputs section of the Simulation window (see Figure 16).

2-5. Select Outputs ----> To be Plotted ---> Select on Schematic and then click on the wires in your circuit diagram corresponding to the node voltages you want to have displayed in your simulation results. As you select the wires, they should change to a dotted pattern on your circuit diagram and the names IN OUT should be added to the list in the Outputs section of the simulation window.

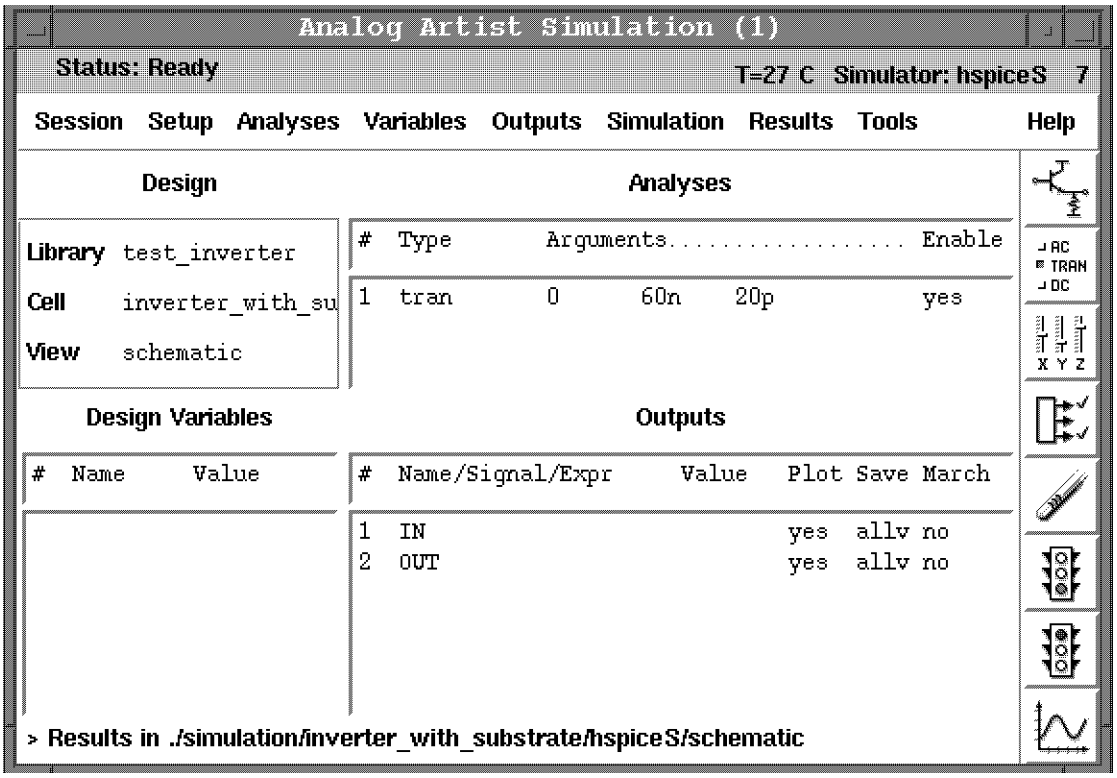

Figure 16: Outputs to be saved and plotted.

2-6. Select Simulation ----> Run to start the simulation. If there are no errors, a window with the simulation results will appear (see Figure 17). You can display the results on separate axes by selecting Axes ---> To Strip. Use Simulation -----> Output log from the Analog Artist Simulation window if the CIW window reports any errors during the simulation.

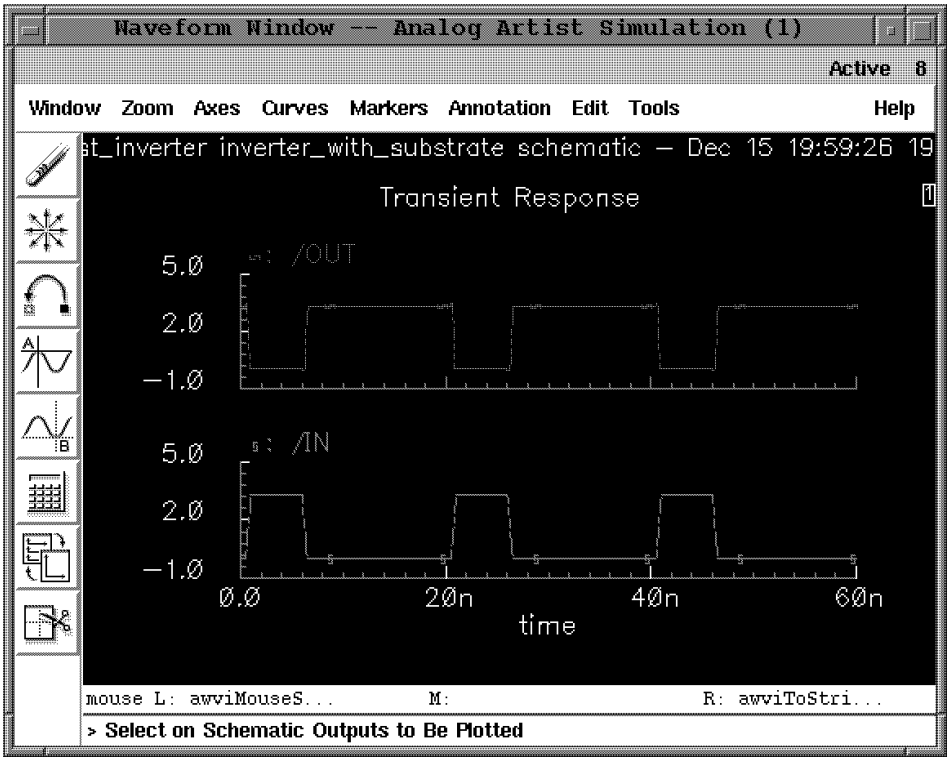

Figure 17: Waveform window.

2-7. To obtain a hardcopy printout of your simulation results, select Window ----> Hardcopy a Hard Copy window will appear. Turn off the Plot with # Header options, select Send Plot only to File and give a file name such as test1result.ps, turn off the Mail Log to options. Click Ok.

PRINTING YOUR SAVED POSTSCRIPT FILES:

Once you have printed your diagrams, results, etc to files you can print them by going to your working directory and issuing the lpr command from the UNIX prompt.

% lpr -Phpl2 circ1.ps
% lpr -Phpl2 test1.ps

etc.. for all your other files you want printed. IT IS ADVISABLE to first preview your file using ghostview before printing it to the laser printer, as you have a fixed amount of print quota. The command to use ghostview is:

% ghostview file_name

III: EXTRACTING A HSPICE NETLIST FOR STANDALONE SIMULATION

3-1. If you wish to extract a hspice netlist from your drawn circuit to be used as an input file to the standalone hspice simulator, select Simulation ----> Netlist ----> Create Final from the Analog Artist Simulation window after having performed the SetUp, Environment, Choosing Analysis, Selecting Outputs To Be Saved/Plotted steps. A window with the hspice netlist file will appear (see Figure 18). Select File ----> Save As and give this file a name such as mynetlist.sp.

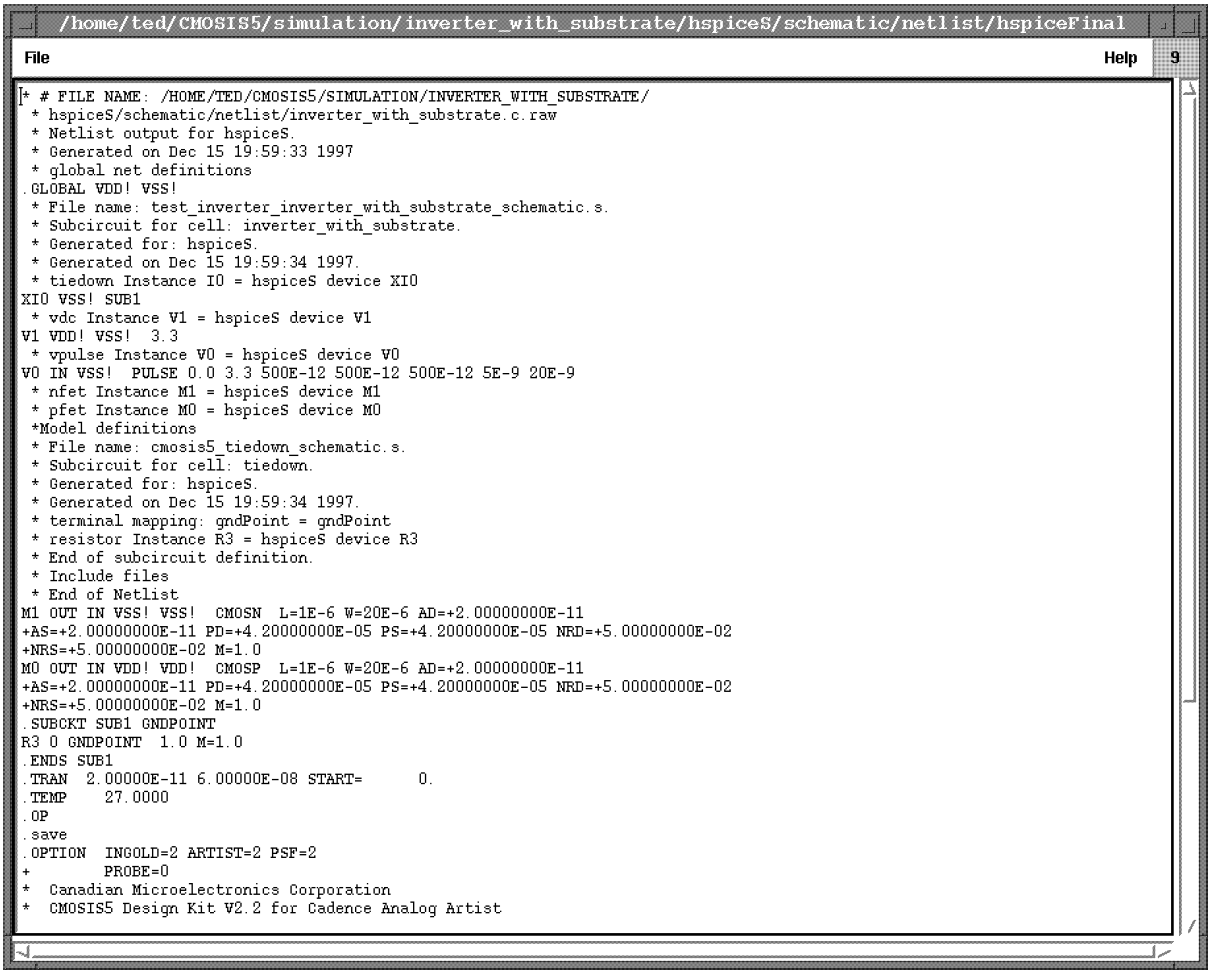

Figure 18: File Window containing Hspice netlist.

3-2. The netlist file create must be edited to allow processing by the hspice simulator. Use the editor to change the lines:

```
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+        PROBE=0
```

To read as:

```
.OPTIONS LIST NODE POST
.PRINT TRAN V(IN) V(OUT)
```

NOTE: the nodes IN and OUT will only appear if you performed the optional step of naming your wires in your circuit diagram. Otherwise, you must search the hspice netlist to identify the node labels generated during netlist extraction and use these node labels instead of IN and OUT in the PRINT tran statement.

3-3. Run the hspice simulator:

% hspice mynetlist.sp > mynetlist.lis

3-4. Run the Awaves tools to display the simulation results as described in the document “A Tutorial on Using Hspice and Awaves as a Standalone Tool”.

EXAMPLE 2: CREATING A SYMBOL.

In this example, a *symbol* for a CMOS inverter circuit will be created. This symbol will then be used to create another schematic diagram to which an input stimulus and power supply will be connected to. This will define a *testbench* for simulation purposes. The use of symbols can make the task of creating complex circuits simpler. One may design a circuit building block at the transistor level (a NAND gate for example), once a symbol has been created it may be used in other circuits.

I: USING THE COMPOSER SCHEMATIC EDITOR.

1-1. Open a new file from the CIW window. You can use the same library you created in Example 1. Choose a suitable cell name and select Schematic as the view name.

1-2. Use Figure 19 to create a circuit diagram consisting of an nmos transistor and a pmos transistor from the cmosis5 library, symbol view. Add an instance of an input pin named IN and an OUTPUT pin named OUT connected to the input and output terminals of the inverter. Add a VDD pin and connect it to the source of the pmos transistor. Connect a VSS pin to the source terminal of the nmos transistor. Add wire names IN and OUT if so desired.

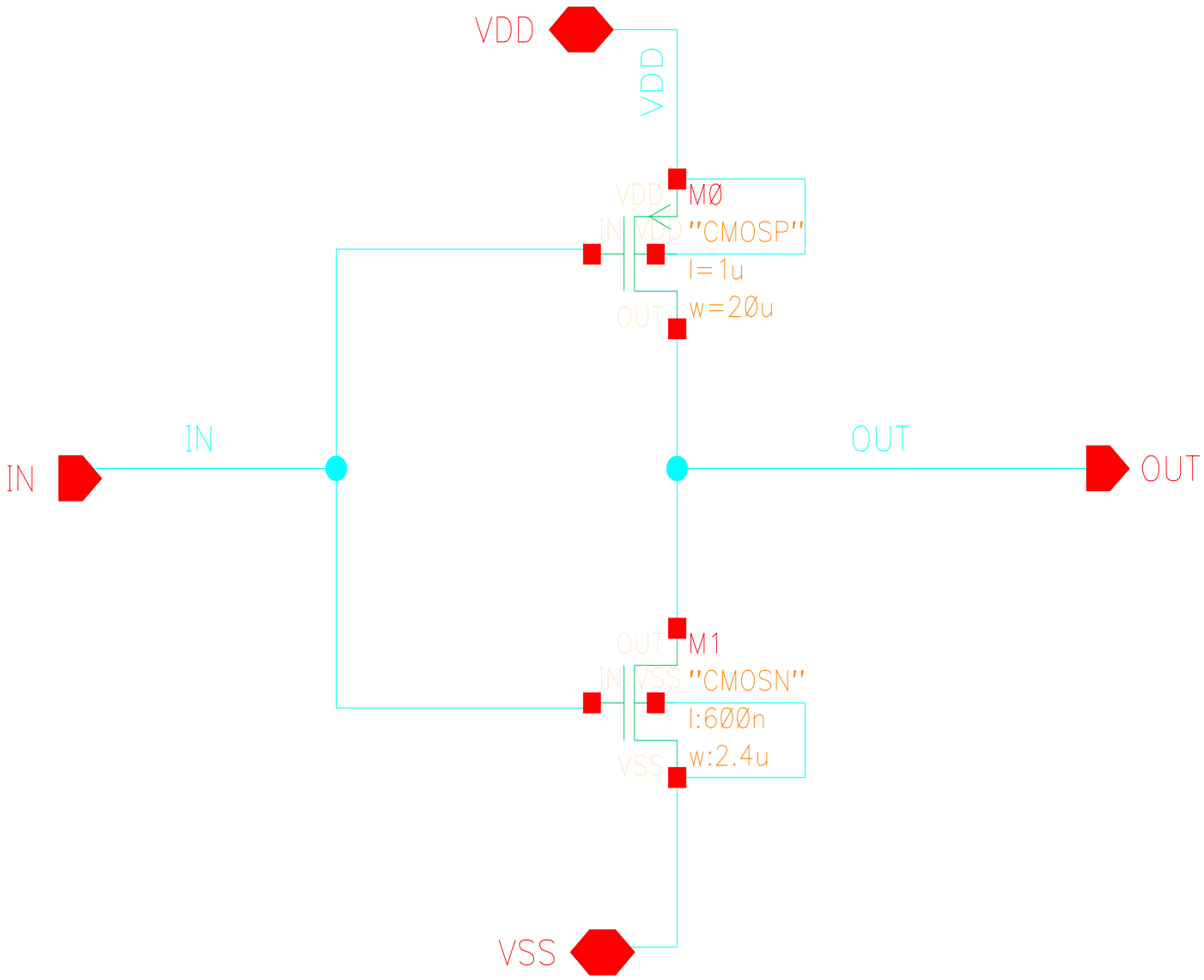

Figure 19: CMOS Inverter circuit used to create a symbol.

1-3. Select Design ---> Check and Save.

II: CREATING A SYMBOL FOR THE INVERTER.

2-1 Select Design ---> Create Cellview ---> From Cellview to create a symbol for the inverter. The Cellview from Cellview window will appear (Figure 20). Ensure that the From view name is set as schematic and the To View name is set as symbol. Click on OK.

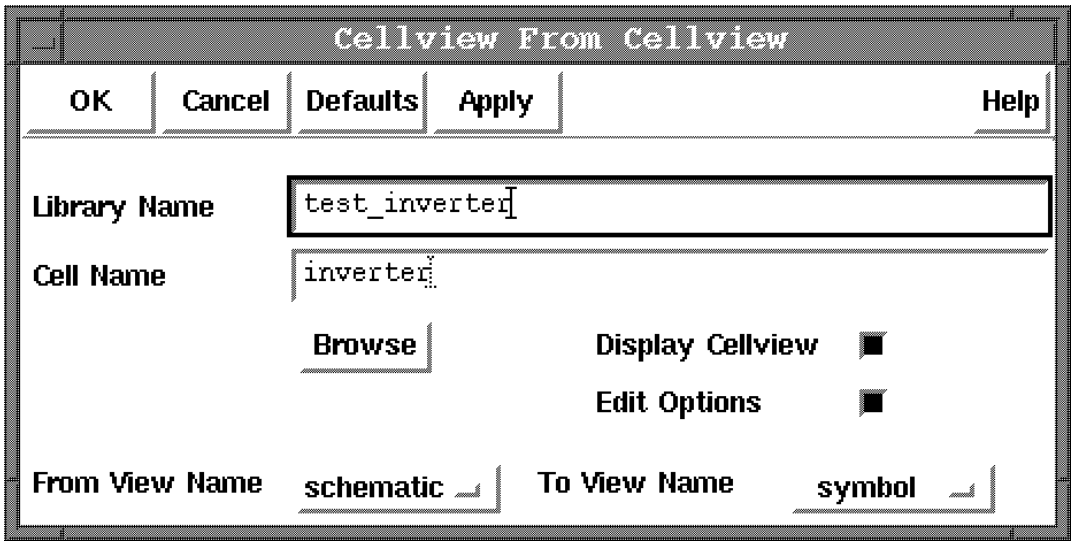

Figure 20: Create Cellview window.

2-2. A Symbol Generation Options window (Figure 21) will appear giving the names and types of any pins in your schematic diagram. Click OK to generate a symbol for your circuit.

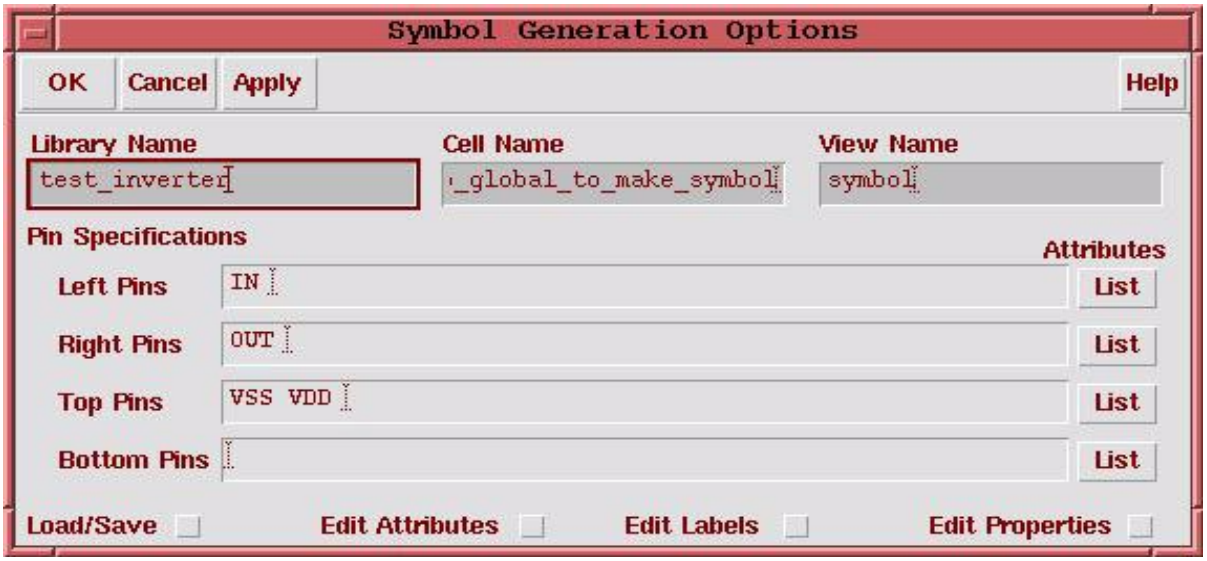

Figure 21: Symbol Generation Options window.

2-3. A new Composer-Symbol window will appear containing a rectangle with pin names IN and OUT with [@partName] in the centre of the rectangle and [@instanceName] in the upper right hand corner. There will also be two pins with names VDD and VSS at the top.This is the symbol

representation for the inverter circuit. Refer to Figure 22.

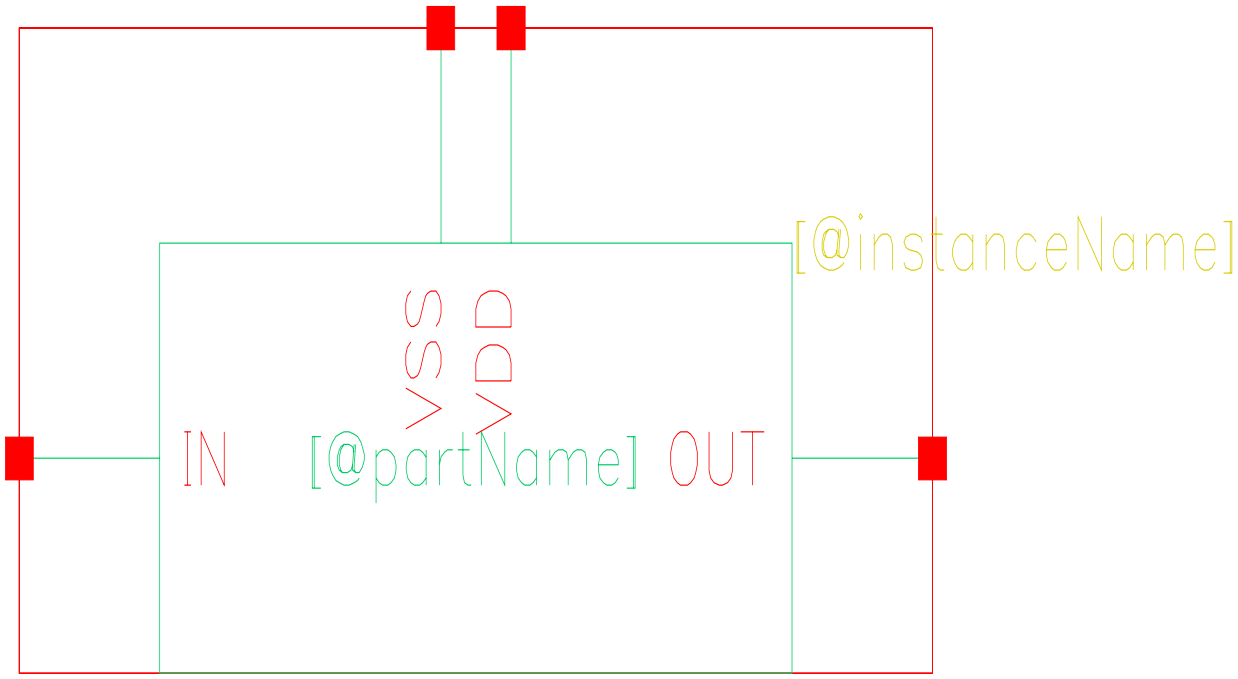

Figure 22: Symbol View of Inverter Circuit.

2-4. The next step is to create a new schematic using the symbol created in Step 2-3 and sources from the cmosis5 library for the input stimulus (vpulse), a power supply (vdc), a tiedown to establish the circuit ground point and VDD and VSS pins. Refer to Figure 23 for the details

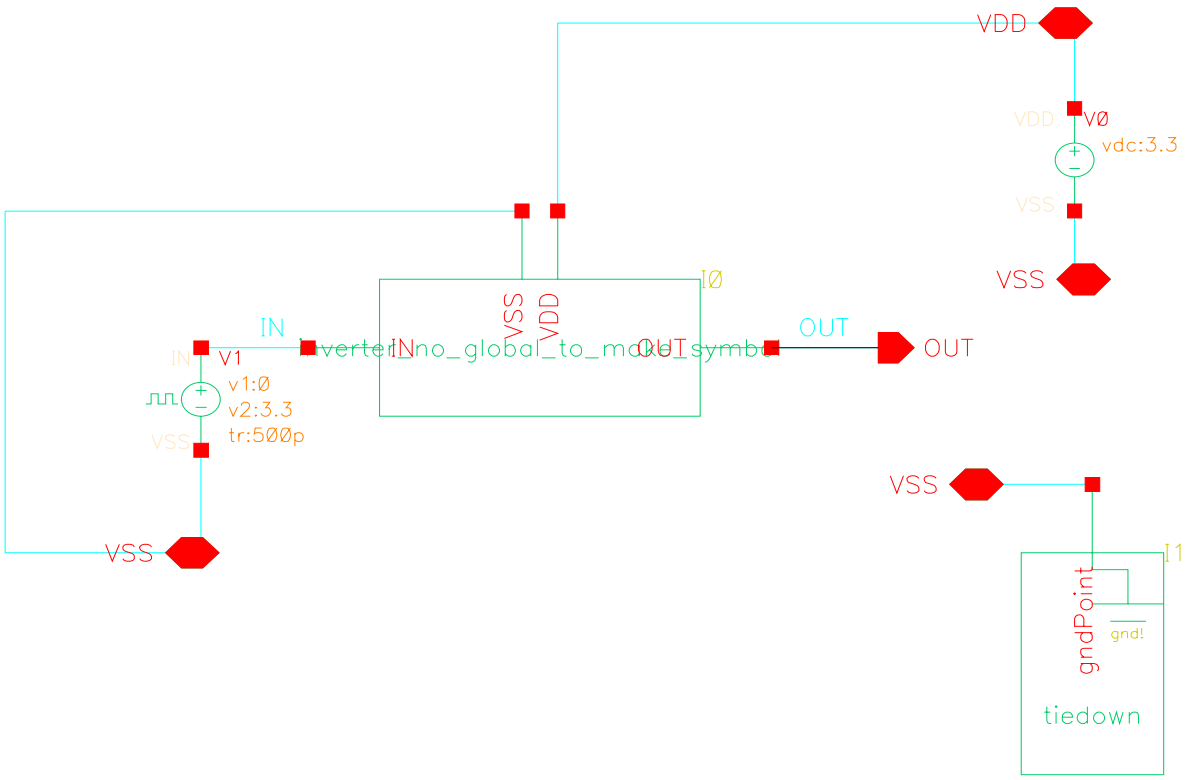

Figure 23: Test Circuit with Inverter Symbol.

EXITING FROM CADENCE

Before logging off from the terminal you are running Cadence from, make sure you exit from the application. From the main CIW window, select File ---> Exit. You will be prompted if you want to save the current design session. Select Cancel to exit. Merely logging off without first exiting is not sufficient; as Cadence continues to execute in the background using CPU resources and degrading network performance.

III: Simulating the Circuit.

3-1. The same procedure which was outlined in Example 2 Section III can be used to simulate the circuit containing the symbol.

EXAMPLE 3: OBTAINING A DC TRANSFER CHARACTERISTIC WITH A TEMPERATURE SWEEP.

In some cases, one is interested in obtaining the V(out) versus V(in) characteristics of an inverter circuit. Such a graph is called the ***DC transfer characteristic*** and can be easily obtained as outlined in this example. This example also illustrates the use of a SWEEP statement within a HSPICE netlist. By sweeping a particular parameter (i.e temperature) one may obtain a family of curves; each curve representing the data for a particular value of the sweep variable.

3-1: Create a new cellview, with View set to Schematic. Add instances of your inverter symbol, a Vdc source connected to VDD and VSS pins, a tiedown connected to a VSS pin, and another Vdc source connected to the inverter's input. Add also an output pin called OUT. Connect the instances together with wires and name the wires IN and OUT. Refer to Figure 24 for the details of this circuit . NOTE: the voltage source connected to the inverter's input terminal is a DC source, rather than a pulse source. We will be varying this DC source's voltage from 0 to 3.3 volts and plotting the corresponding value of the output voltage; thereby obtaining the DC transfer characteristic.

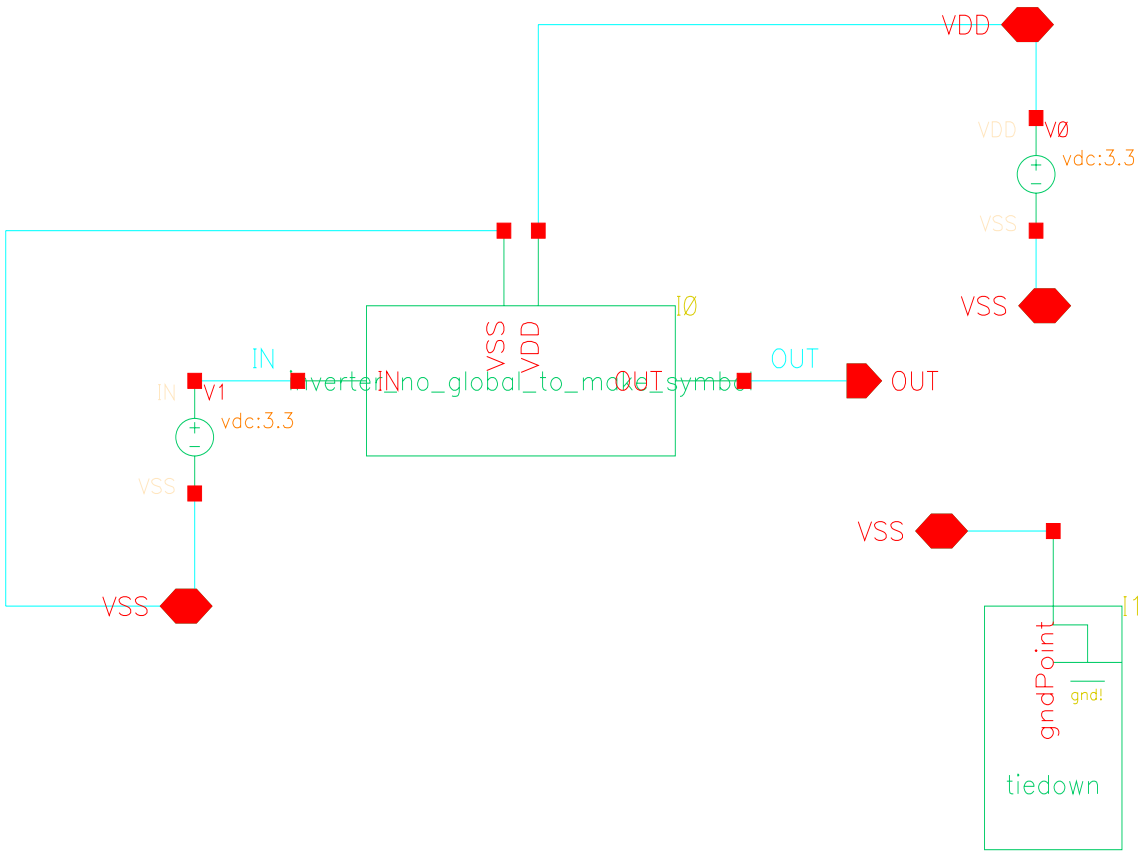

Figure 24: Inverter circuit with a DC input source used to obtain a DC Transfer Characteristic.

3-2: Save your current design. Select **Design -> Check and save**.
3-3: Invoke the Analog Artist simulation tool. Select **Tools -> Analog Environment**.
3-3: From the Analog Artist simulation window, select **Setup -> Simulator/Directory/Host/...** and in the Choosing Simulator/Directory/Host window select **hspiceS** as the simulator and click OK. Click No in the Do you want to Save Current State query window which will appear.

3-4: Select **Setup -> Environment** and in the Environment Options form click the **hspice** button in the Include/Stimulus file Syntax choice, and enter as the Include file **./icchspice.init** .

3-5: Select **Analyses -> Choose** and in the Choosing Analyses form select **dc** as the Analysis, enter 0 in the From field and 3.3 in the To field, and 0.1 as the By entry. Click the **Select Source** button and move the cursor and left click on the dc source which is the inverter's input source. Refer to Figure 25.

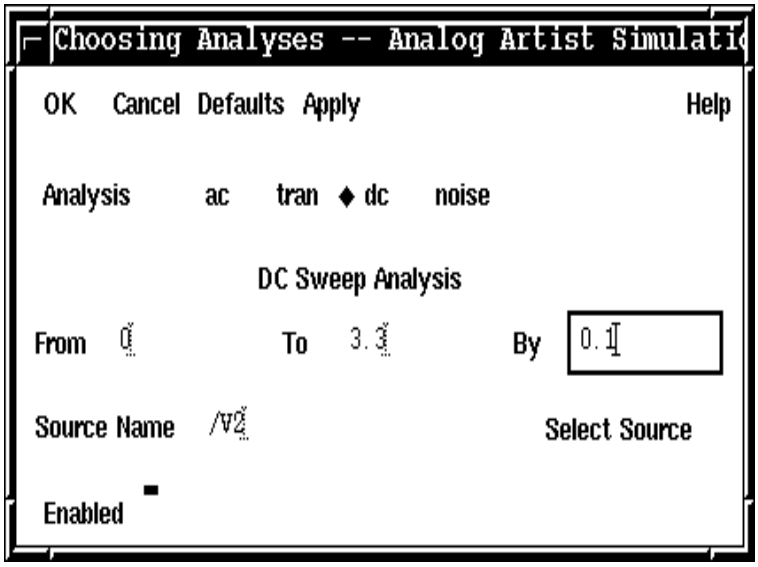

Figure 25: Setting the DC analysis parameters.

3-6: Set up the Outputs to be Saved and Outputs to be Plotted as was done in the earlier example by clicking on the appropriate wires in the Schematic diagram.

3-7: Obtain a netlist by selecting **Simulation -> Netlist -> Create Final**. A window will appear with the netlist. Select **File -> Save As**, enter an appropriate filename (i.e sweep.sp). Exit from all of the Cadence windows. The remaining steps will be performed using Hspice as a standalone tool together with the Awaves Waveform Display tool.

3-8: Using any UNIX editor , edit the file you saved in step 3-7 to change the .OPTION line to read as follows:

.OPTIONS LIST NODE POST

if you want to obtain a listing of your simulation results, add the following line to the netlist:
.PRINT DC V(IN) V(OUT)

3-9: Change the .DC line to read as:SWEEP TEMP LIN 5 0 100

.DC V2 0. 3.30000 0.100000 SWEEP TEMP LIN 5 0 100

i.e. add SWEEP TEMP LIN 5 0 100 to the end of your existing .DC statement

Note: the SWEEP TEMP LIN 5 0 100 part tells Hspice to sweep the value of the temperature from a starting value of 0 degrees Celsius to and ending value of 100 Celsius with a total of 5 values (ie. 0, 25, 50, 75, and 100 C). Save your edited file.

3-10: Run the standalone hspice simulator:

hspice sweep.sp > sweep.lis

3-11: Examine the listing file created by Hspice (sweep.lis) . It will contain listings for 5 values of temperature: 0, 25, 50, 75, and 100 C. Each listing gives the V(out) and V(in) values (as opposed to V(out), V(in), and Time triples as given by a transient analysis).

3-12: Invoke the Awaves tool, and open the Design called sweep.sw0.

3-13: Select the v(out) family of curves and drag this selection into the panel by clicking and holding the middle mouse button. Notice that the graph is a plot of V(OUT) versus V(IN) and there are 5 separate curves; one curve for each particular temperature value of dictated by the SWEEP TEMP LIN command. Refer to Figure 26.

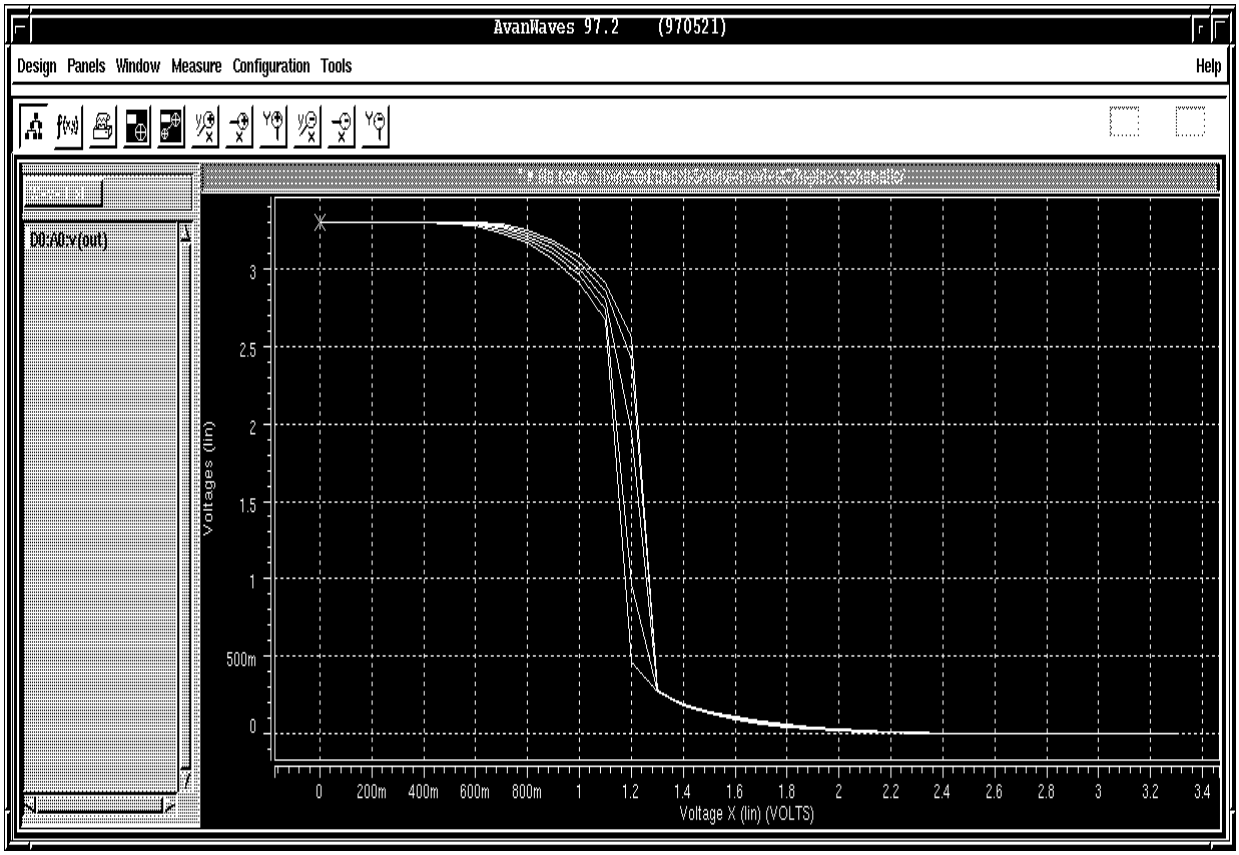

Figure 26: DC Transfer Characteristics corresponding to a Temperature Sweep.