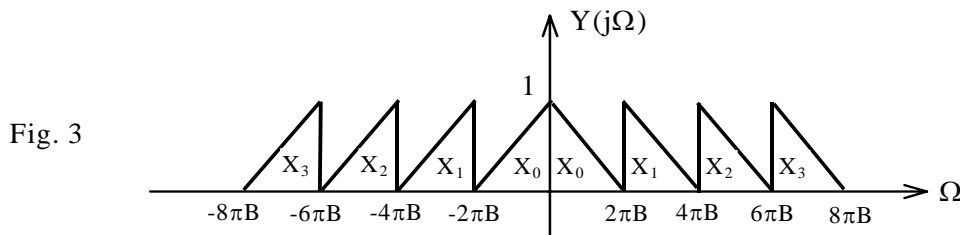
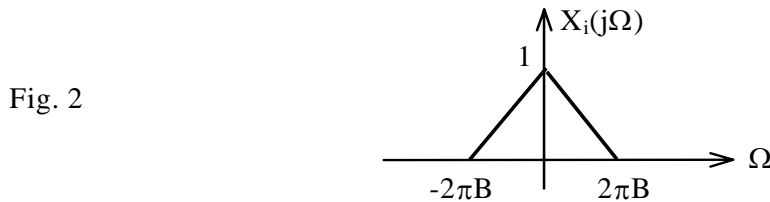
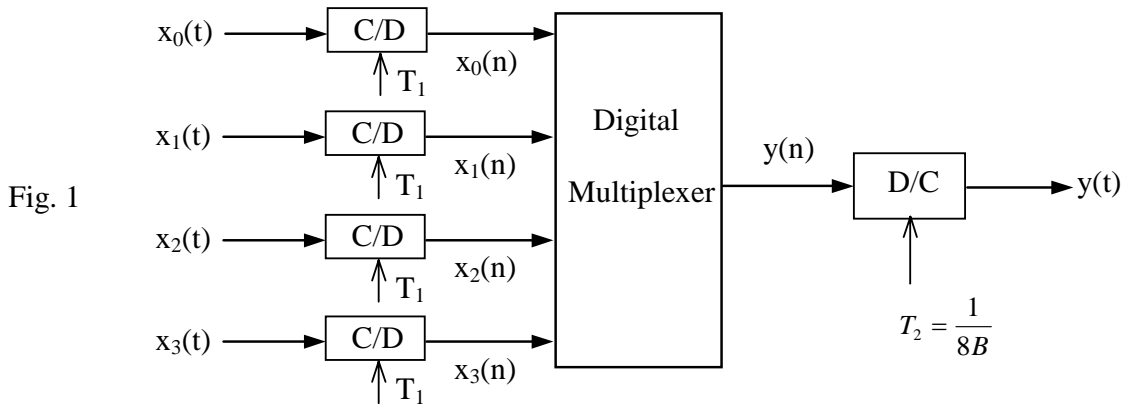


ELEC 6601 Project

Design and Simulation of a Frequency Division Multiplexer

Fig.1 shows a frequency division modulator, which is to convert a number of bandlimited signals to a wide-band frequency division modulated signal. Each of input signals $x_i(t)$ ($i=0,1,2,3$) has a bandwidth of B Hz as illustrated in Fig.2, and is already sampled with $T_1 = \frac{1}{2B}$. The output signal of the modulator should have a spectrum as shown in Fig.3. The Digital Multiplexer is designed to carry out the modulation in discrete-time domain. It contains upsamplers and digital filters.



These digital filters can be derived from the same lowpass filter, called prototype filter and denoted as $H(z)$ (you can use an FIR filter for this purpose). Assume that $B=4\text{kHz}$ and 4 sinusoidal signals $x_k(t)$ are used as input each having a frequency less than 4kHz . In order to distinguish them, you should choose 4 different frequencies.

- Develop the multiplexing algorithm to obtain $y(n)$ from $x_i(n)$ or $y(t)$ from $x_i(t)$. (You might find it easier to work in frequency domain). Draw the implementation diagram of the multiplexer as well as its polyphase structure.
- Plot your input signals $x_k(t)$ and the output signal $y(t)$ with Matlab.
- Design a de-multiplexer to convert the “wide-band” signal $y(t)$ to four narrow band signals, i.e., to recover $x_k(t)$ from $y(t)$. Plot the recovered signals using the result $y(t)$ you obtained in part (a), and compare them with your original input signals.