The Intrinsic Silicon

- Thermally generated electrons and holes
- Carrier concentration

$$p_i = n_i$$

$ni = 1.45X10^{10}$ cm-3 @ room temp

Generally:

$n_i = 3.1X10^{16}\ T^{3/2}\ e^{-1.21/2KT}\ cm^{-3}$

T= temperature in K^o (Degrees Kelvin)

K= Boltzmann Constant

= $8.63X10^{-5}$ eV/K^o

The Extrinsic Silicon

- Number of carriers is increased by introducing foreign atoms called impurities

- The process of introducing impurities is called doping

- Two Types of dopants: p type and n type
    p-type dopants: Boron (B), Gallium (G), Aluminum (Al)
    n-type dopants: Arsenics (Ar), Phosphorous (P), Antimony (Sb)

Doping Concentration

- **P-type:**

  concentration = p = $N_A + p_{th}$

  N_A = concentration of p type do pant (atoms/cm^3)

  p_{th} = concentration of thermally generated holes (holes/cm^3)

  $$p \approx N_A \qquad (N_A >> p_{th})$$

- **n-type:**

  concentration = n = $N_D + n_{th}$

  N_D = concentration of n type do pant (atoms/cm^3)

  n_{th} = concentration of thermally generated electrons (electrons/cm^3)

  $$n \approx N_D \qquad (N_D >> n_{th})$$

Degrees of Doping

Degree of concentration

- **N^{--} or P^{--} :** N_D or $N_A < 10^{14}$ cm^{-3}
- **N^{-} or P^{-} :** 10^{14} cm^{-3} $< N_D$ or $N_A < 10^{16}$ cm^{-3} (lightly doped)
- **N or P :** 10^{16} cm^{-3} $< N_D$ or $N_A < 10^{18}$ cm^{-3} (moderately dop
- **N^{+} or P^{+} :** 10^{18} cm^{-3} $< N_D$ or $N_A < 10^{20}$ cm^{-3} (heavily doped)
- **N^{++} or P^{++} :** N_D or $N_A > 10^{20}$ cm^{-3}

Review of the pn Junction

Potential across pn junction:

$\Phi_D = \quad (KT/q) \ln(N_A.N_D/ni^2)$

Depletion) region length:

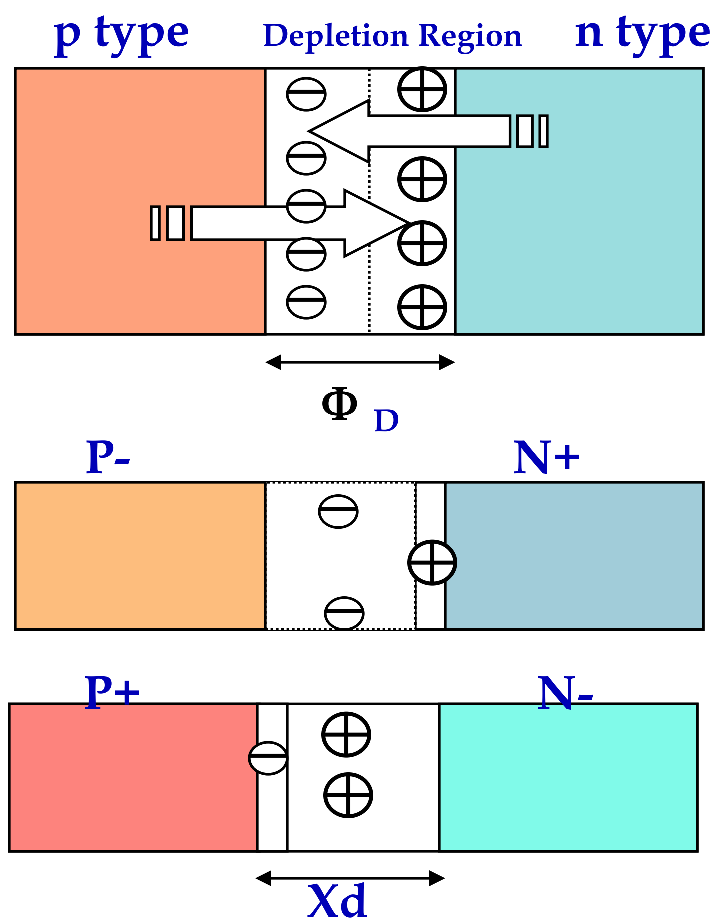
$Xd = K [[(1/N_A) + (1/N_D)] \Phi_D]^{0.5}$

K constant a function of (ε_{si} , q)

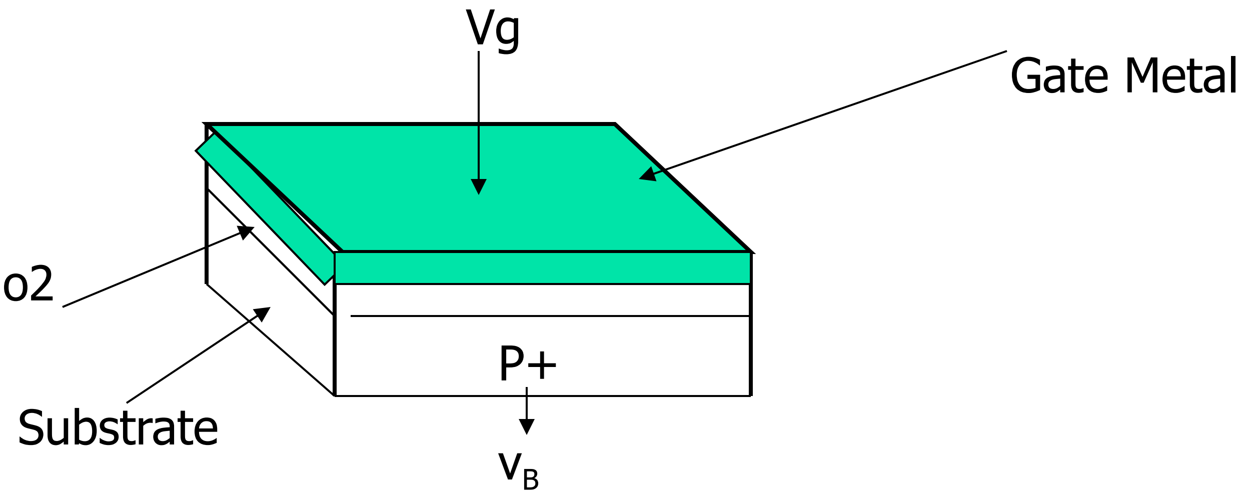
Junction Capacitance:

$Cj = Cjo / (1+V/ \Phi_D)^{0.5}$

It is a function of the applied voltage and doping concentration



Two terminal MOS Structure



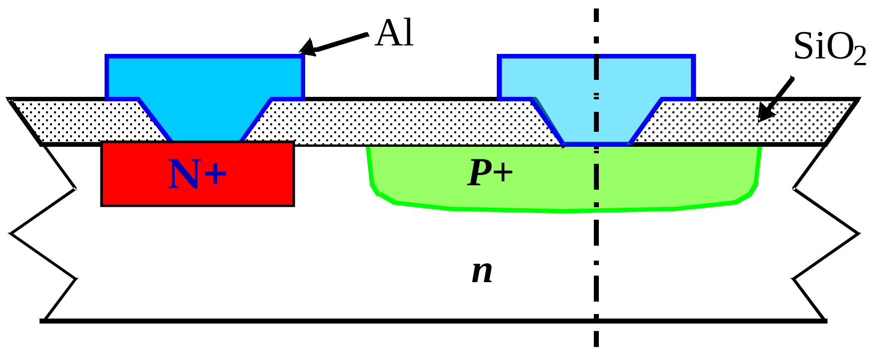
Depth of Depletion region:

$X_d = \{ 2\, \varepsilon_{Si} \,.\, |\Phi_s - \Phi_F| \}^{0.5}$

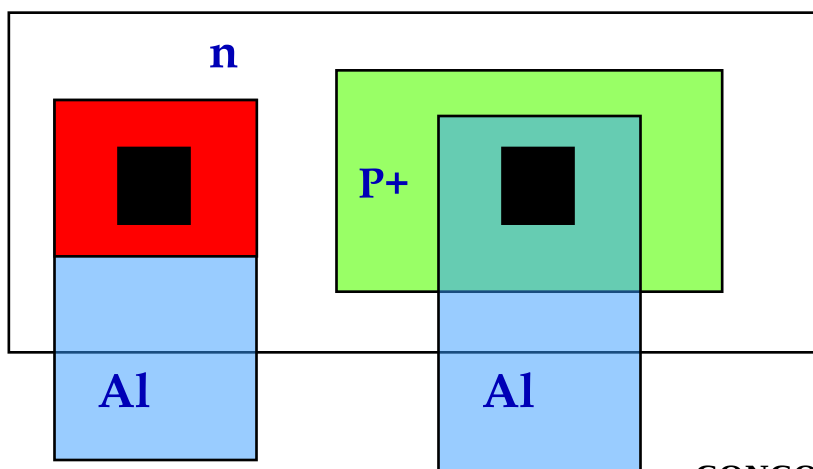
The Charge Density:

$Q = -\{ 2\, q\, N_A\, \varepsilon_{Si} \,.\, |\Phi_s - \Phi_F| \}^{0.5}$

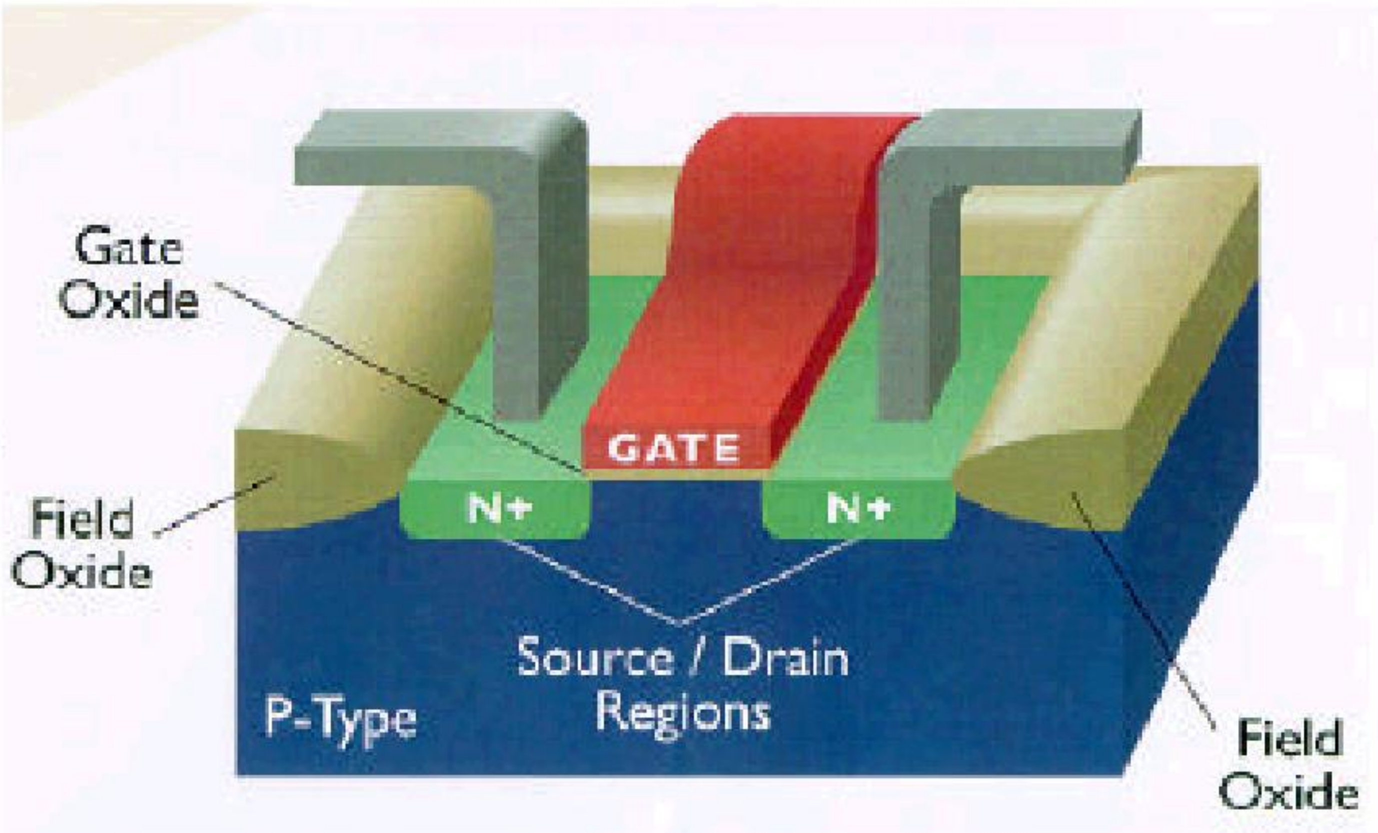
The Physical Structure



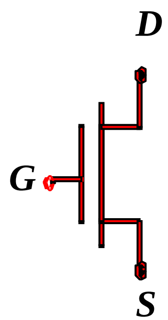
Cross-section of *pn*-junction in an IC process



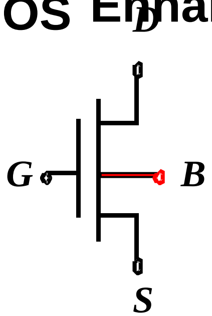
3D Perspective



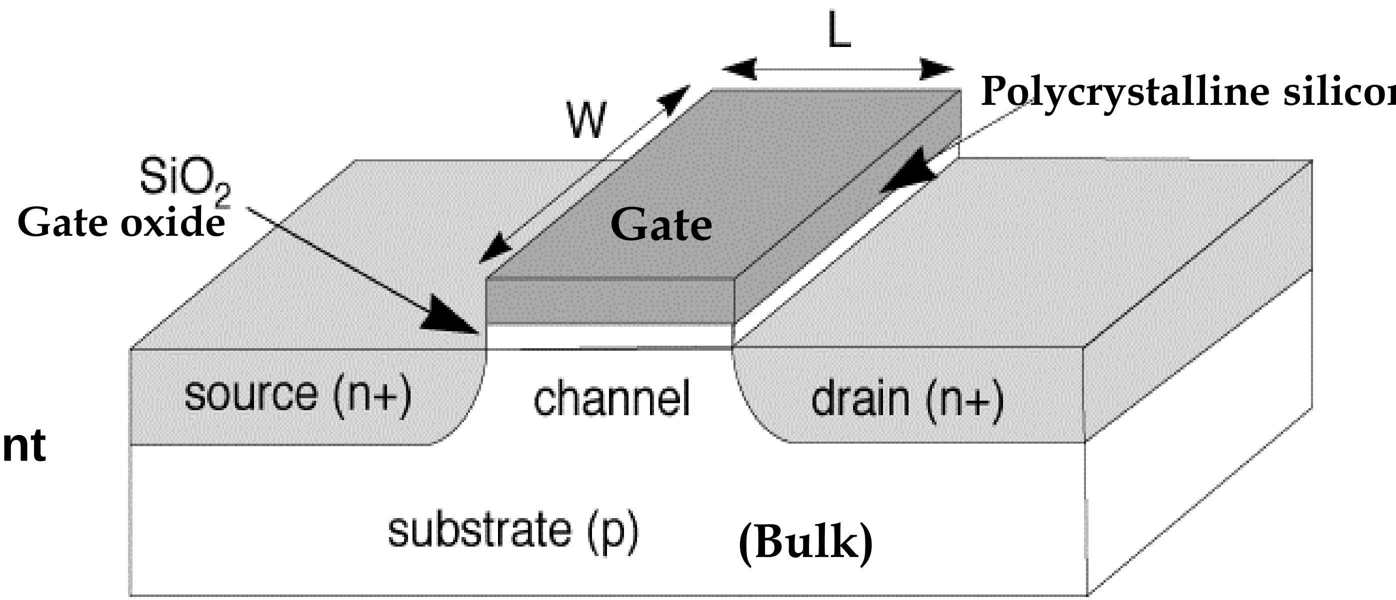
Nmos Transistor



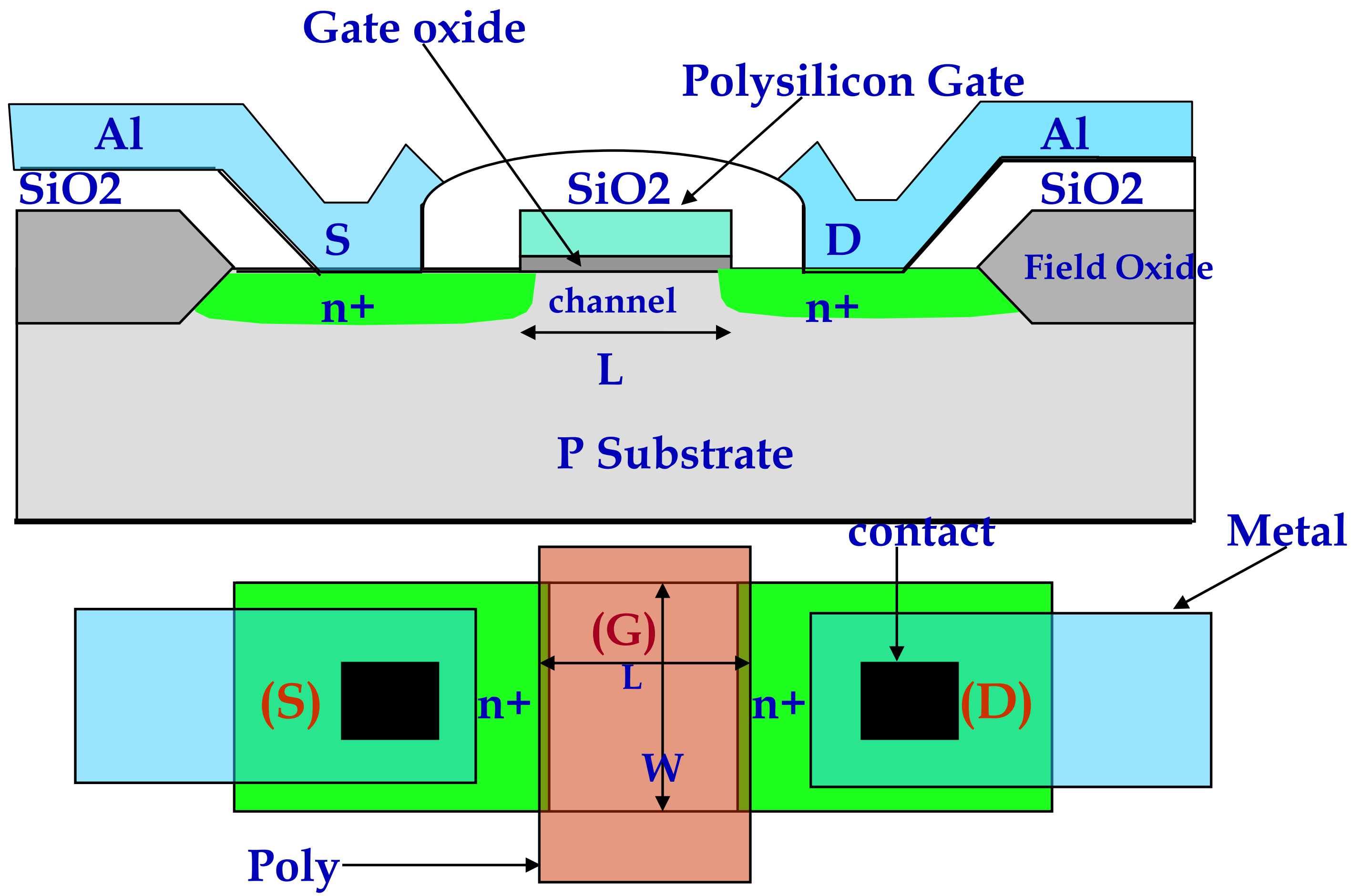
NMOS Enhancement



NMOS with
Bulk Contact



The Physical Structure (NMOS)



The process and sequence is designed by the fabrication house

You design the MASKS

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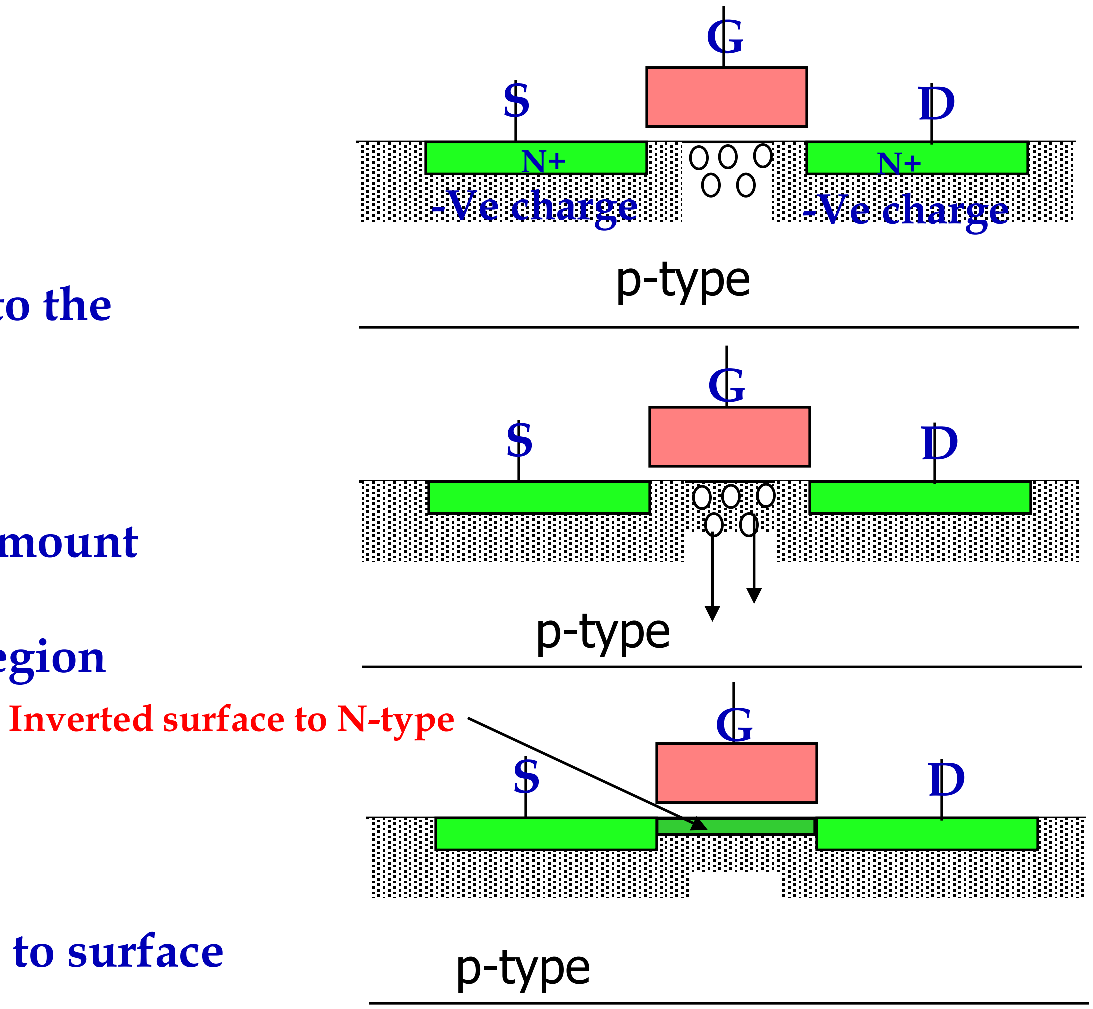
Regimes of Operation

1. **Accumulation**
   - V_{GS} is negative
   - Majority carries attracted to the surface

2. **Depletion**
   - V_{GS} increased by a small amount
   - Majority carriers depleted
   - Space charge (depletion) region formed

3. **Inversion**
   - VGS increased further
   - Minority carriers attracted to surface
   - Inverted surface provides conduction



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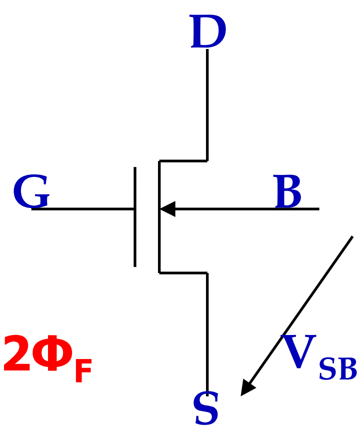
The Threshold Voltage

- The voltage applied between the gate and the source which causes the beginning of the channel surface strong inversion.
- Threshold voltage V_t is a function of :
  - V_{fb} = flatband voltage; depends on difference in work function between gate and substrate and on fixed surface charge.
  - Φ_s = surface potential.
  - Gate oxide thickness.
  - Charge in the channel area.
  - Additional ion implantation.
- Typical values: 0.2V to 1.0V for NMOS and -0.2 to -1.0V for PMOS

Threshold Adjust

- Threshold voltage is a function of source to substrate voltage V_{SB}.
- Body factor γ is the coefficient for the V_{SB} dependence factor.



$$V_T = V_{TO} \pm \Upsilon\left(\sqrt{|-\phi_S + V_{SB}|} - \sqrt{|\phi_S|}\right) \quad , \Phi_s = 2\Phi_F$$

Φ_s is the surface potential ~ -0.6V for NMOS

γ is the body factor ~ 0.6 to 1.2 $V^{1/2}$

Fermi potential Φ_F is is –ve in nMOS, +ve in pMOS

The body effect coefficient γ is +ve in nMOS, -ve in pMOS

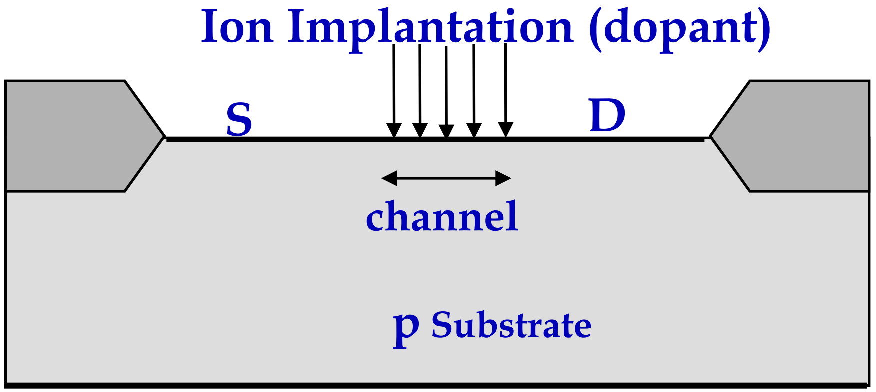
The substrate bias voltage V_{SB} is +ve in nMOS, -ve in pMOS

Threshold Adjust

- nMOS transistors implanted with n-type dopant results in a decrease in threshold voltage

- An effective mean to adjust the threshold is to change the doping concentration through an ion implantation dose.

- nMOS transistors implanted with p-type dopant results in an increase in the threshold voltage.



$V_{TO}' = V_{TO} + (q \cdot D_I / Cox)$

D_I = dose of dopant in the channel area(atoms/cm^2)

C_{ox} = gate oxide capacitance per unit area

Threshold Adjust… Continued

Example of Numerical Values for our process

$$C_{OX} = \frac{0.345}{200A^o} = 0.1725*10^{-2}\ pF/\mu m^2$$

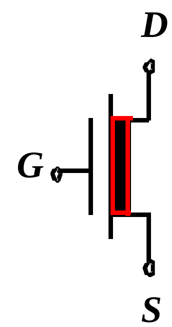
$$q = +1.6*10^{-19} Col/atom$$

$$D_I = \frac{0.1725*10^{-2} F}{1.6*10^{-19} Col/atom} * \frac{10^{-12}}{10^{-8} cm^2}$$

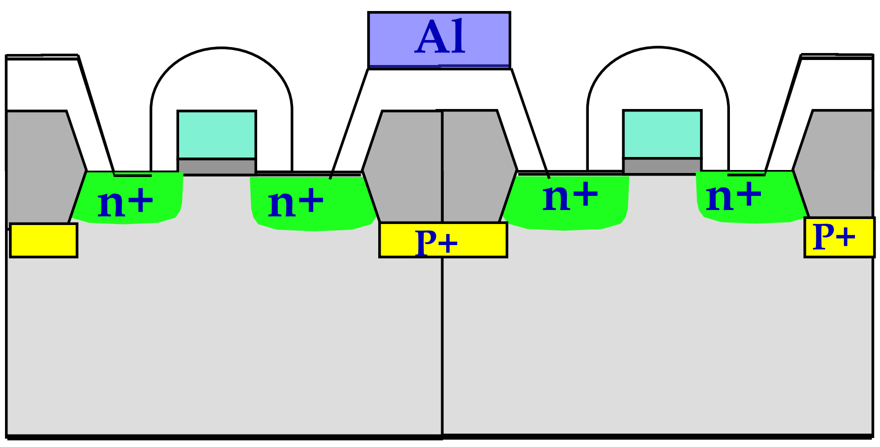
$$= 1.078*10^{12} atom/cm^2$$

Threshold Adjust

- Depletion NMOS transistor
  - **Heavy ion implantation of n dopant in the channel area results in negative threshold voltage**
  - **Transistor conducts with zero gate to source voltage.**
  - **It is called Depletion mode transistor**

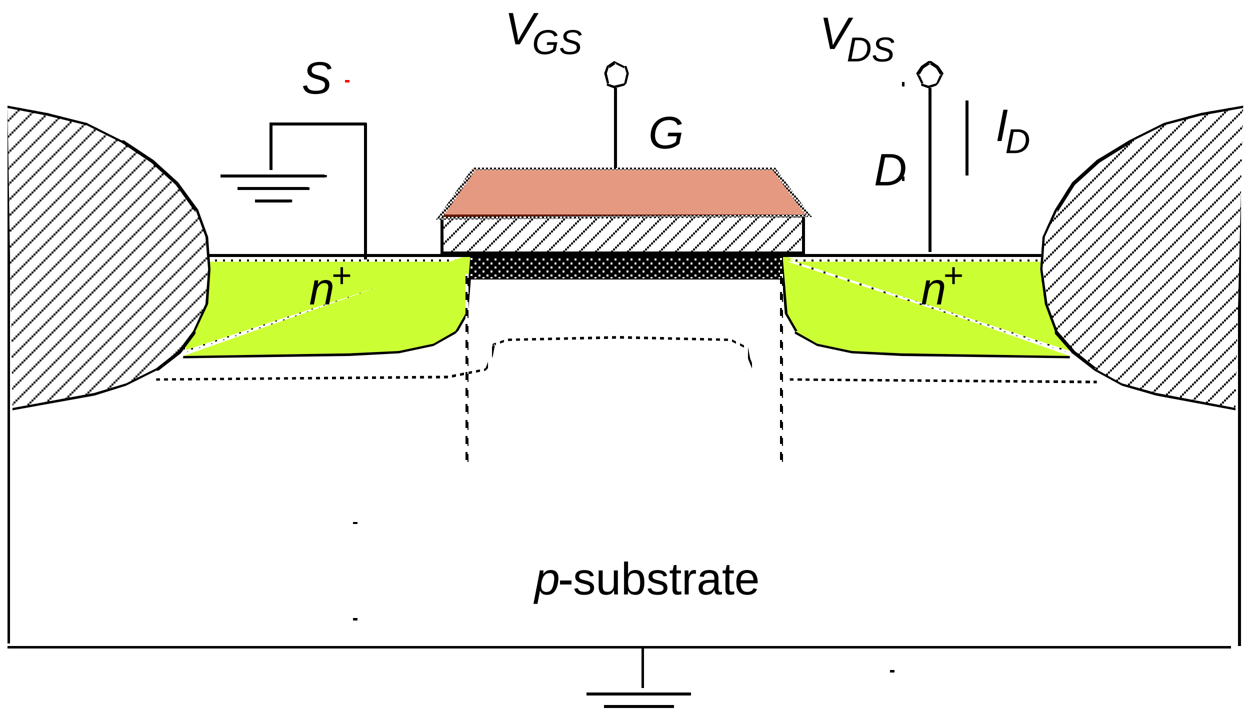


NMOS Depletion



- Field threshold adjust
  - **Required to minimize interaction between transistors.**
  - **Heavy implantation called p-guard/n-guard**
  - **VTF = 12 to 22V**

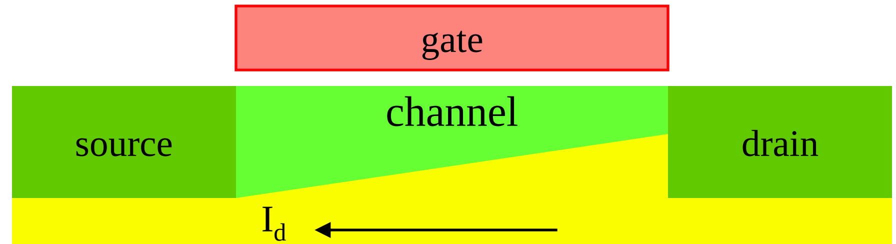
Current-Voltage Relations



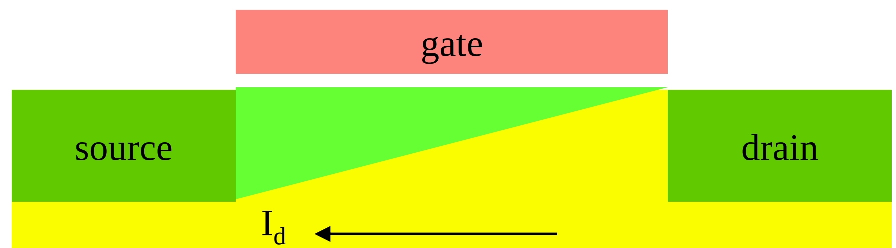
MOS transistor and its bias conditions

Gate Voltage and the Channel

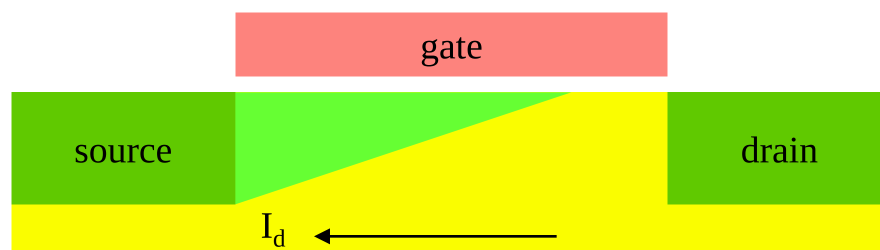
$V_{GS} > V_T$
$V_{DS} < (V_{GS} - V_T)$



$V_{GS} > V_T$
$V_{DS} = (V_{GS} - V_T)$



$V_{GS} > V_T$
$V_{DS} > (V_{GS} - V_T)$



Qualitative Operation of NMOS Transistor

1. Cut-Off Region

$V_{GS} < V_T$

- No Inversion or Weak Inversion
- I_{DS} = leakage current or sub-threshold current

2. Linear Region

$V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$

- Channel surface is inverted
- Output current depends on V_{GS} and V_{DS}
- The relationship between I_{DS} and V_{DS} is almost linear

$$I_{DS} = K' \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{1}{2} \cdot V^2{}_{DS} \right]$$

NMOS Operation-Linear

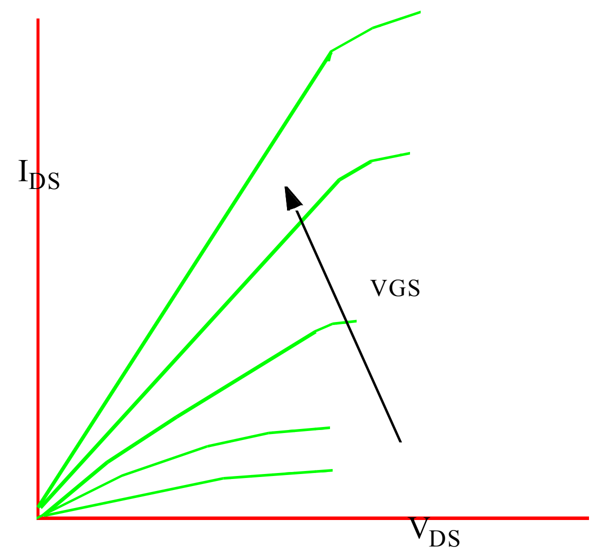
$$I_{DS} = K' \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{1}{2} \cdot V^2{}_{DS}\right]$$

$K' = \mu C_{ox}$ **Process Tranconductance uA/V^2 for 0.35u, K' (Kp)=196uA/ V^2**

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ **Gate oxide capacitance per unit area**

$\varepsilon_{ox} = 3.9 \text{ x } \varepsilon_o = 3.45 \text{ x } 10^{-11}$ F/m

t_{ox} **Oxide thickness for 0.35 u and tox=100A^o**



Quick calculation of Cox:
Cox= 0.345 / tox (A^o) pf/um^2

u = mobility of electrons
550 cm^2/V-sec for 0.35 u process

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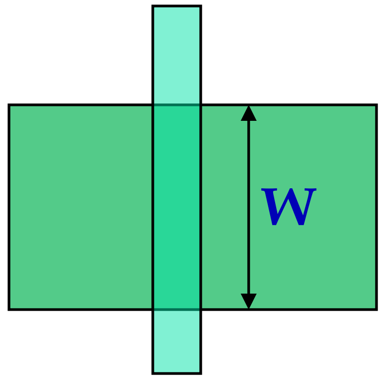
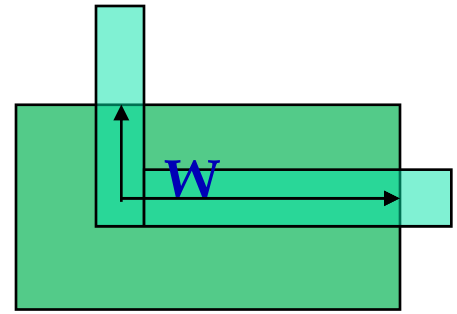
NMOS Operation-Linear

Effect of W/L

↑ **W/L** ↑ **Ids**





Effect of temperature

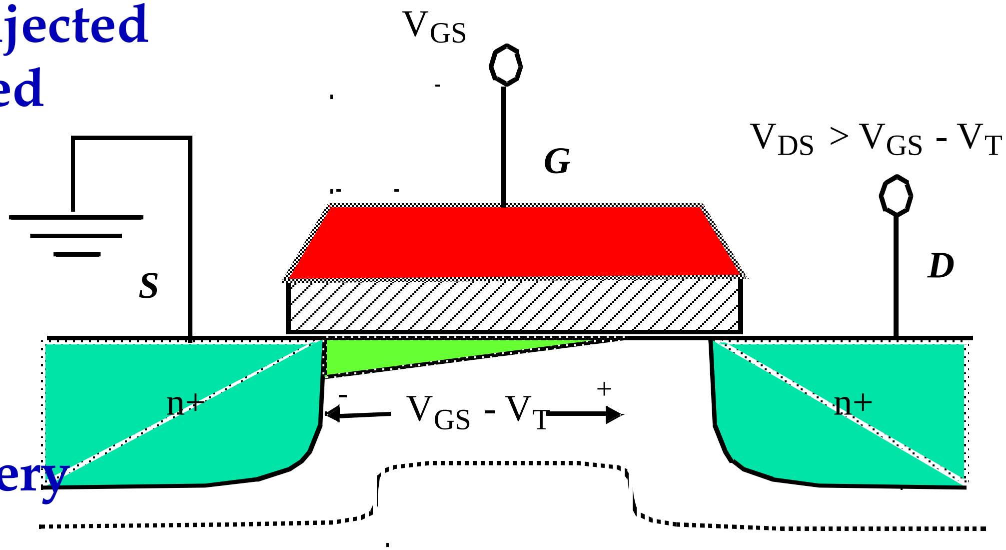
↑ **temp** ↓ **u** ↓ **Ids**

Impact of oxide thickness

↓ **tox** ↑ **K′** ↑ **Ids**

Transistor in Saturation

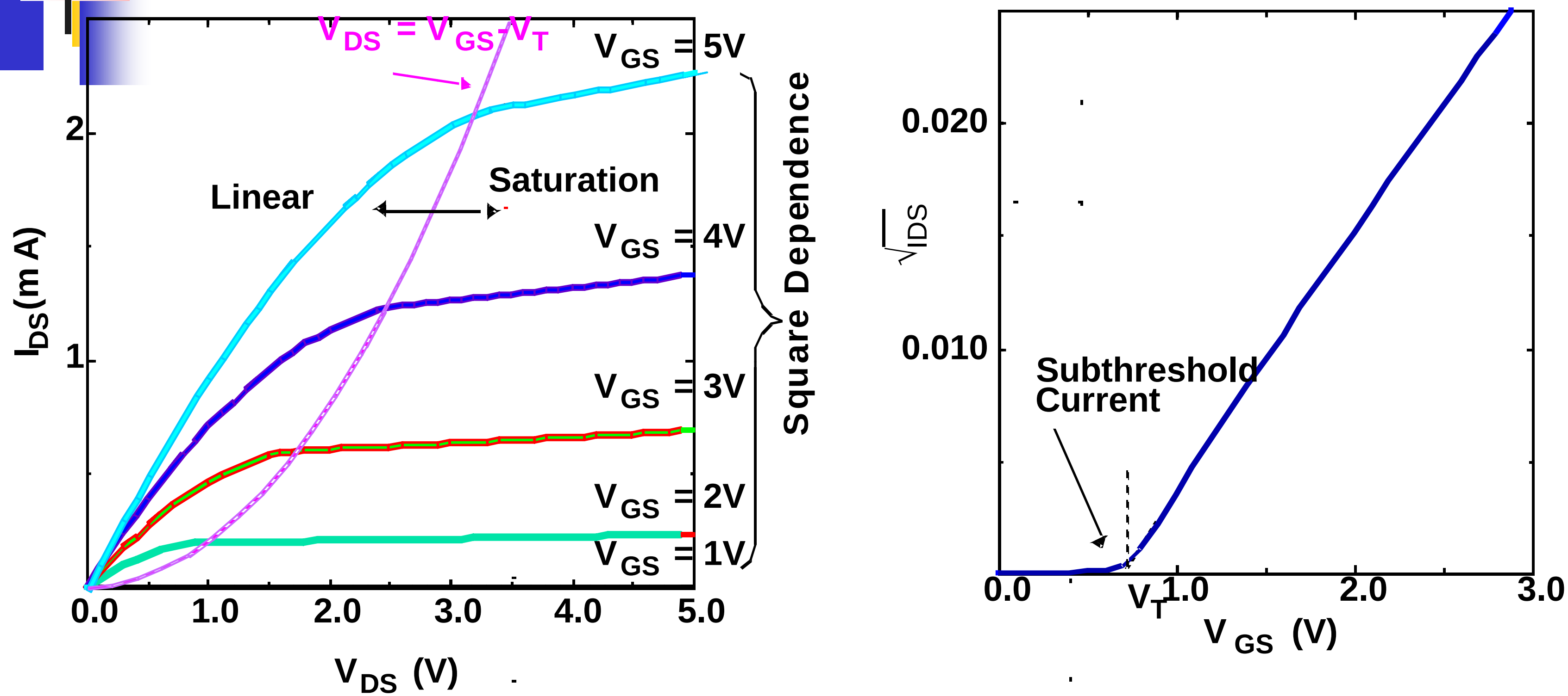
- Electrons leaving channel are injected in depletion region and accelerated towards drain
- Voltage across channel tends to remain constant
- The current I_{DS} saturates with very weak dependence on V_{DS}



$$I_{DS} = K' \cdot \frac{W}{2L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS})$$

λ = channel length modulation parameter
typical values $0.01V^{-1}$ to 0.1

I-V Relation



(a) I_{DS} as a function of V_{DS}

(b) $\sqrt{I_{DS}}$ as a function of V_{GS} (for V_{DS} = 5V)

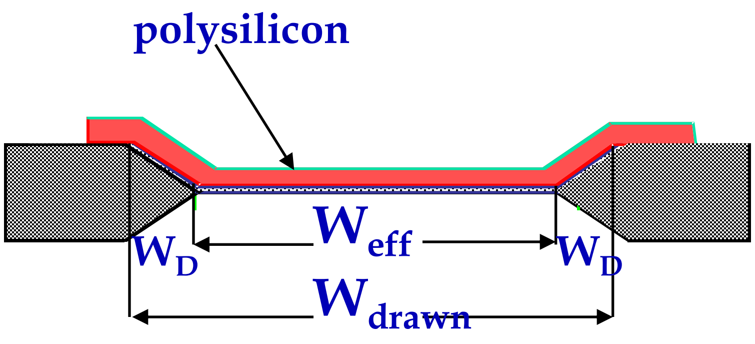
NMOS Enhancement Transistor

Variations in Width and Length

1. Width

Oxide encroachment

$$W_{eff} = W_{drawn} - 2W_D$$

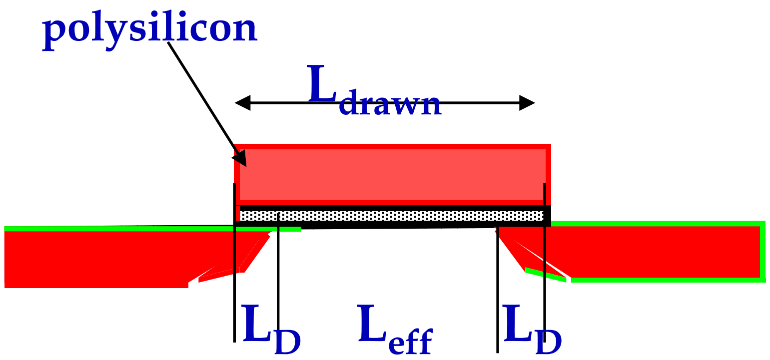


2. Length

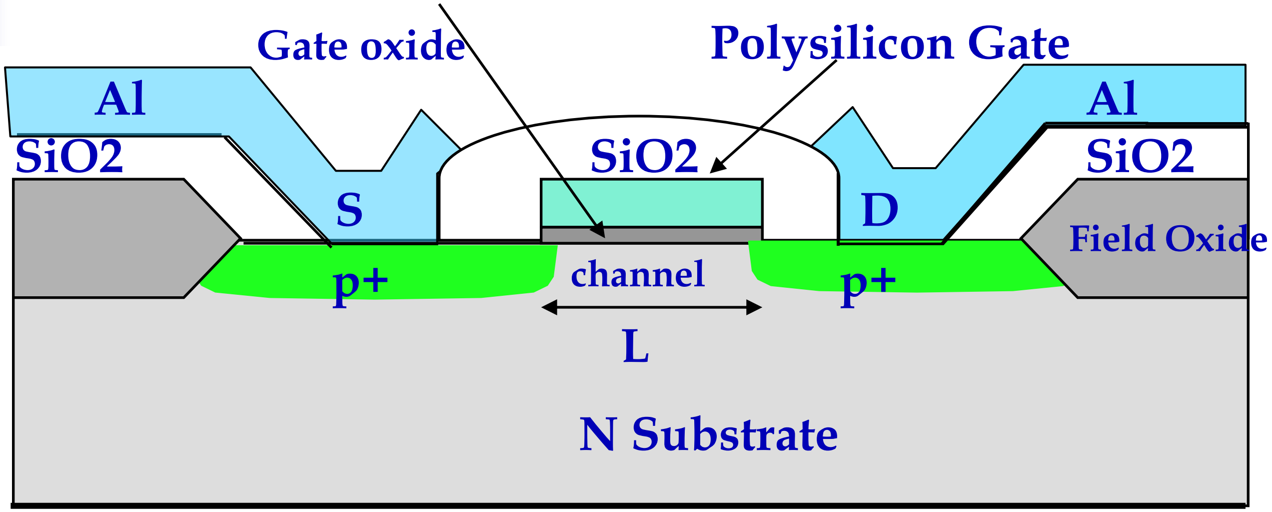
Lateral diffusion

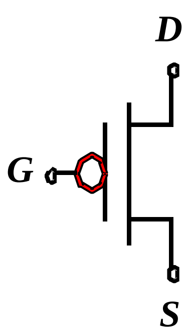
$$L_D = 0.7X_j$$

$$L_{eff} = L_{drawn} - 2L_D$$

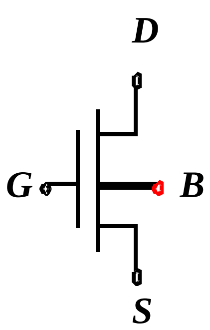


The PMOS Transistor



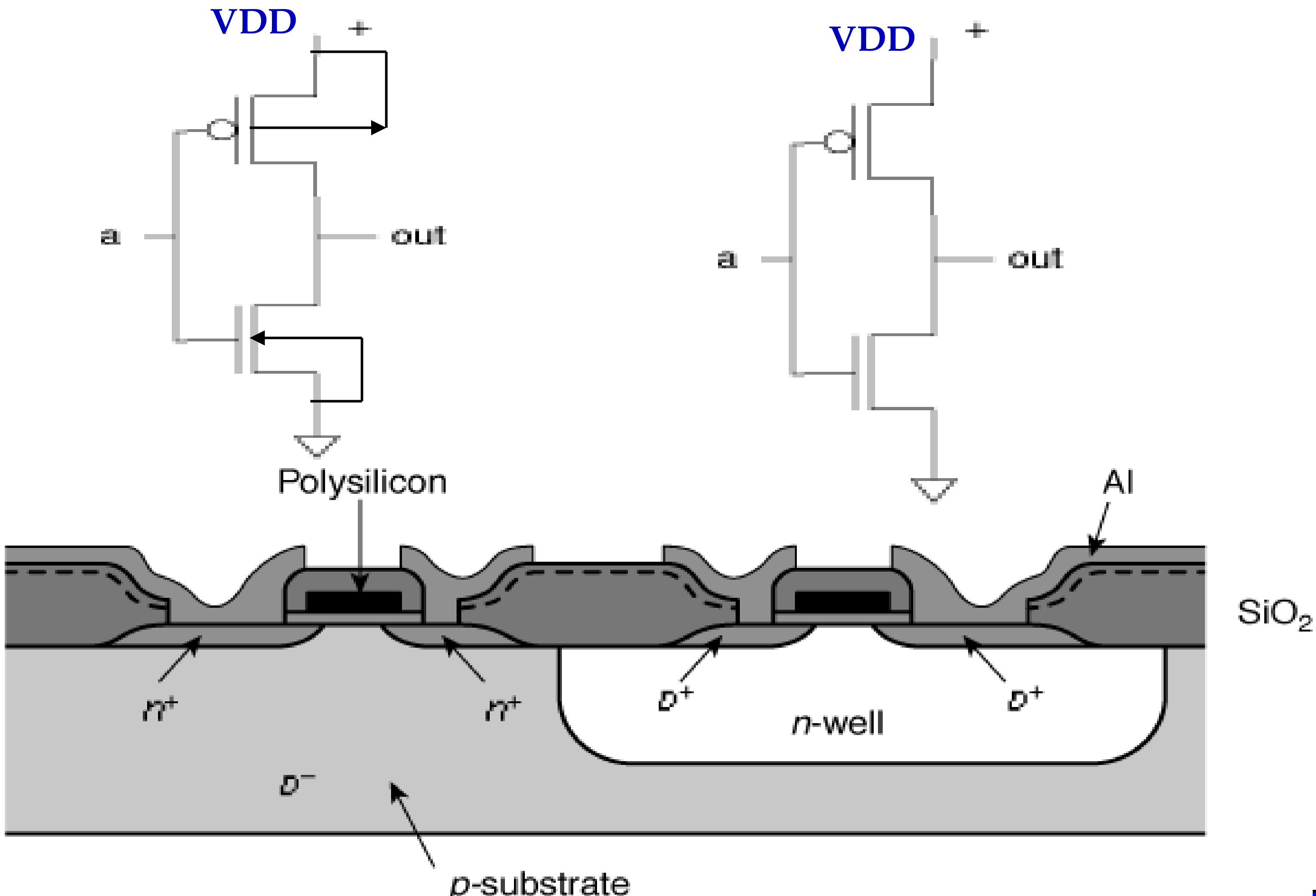


PMOS Enhancement



PMOS with Bulk Contact

The CMOS



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