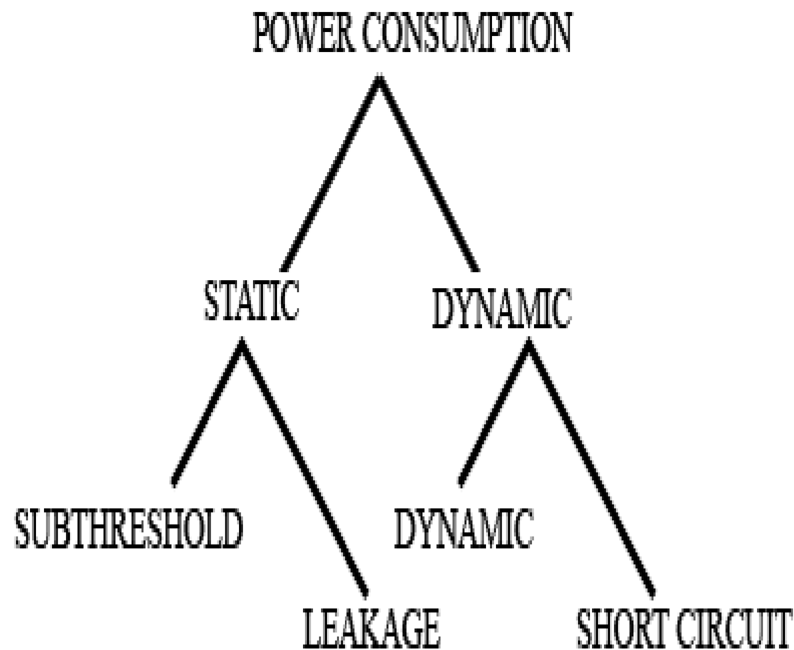
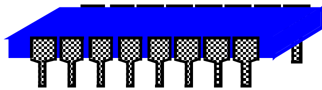
Power Consumption in CMOS



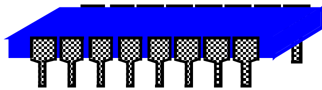


Power Dissipation in CMOS

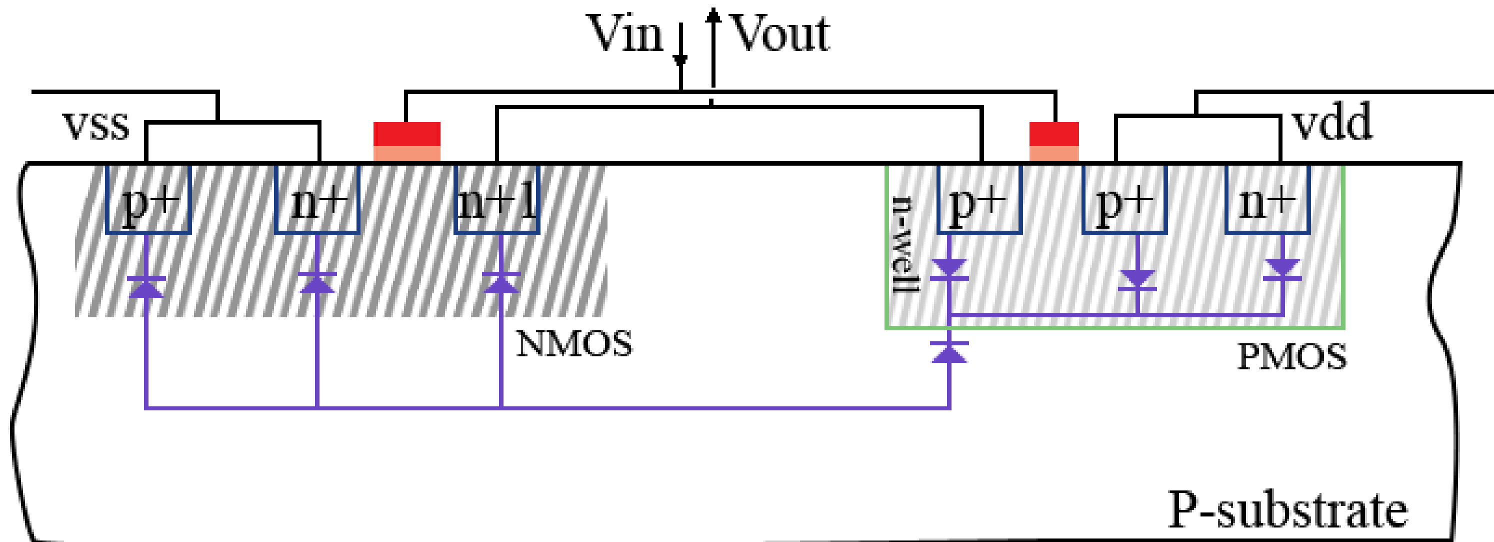
Two Components contribute to the power dissipation:

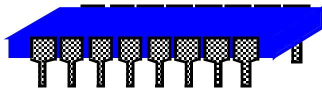
» **Static Power Dissipation**
  - Leakage current
  - Sub-threshold current

» **Dynamic Power Dissipation**
  - Short circuit power dissipation
  - Charging and discharging power dissipation



Static Power Consumption



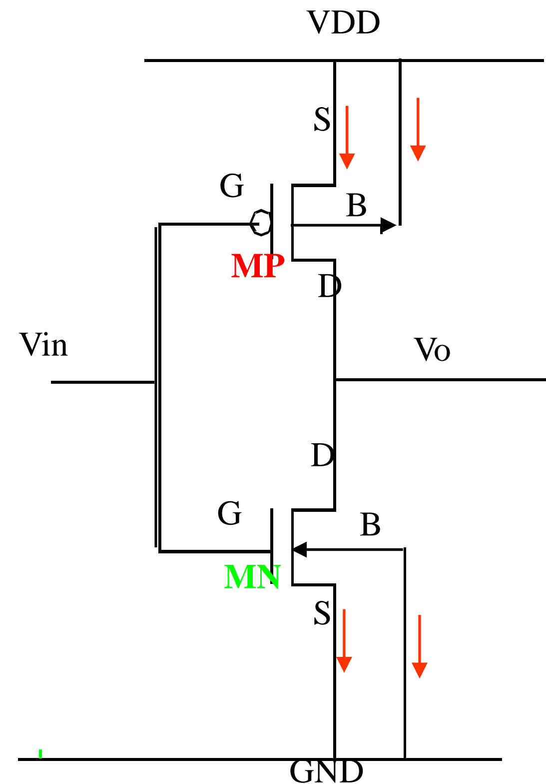


Static Power Dissipation

Leakage Current:

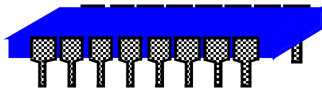
- P-N junction reverse biased current:
  $i_L = A.\, i_s(e^{qV/kT} - 1)$
- Typical value 1pA to 5A / µm²@room temp.
- Total Power dissipation:

$$P_{sL} = \sum i_L . V_{DD}$$



Sub-threshold Current

- Relatively high in low threshold devices



Subthreshold Current

Vgs <≈Vt

Vss

Vdd

Gate
Oxide

GATE

N+

N+

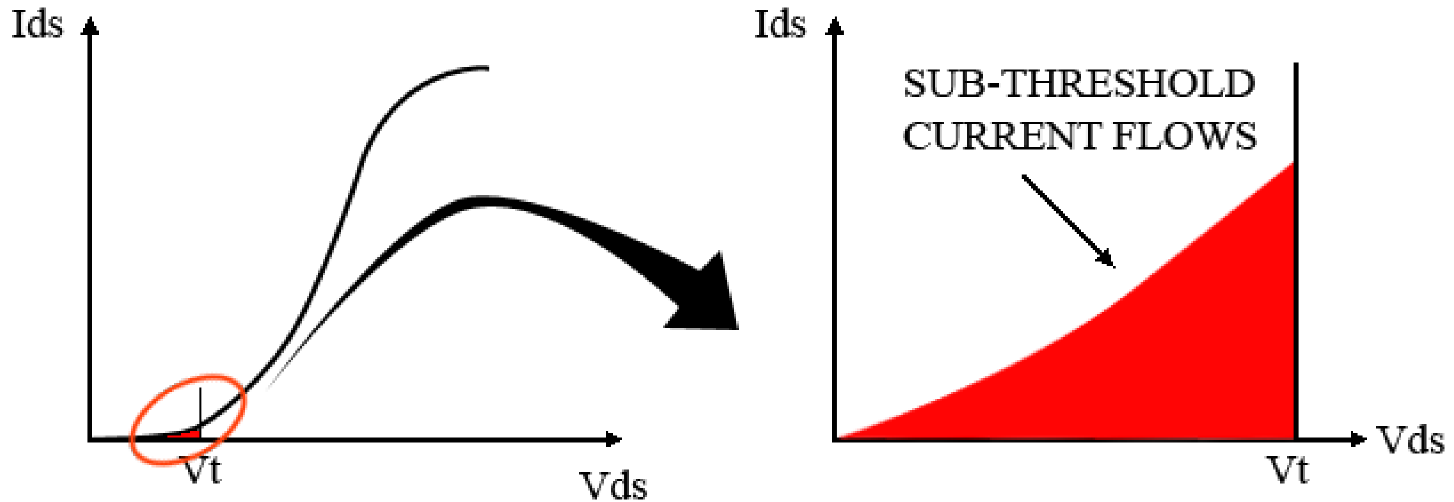
Field
Oxide

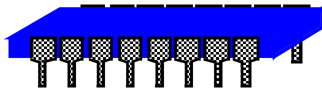
Field
Oxide

Source / Drain
Regions

P-Type

Subthreshold Current





Analysis of CMOS circuit power dissipation

- The power dissipation in a CMOS logic gate can be
- expressed as
- $P = P_{static} + P_{dynamic}$

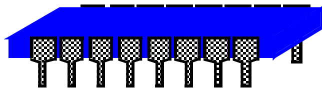
$$= (VDD \cdot I_{leakage}) + (VDD \cdot I_{subthreshold}) + (VDD \cdot I_{lshort\ circuit}) + (\alpha \cdot f \cdot E_{dynamic})$$

- Where α is the switching probability or activity factor

at the output node (i.e. the average number of output switching events per clock cycle).

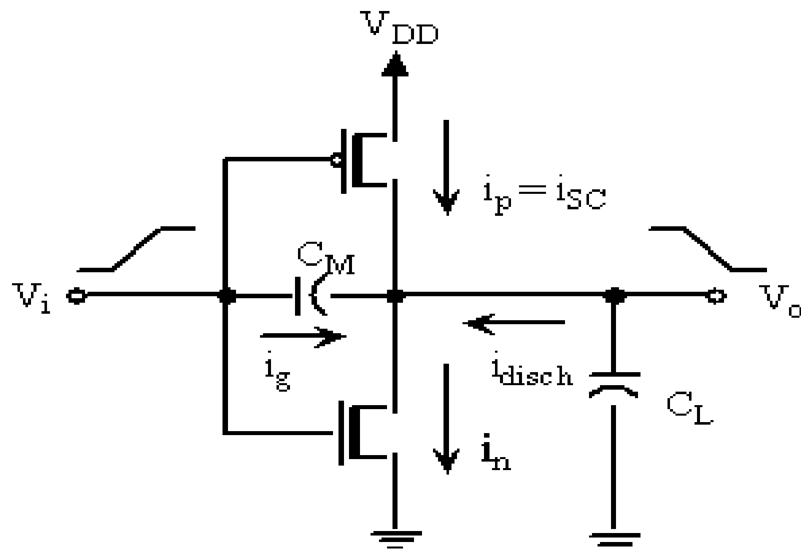
- The dynamic energy consumed per output switching event is defined as

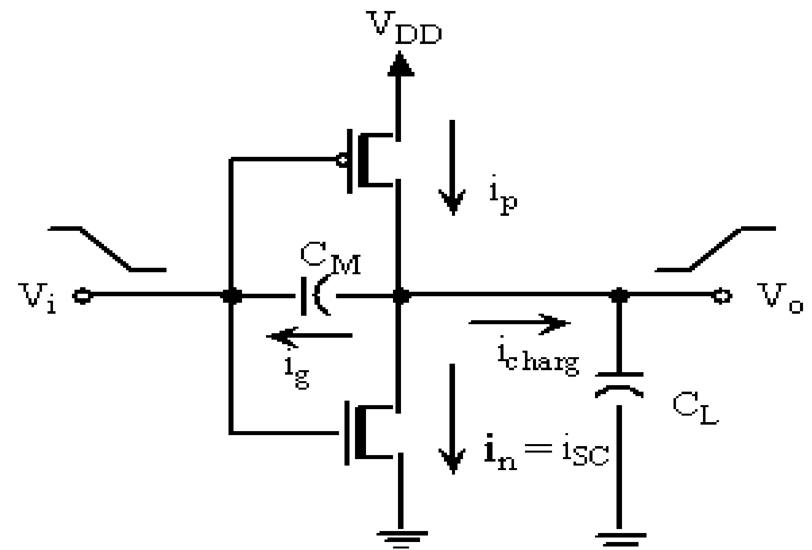
$$E_{dynamic} = \int_{1_switching_event} i_{DD} V_{DD}\, dt$$

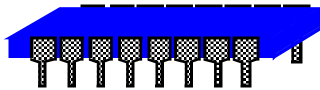


Charging and discharging currents

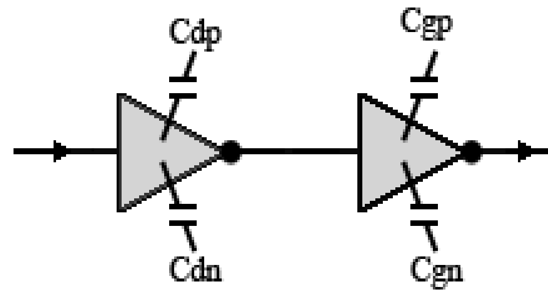
- Discharging Inverter Charging Inverter

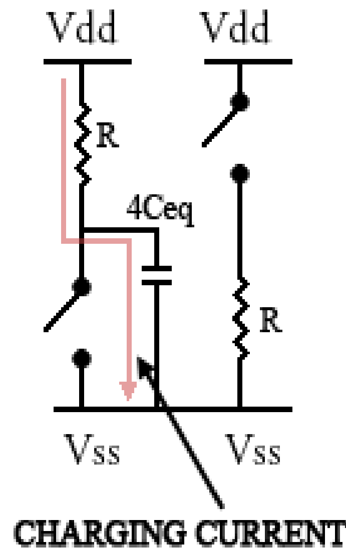


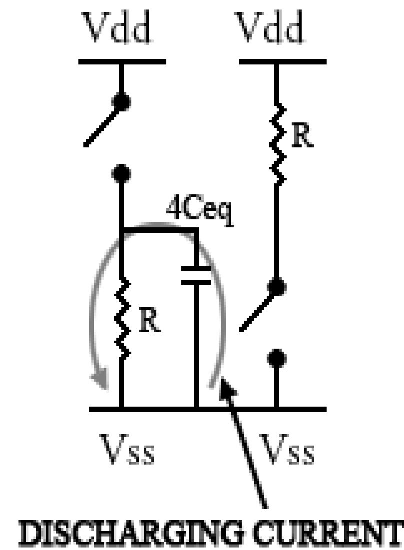


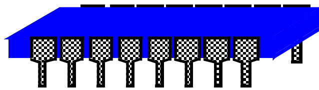


Currents due to Charging and Discharging

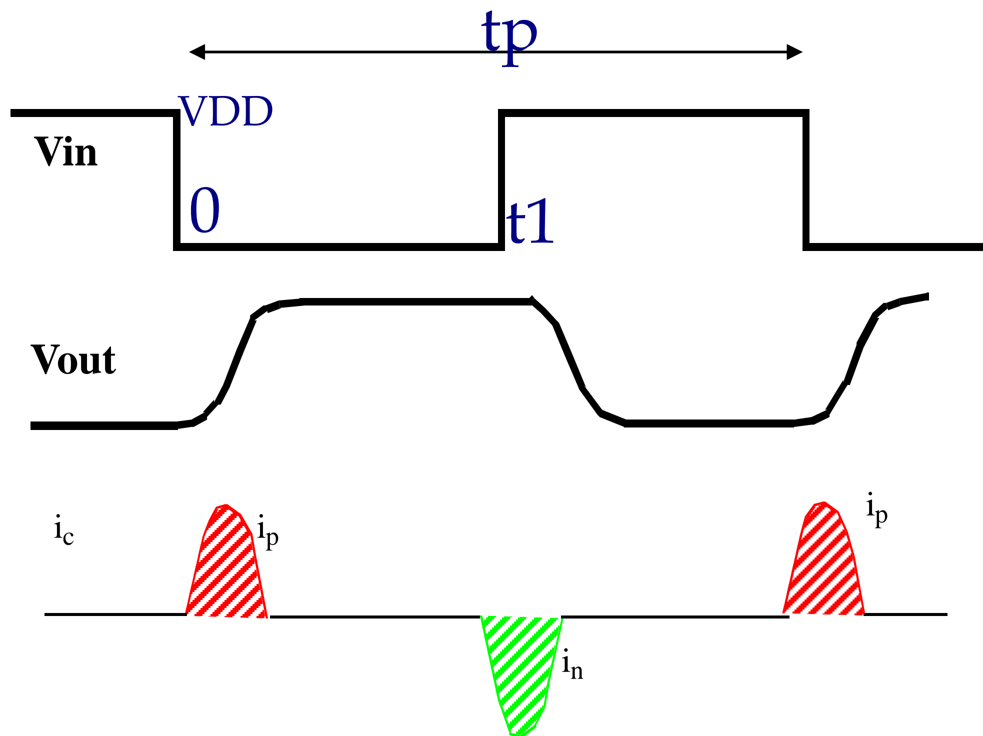


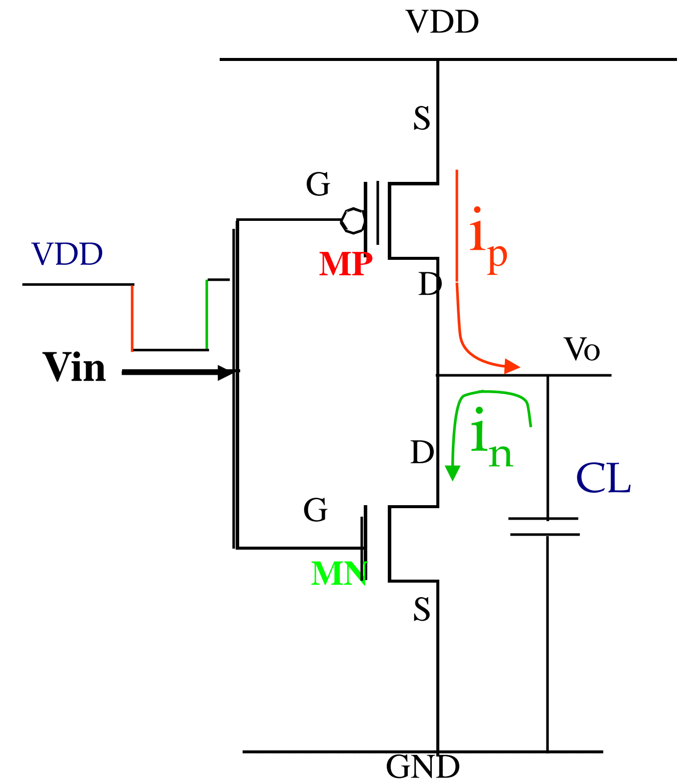






Power Dissipation: Dynamic





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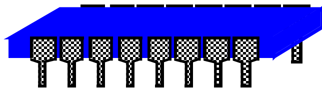


Power Dissipation: Dynamic

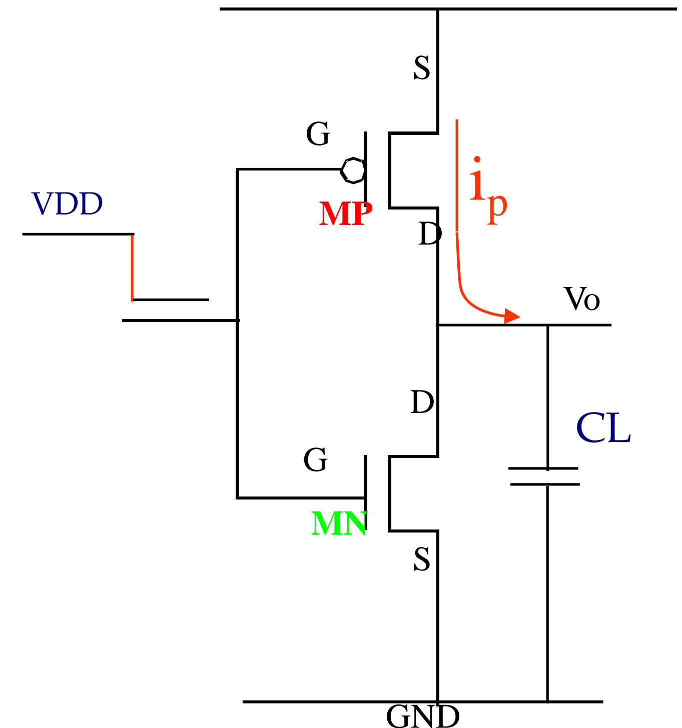
During charging

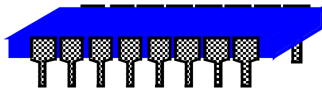
$$P_{dp} = \frac{1}{tp}\int_{0}^{t1} ip(t)(VDD - Vo)dt$$

$$ip(t) = C_L \frac{dVo}{dt}$$

$$Pdp = \frac{C_L}{tp}\int_{0}^{VDD} (VDD - Vo)dVc$$

$$Pdp = \frac{C_L}{2tp}(VDD)^2$$





Power Dissipation: Dynamic

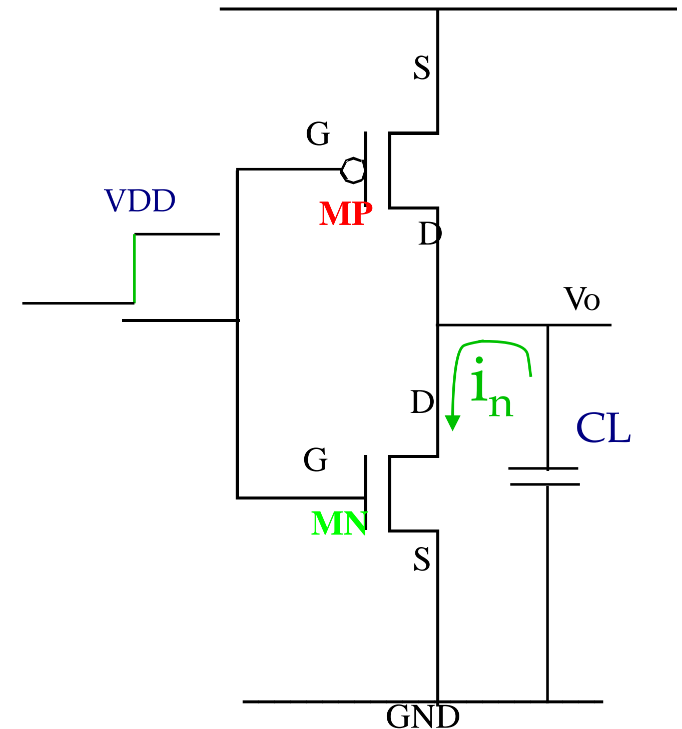
During Discharging

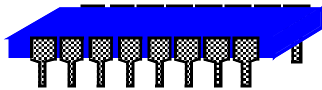
$$Pdn = \frac{1}{tp}\int_{t1}^{tp} in(t)Vodt$$

$$in(t) = -C_L \frac{dVo}{dt}$$

$$Pdn = \frac{C_L}{tp}\int_{VDD}^{0} -VodVo$$

$$= \frac{C_L}{tp}\frac{VDD^2}{2}$$





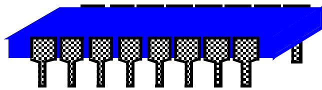
Power Dissipation: Dynamic

Total Power dissipation

$$\text{Pdp} + \text{Pdn} = (C_L/tp)\,(V_{DD})^2$$
$$= C_{L.}\, f.\, (V_{DD})^2$$

Taking node activity factor α into consideration:

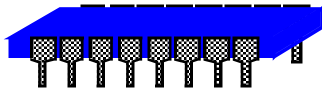
The power dissipation= $\alpha\, C_{L.}\, f.\, (V_{DD})^2$



The MOSFET parasitic capacitances

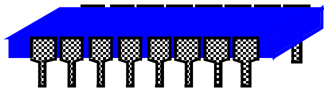
- • distributed,
- • voltage-dependent, and
- • nonlinear.
- So their exact modeling is quite complex and accurate power modeling and calculation is very difficult,

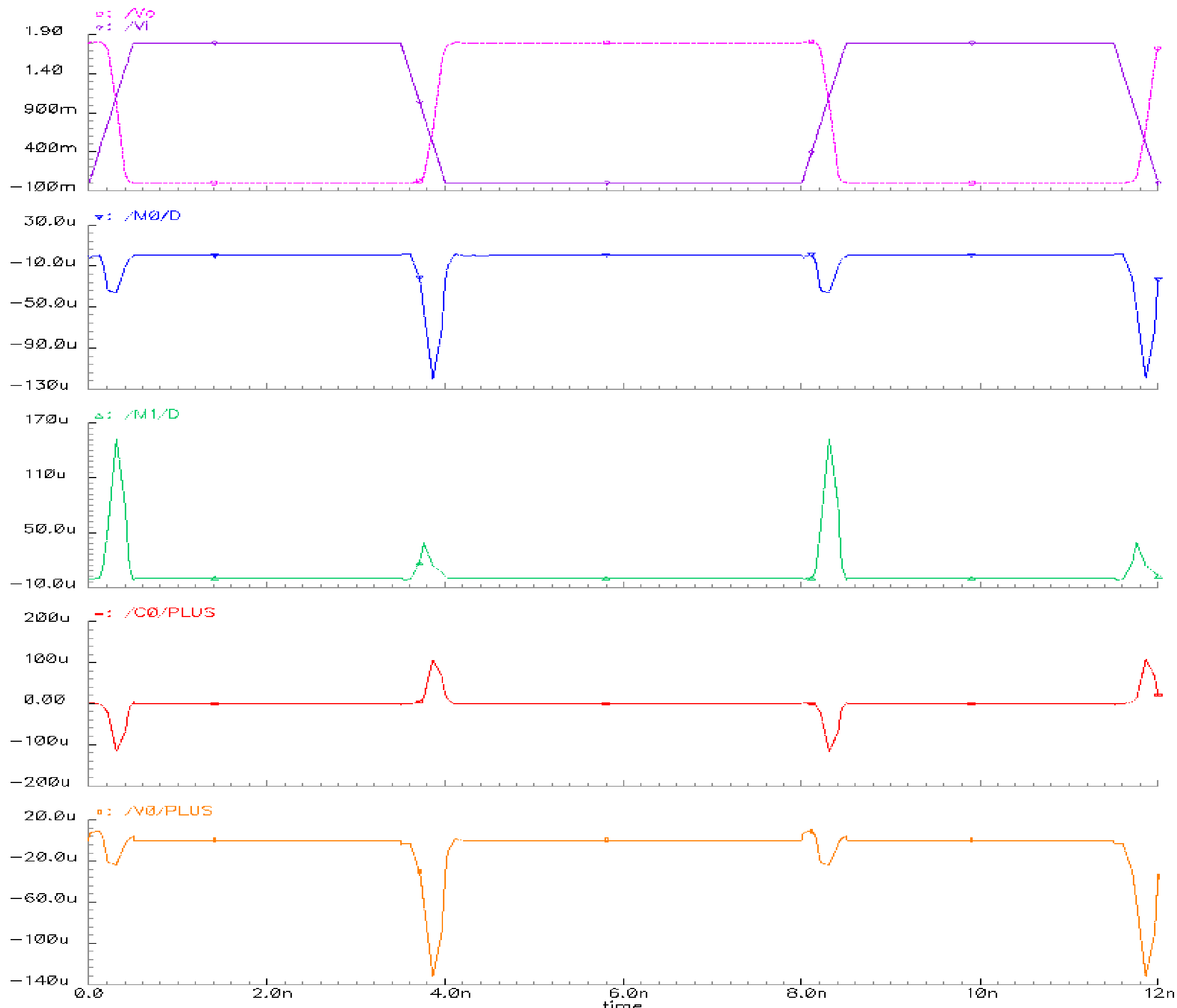
inaccurate and time consuming.



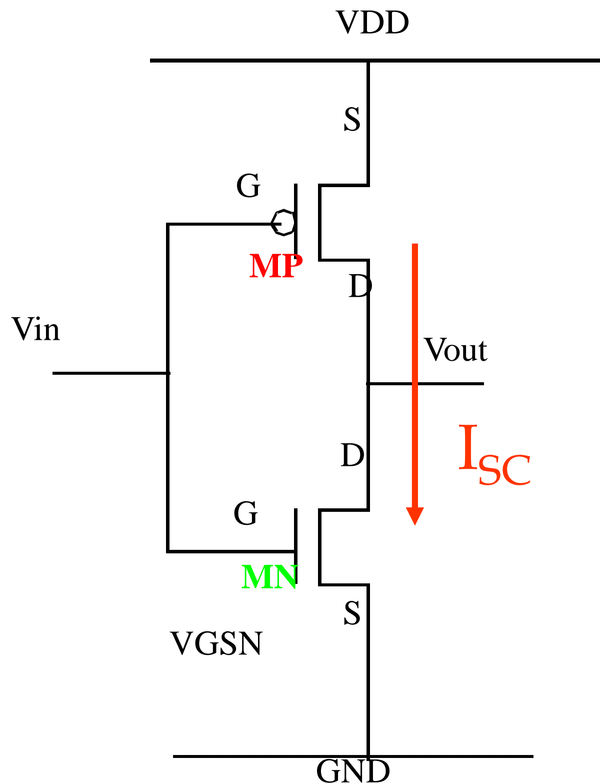
Schematic of the Inverter

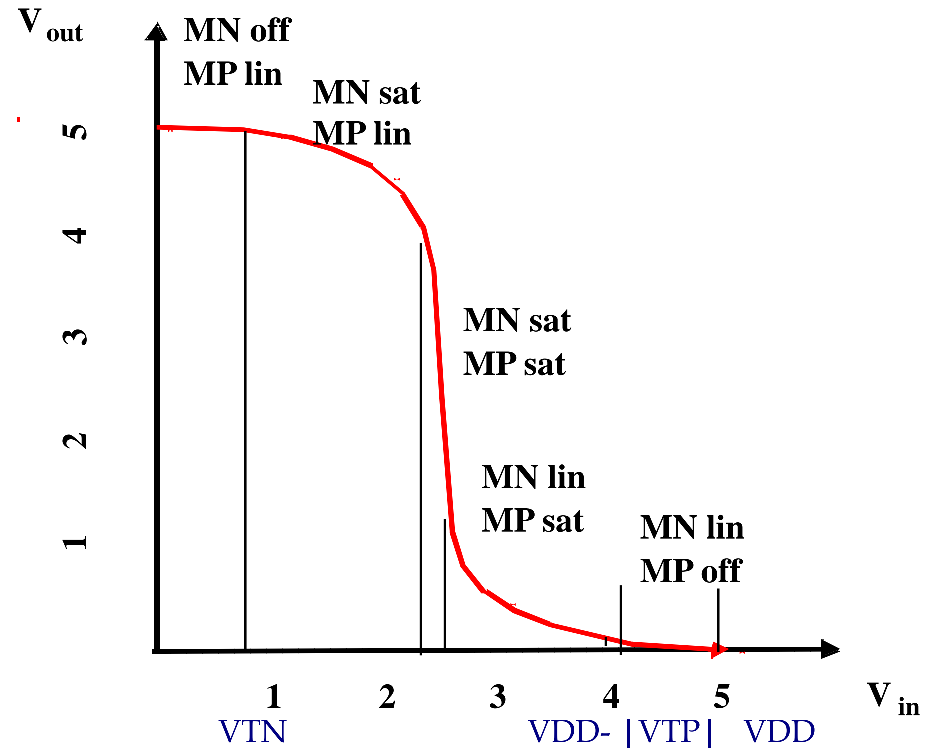
VDD!
M0
"pch"
l:180.00n
w=1.3u
Vi
Vo
V1
v1:0
v2:1.8
tr:500p
M1
"nch"
l:180.00n
w=620.0n
C0
c=10f
VSS!
VDD!
V0
vdc:1.8
VSS!
I0
gndPoint
gnd!
tiedown

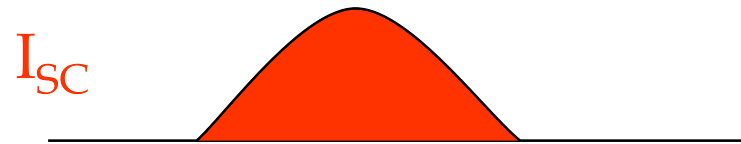


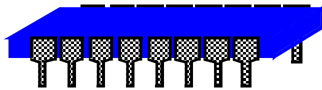

Waveforms of input/output voltages and currents for several nodes
Transient Response
/Vo
/Vi
1.90
1.40
900m
400m
-100m
/M0/D
30.0u
-10.0u
-50.0u
-90.0u
-130u
/M1/D
170u
110u
50.0u
-10.0u
/C0/PLUS
200u
100u
0.00
-100u
-200u
/V0/PLUS
20.0u
-20.0u
-60.0u
-100u
-140u
0.0
2.0n
4.0n
6.0n
8.0n
10n
12n
time

CMOS Inverter VTC /short Circuit Current









Analysis of short-circuit current

The short-circuit energy dissipation E_{SC} is due to the rail-to-rail current when both the PMOS and NMOS devices are simultaneously on.

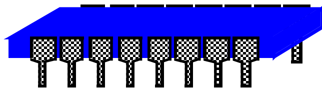
$$E_{SC} = E_{SC_c} + E_{SC_n}$$

Where

$$E_{SC_c} = V_{DD} \int_{v_0 = 0 \rightarrow V_{DD}} i_n \, dt$$

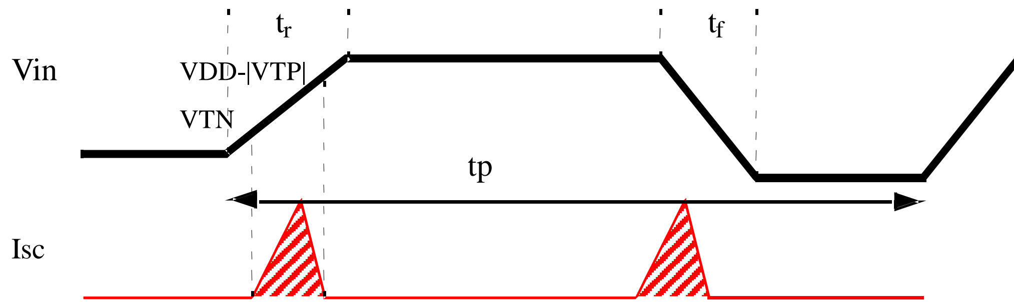
and

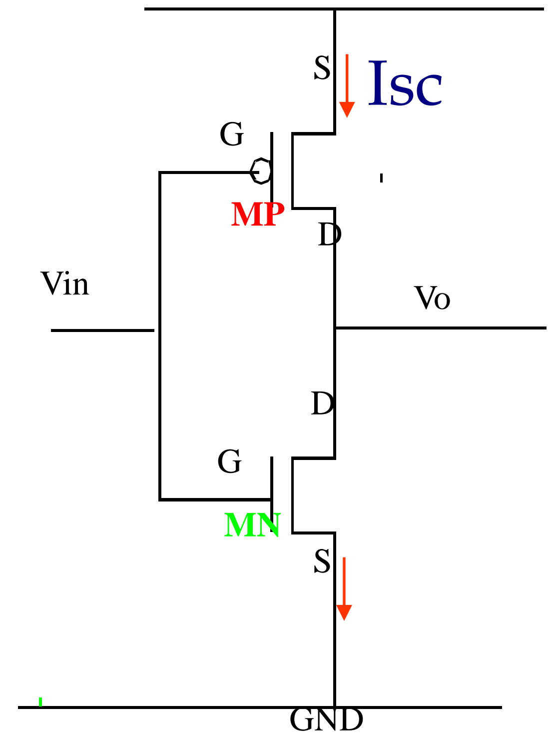
$$E_{SC_d} = V_{DD} \int_{v_0 = V_{DD} \rightarrow 0} i_p \, dt$$



Power Dissipation: short circuit current

Short Circuit:





For tr=tf = trf

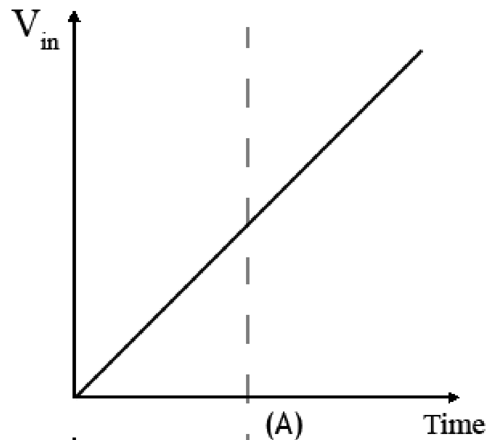
VTN=|VTP|

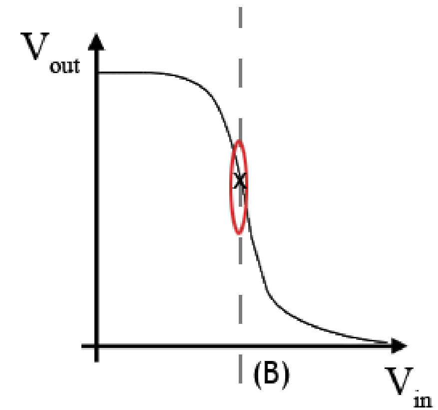
The short circuit power dissipation:

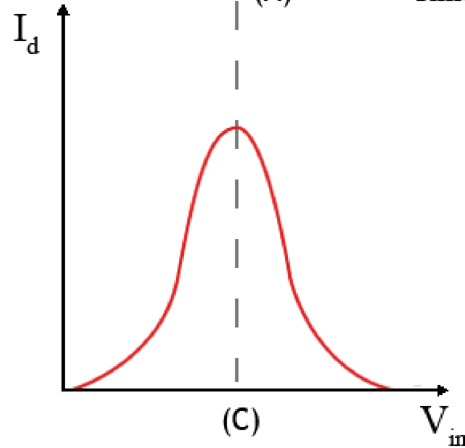
$$P_{sc} = \frac{Kn}{12}(V_{DD} - 2VT)^3 \frac{t_{rf}}{tp}$$

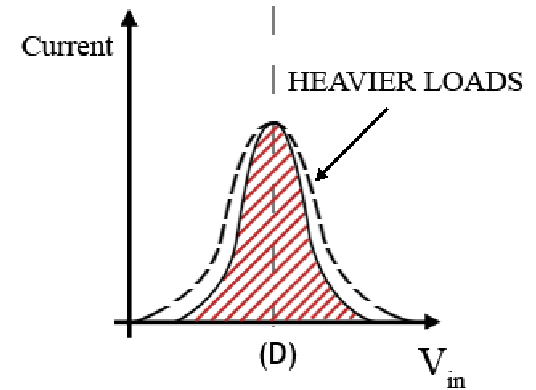
Current flows with load

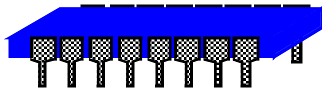
A: Input
B: VTC
C: Current flow
D: Current flow when load is increased











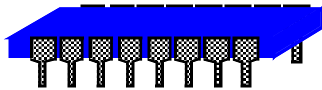
Factors that affect the short-circuit current

For a long-channel device, assuming that the inverter is symmetrical ($\beta_n = \beta_p = \beta$ and $V_{Tn} = -V_{Tp} = V_T$) and with zero load capacitance, and input signal has equal rise and fall times ($\tau_r = \tau_f = \tau$), the average short-circuit current [Veendrick, 1994] is

$$I_{mean} = \frac{1}{12}\frac{\beta}{V_{DD}}(V_{DD} - 2V_T)^3 \frac{\tau}{T}$$

From the above equation, some fundamental factors that affect short-circuit current are:

β $\left(= \frac{\mu\varepsilon}{t_{ox}}\frac{W}{L}\right)$, V_{DD}, V_T, $\tau_{r,f}$ and T.



Parameters affecting short cct current

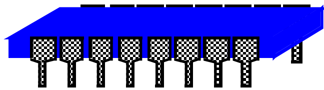
For a short-channel device, β and VT are no longer constants, but affected by a large number of parameters (i.e. circuit conditions, hspice parameters and process parameters).

C_L also affects short-circuit current.

I_{mean} is a function of the following parameters (t_{ox} is process-dependent):

C_L, τ, T (or τ/T), V_{DD}, $W_{n,p}$, $L_{n,p}$ (or $W_{n,p}/L_{n,p}$), t_{ox}, …

The above argument is validated by the means of simulation in the case of discharging inverter,



The effect of C_L on Short CCt Current

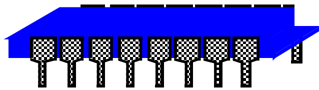
The effect of CL on short-circuit current

Transient Response

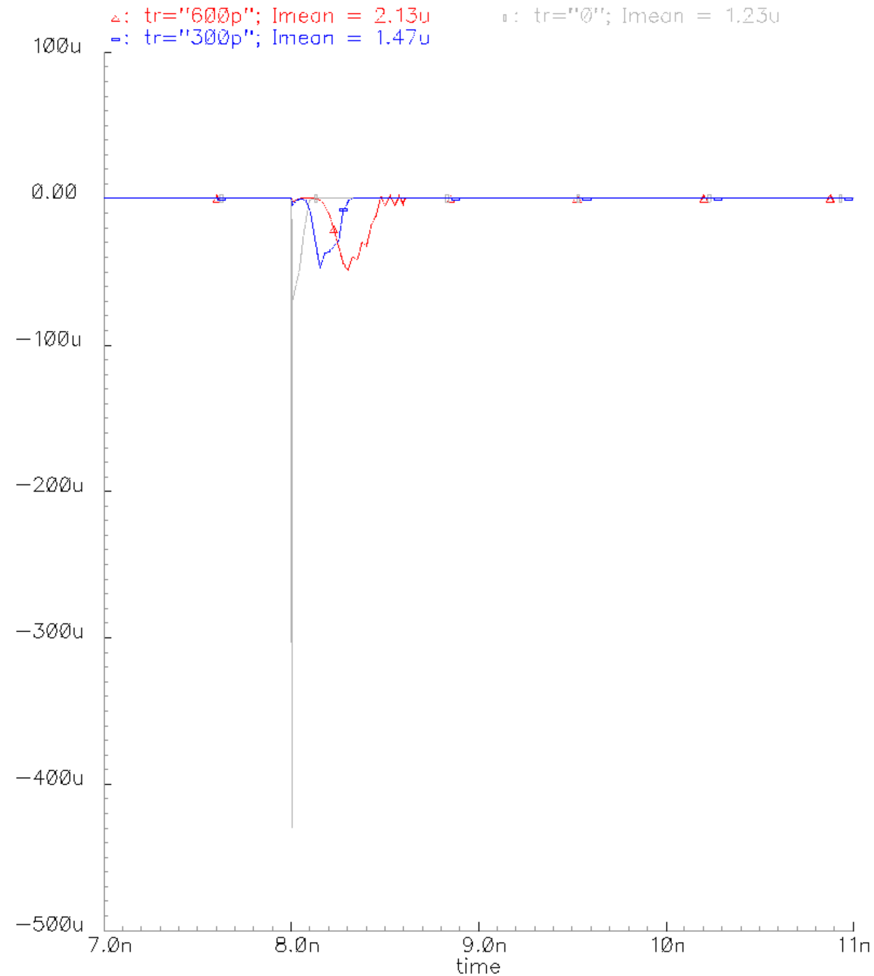
-: cl="50f"; Imean = 1.578u
▫: cl="0"; Imean = 2.25u
△: cl="100f"; Imean = 1.462u

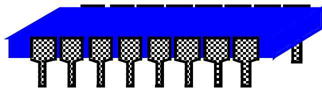
10u
0.0
−10u
−20u
−30u
−40u
−50u
−60u
−70u
−80u
−90u

7.0n
8.0n
9.0n
10n
11n
time



Effect of t_r on short cct Current





Effect of Wp on Short cct Current

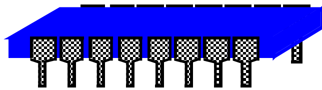
The effect of Wp on short–circuit current

Transient Response

△: wp="1.6u"; Imean = 2.304u
▫: wp="1u"; Imean = 1.572u
▭: wp="1.3u"; Imean = 1.923u

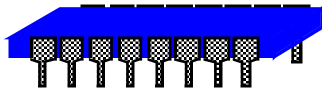
10u
0.0
−10u
−20u
−30u
−40u
−50u
−60u

7.0n 8.0n 9.0n 10n 11n
time



Effect of time step setting on simulation results

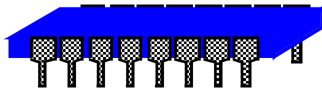
Tr (ps)	Timestep (ps)	MaxStep (ps)	i_{Max} (uA)	$i_{average_inT/2}$ (uA)
0	2	10	802.6	1.258
	4	10	413.8	1.264
	5	10	336.4	1.24
	6	10	284.9	1.234
	8	10	221	1.245
	10	20	183	1.231
100	2	10	73.09	1.202
	4	10	64.4	1.213
	5	10	58.69	1.21
	6	10	65.64	1.208
	8	10	76.13	1.207
	10	20	63.1	1.217
200	2	10	50.96	1.311
	5	10	49.78	1.295
	5	20	50.46	1.313
	8	10	50.72	1.311
	8	20	52.08	1.311
	10	20	51.25	1.311



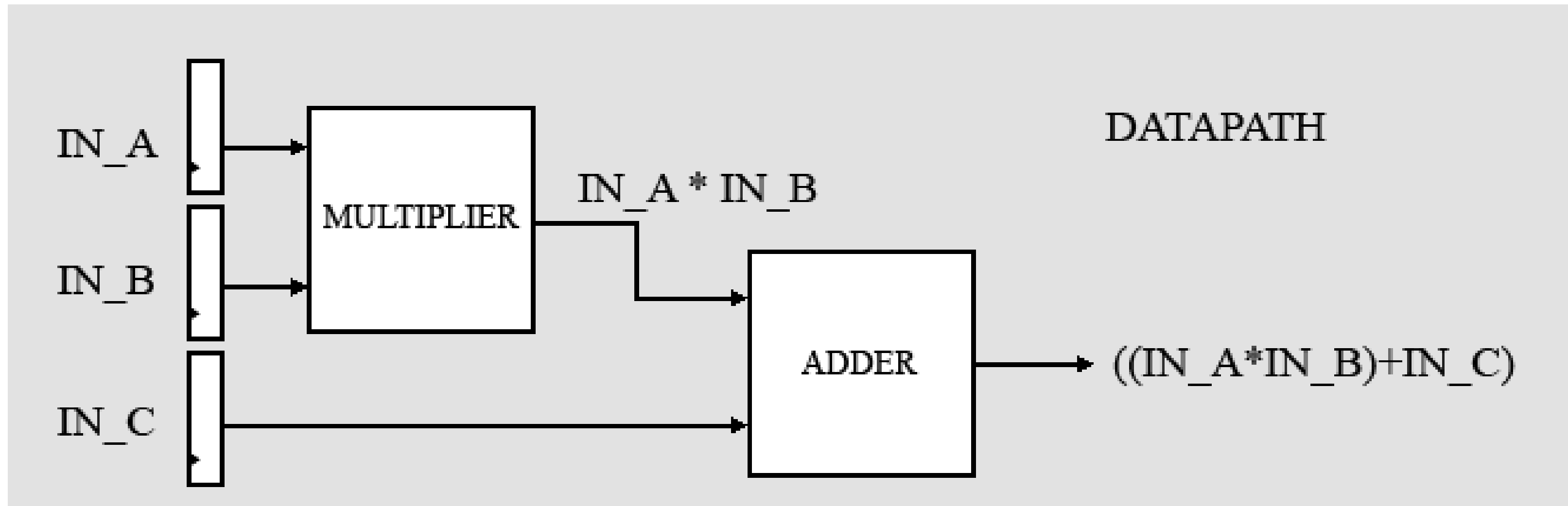
Reducing Power Consumption

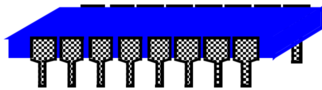
It can be done in several ways:

- Circuit Design
- Architecture design
- Activity reduction
- Changing Vt
- Etc.



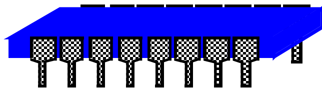
Datapath to be optimised for power consumption





Pipelining the circuit

Level 1
Level 2
DATAPATH
WITH PIPELINING
REGISTERS
IN_A
IN_B
IN_C
MULTIPLIER
ADDER
((IN_A*IN_B)+IN_C)



Parallelism

DATAPATH WITH PARALLELISM

f/2
f/2
f/2
f/2
f/2
f/2

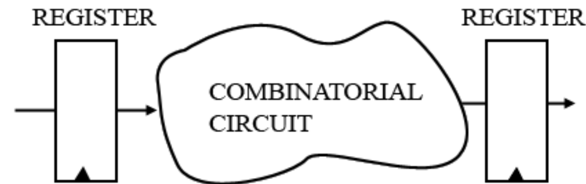
M
M
A
A
MUX
f

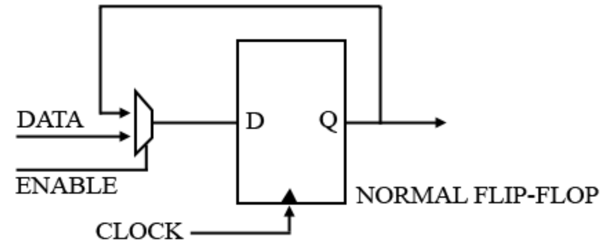
Parallelism and pipelining

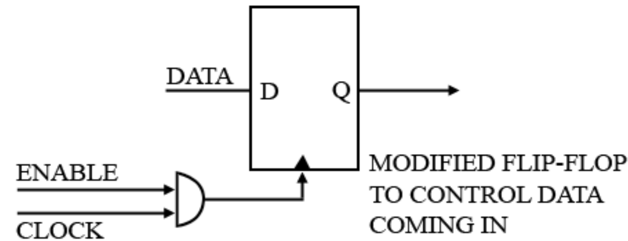
DATAPATH WITH PARALLELISM AND PIPELINING

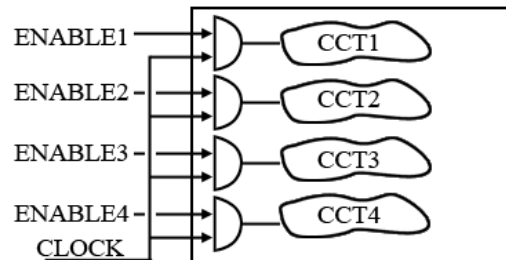
f/2
f/2
f/2
f/2
f/2
f/2
M
M
A
A
MUX
f

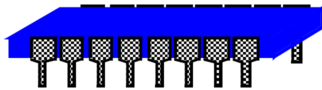
Activity reduction .



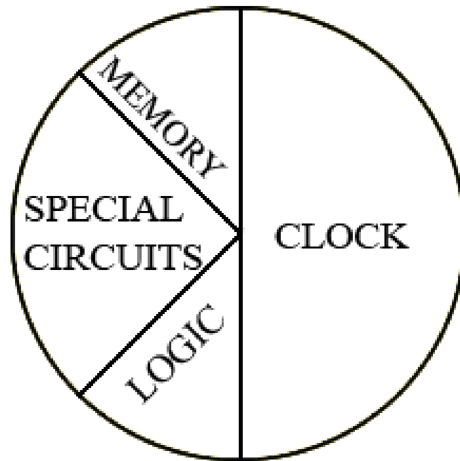




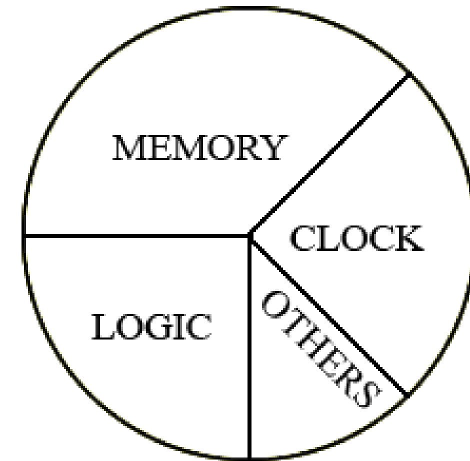




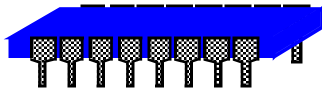
Power Distribution



TYPICAL MICROPROCESSOR POWER CONSUMPTION DISTRIBUTION



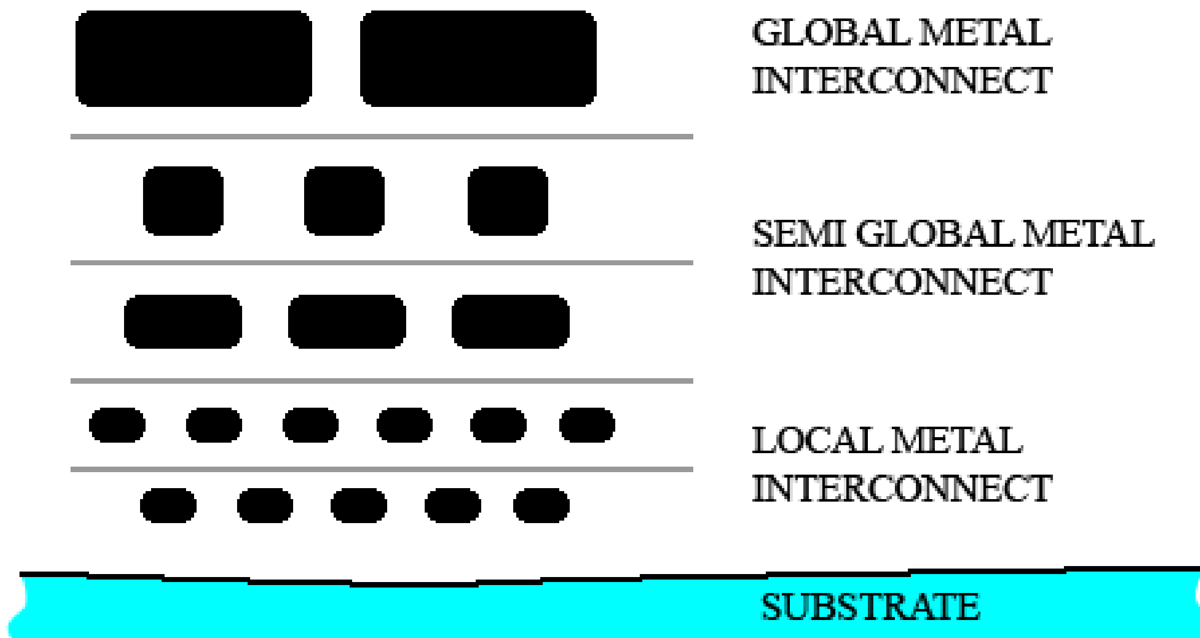
SPECIAL CIRCUITS POWER CONSUMPTION DISTRIBUTION

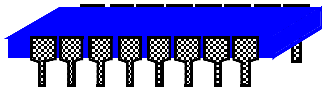


Thank you !

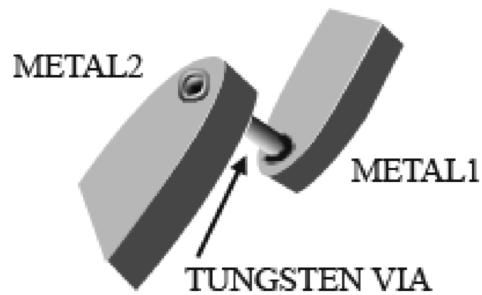
Interconnect

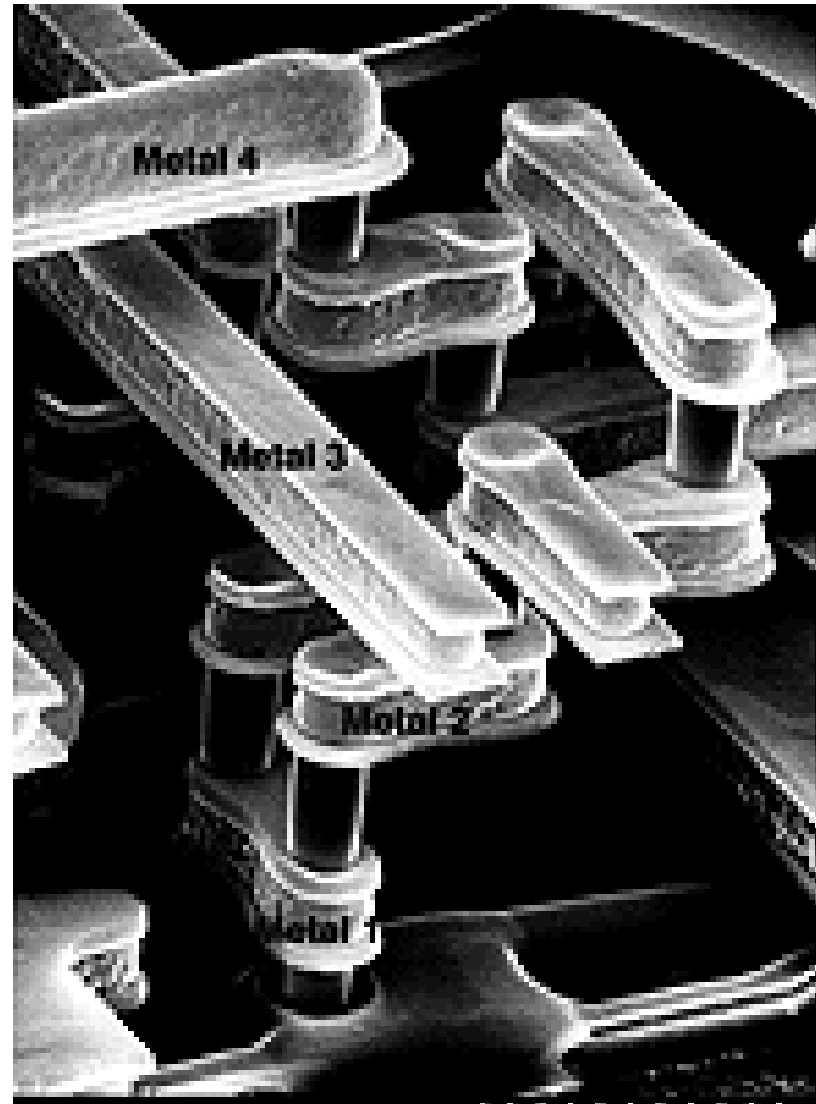
Interconnects in chips are routed in several layers horizontally and vertically and used according to their application

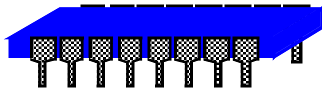




Interconnect/Via







Large Vias

An example of replacing one large contact cut with several smaller cuts to avoid current crowding

1um

1um

Each contact (Via) is of perimeter 4um

METAL1

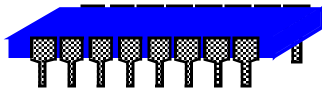
10mA

20 X 1um x 1um VIA

Each carrying 0.5mA

METAL2

10mA



Electromigration

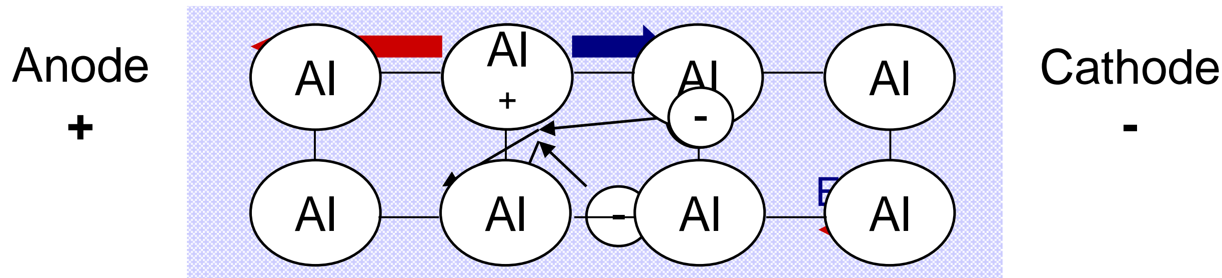
Electromigration is the forced movement of metal ions due to an electric field

$$F_{total} = F_{direct} + F_{wind}$$

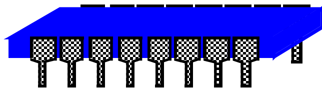
Direct action of electric field on metal ions

<<

Force on metal ions resulting from momentum transfer from the conduction electrons



Note: For simplicity, the term “electron wind force” often refers to the net effect of these two electrical forces

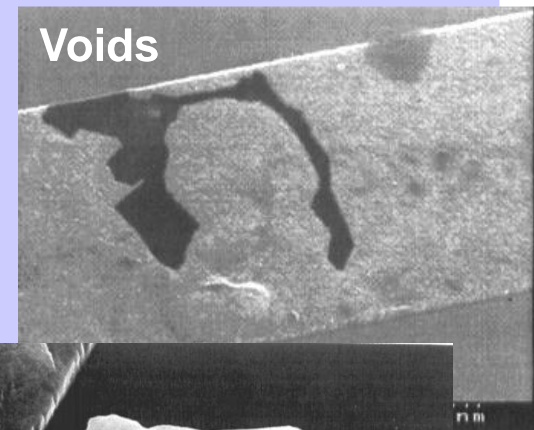


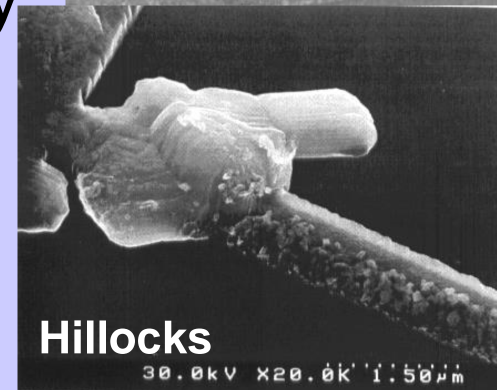
Electromigration

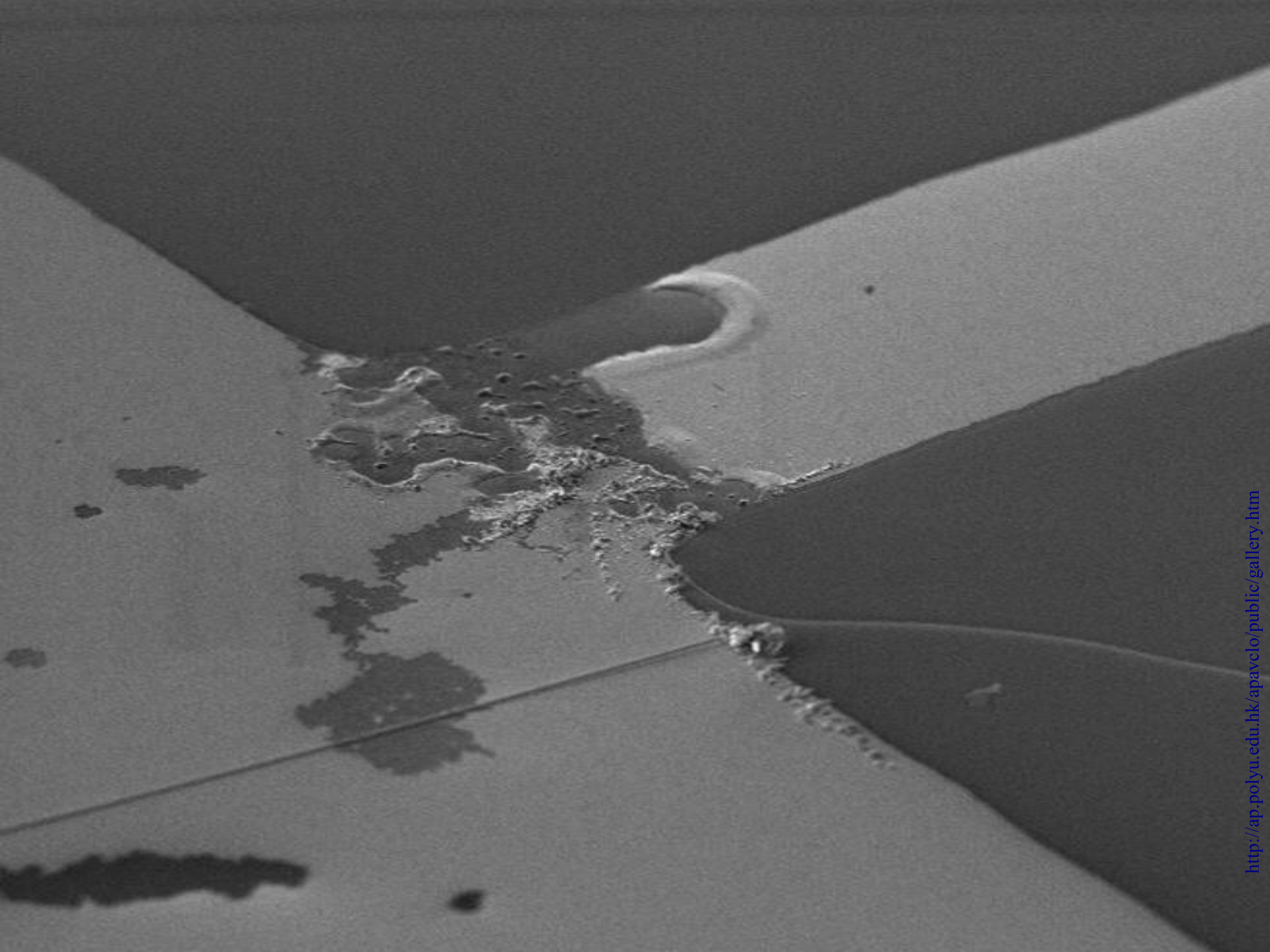
=> Metal atoms (ions) travel toward the positive end of the conductor while vacancies move toward the negative end

Effects of electromigration in metal interconnects:

- Depletion of atoms (Voids):
  - Slow reduction of connectivity
  - Interconnect failure
  - Short cuts (Deposition
- of atoms)



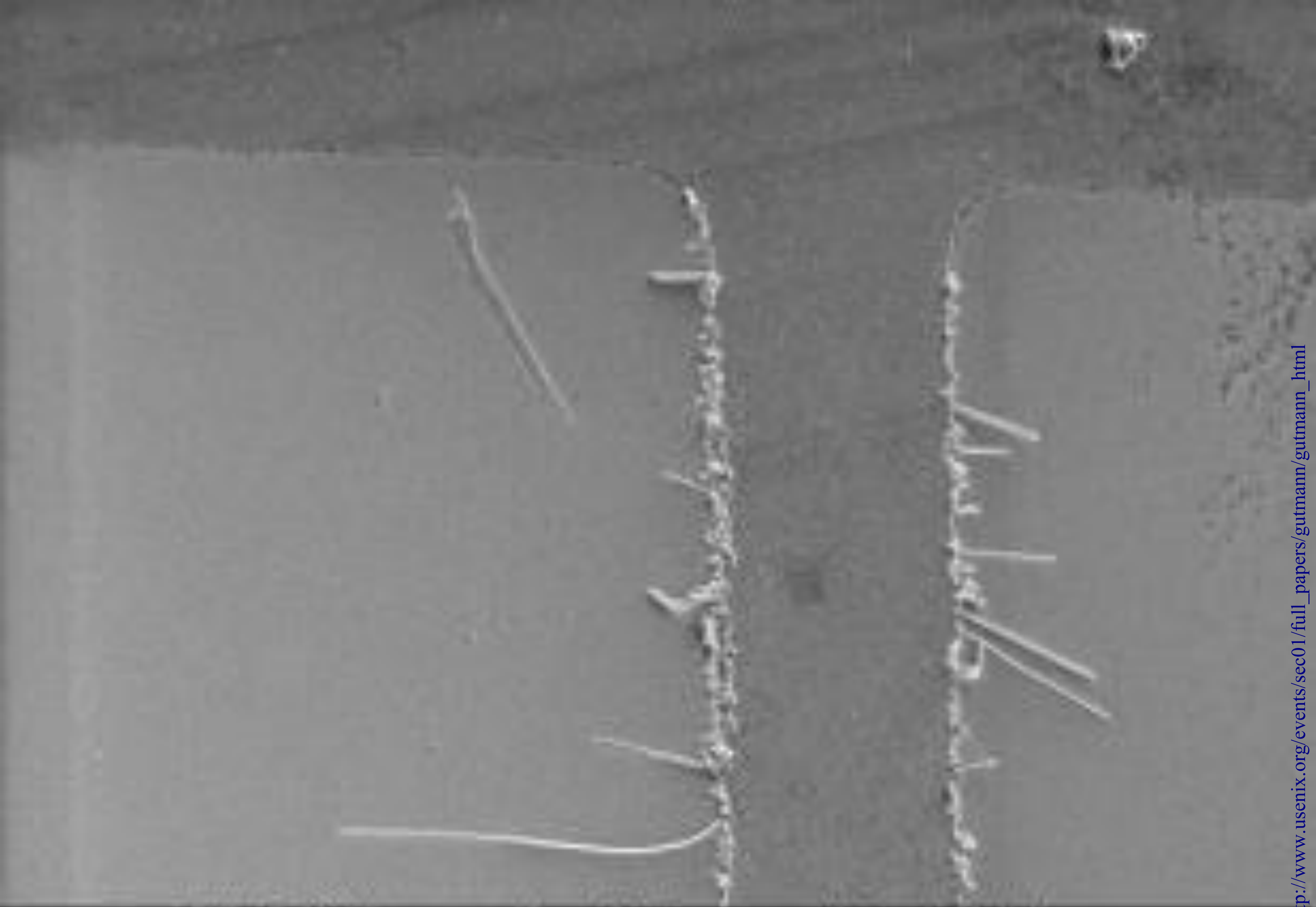




http://ap.polyu.edu.hk/apavclo/public/gallery.htm

EHT= 3.00 kV WD= 11 mm Mag= 2.91 K X
10μm Photo No.=218 Detector= SE1

http://www.usenix.org/events/sec01/full_papers/gutmann/gutmann_html



http://www.usenix.org/events/sec01/full_papers/gutmann/gutmann_html

Metal-2

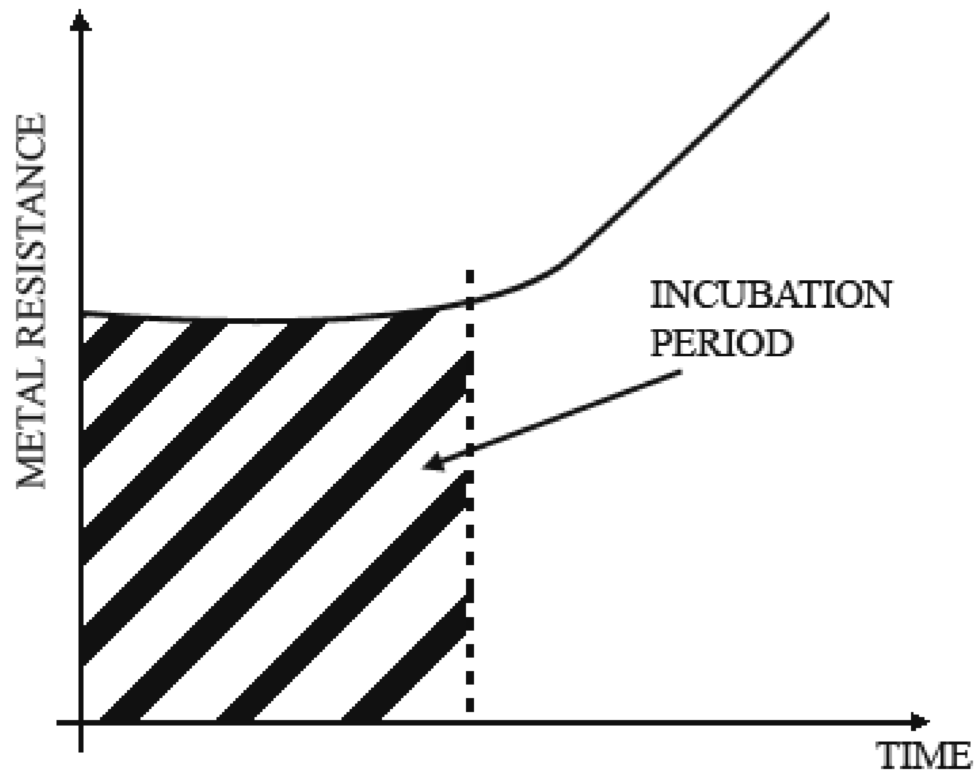
Void

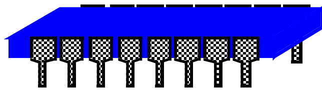
Via

Metal-1

www.lamel.bo.cnr.it/research/ elettronica/em/rel_res.htm

Incubation period





Mean Time To Failure

MTTF

T_1

T_2

T_3

$T_3 > T_2 > T_1$

CURRENT (J)
DENSITY

Mean Time To Failure

DC interconnect, the MTTF is defined as:

$$MTTF_{DC} = AJ_m^{-2} \exp \frac{-E}{kT}$$

A is the area, J_m is the current density, E is 0.5eV,
K is the Boltzsman constant, and T is the absolute temperature.

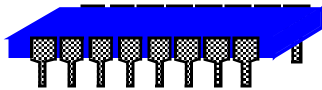
For Ac interconnect the MTTF is defined as

$$MTTF_{DC} = \frac{A \exp \frac{-E}{kT}}{\bar{J}_m \left|\bar{J}_m\right| + k \frac{AC}{DC} \overline{\left|J_m\right|}^2}$$

$\bar{J}_m$ **is the average current density,**

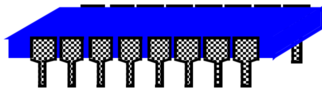
$\left|\bar{J}_m\right|$ **is the average absolute current density and**

$\frac{AC}{DC}$ **is a constant.**



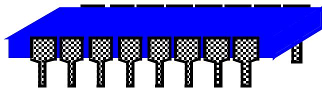
Layout of a controller

http://electronics.stackexchange.com/questions/128120/reason-of-multiple-gnd-and-vcc-on-an-ic



Reasons for having multiple supply lines.

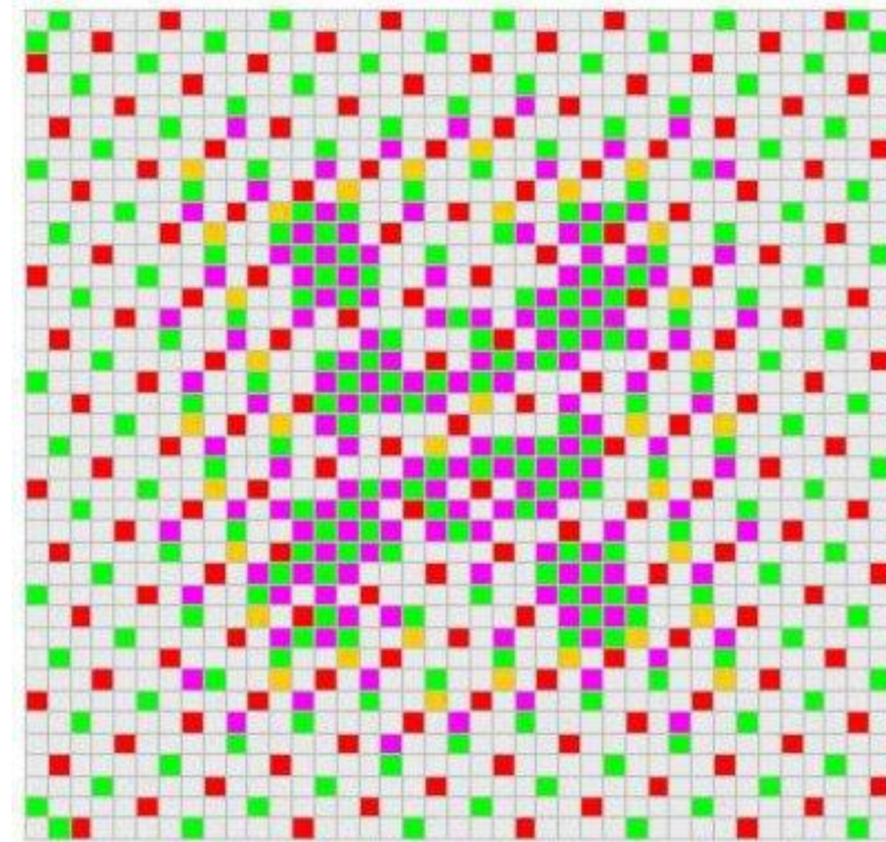
- Current has to be distributed, it is impractical that any pad can take the total current. The resistance drop is prohibiting
- Power coming in from any one pin will probably have to snake it's away around a lot of stuff to get to every part of the device. Multiple power lines gives the device multiple avenues to pull power from, which keeps the voltage from dipping as much during high current events.
- Need for a clean supply voltage at certain areas.
- Analog devices require special attention and probably different voltage supply.
- Heat distrubution, and removal



Xilinx Virtex I/O distribution

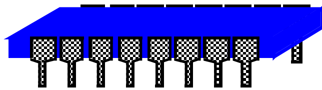
The figure represents all of the power and ground pins on a Virtex 4 FPGA in a BGA package with 1513 pins. The FPGA can draw up to 30 or 40 amps at 1.2 volts

Every I/O pin is adjacent to at least one power or ground pin, minimizing the inductance and therefore the generated crosstalk.



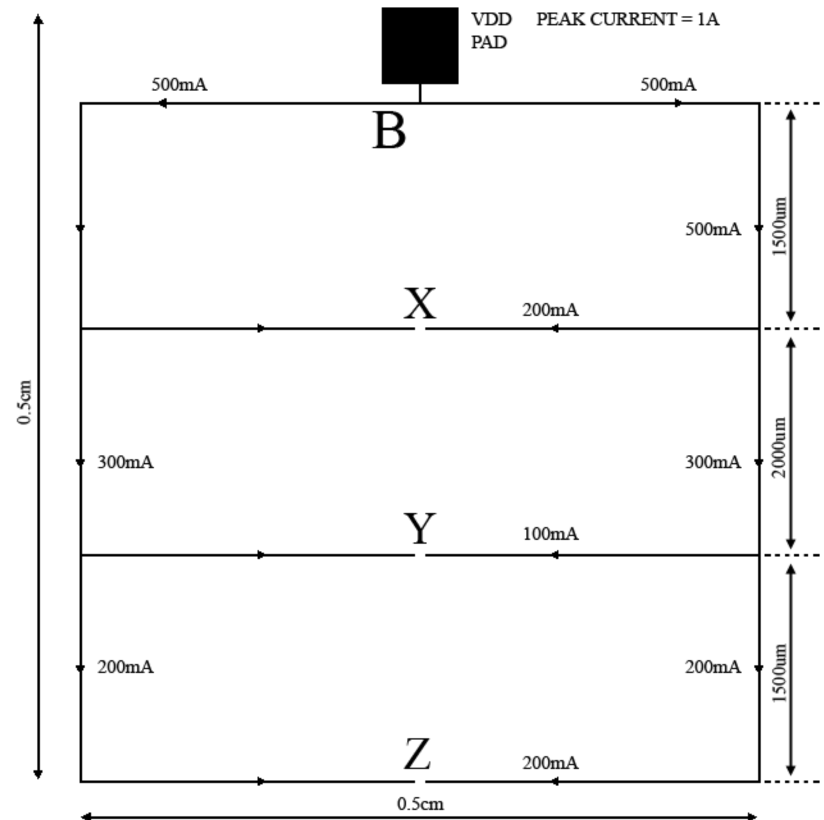
Virtex-4 FF1513 Package

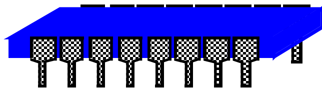
http://electronics.stackexchange.com/questions/128120/reason-of-multiple-gnd-and-vcc-on-an-ic



Example

Assume a chip of 0.5cm by 0.5cm fed by one Vdd pad.
The chip consumes 1A at 3.3Volts.
Determine the voltages on points marked X, Y and Z.
Are these values Acceptable?
What can you do about it?
(assume Jm = 1mA/um2
and a 1µm thick aluminum)





Thank you !