**VLSI Project Proposal**

**DESIGN OF A 4-BIT SUBTRACTOR**

**A Report  
Presented to  
The Department of Electrical & Computer Engineering  
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**In Partial Fulfillment  
of the Requirements  
of COEN 451**

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**ABSTRACT**

**DESIGN OF A 4-BIT SUBTRACTOR  
  
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The purpose of this project is to perform the design, full custom implementation and simulation of a 4-bit subtractor at the transistor level by means of CMOSIS5 technology. Our methodology will aim at designing a 1-bit subtractor and than cascade for instances of this component to manufacture a 4-bit subtractor. Two types of simulation or testbench will be performed in order to ensure that the implementation is fully functional and “factory-ready”. First, a schematic simulation will be performed by means of the “Cadence Schematic Editor and Analog Environment” software. Second, the 4-bit subtractor layout model will be emulated by the “Cadence Virtuoso Editor”. Performing the simulation will mainly consist in evaluating the quality of the output signals in terms of voltage levels, to assess the performance of the circuit in terms of speed, area and power dissipation. Finally, at the completion of the implementation and simulation, a padframe will be designed.

***Keywords: 4-bit Subtractor, 1-bit Subtractor, Cadence, Virtuoso, Padframe***

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1. INTRODUCTION

## Purpose

* To perform the design, full custom implementation and simulation of a 4-bit subtractor at the transistor level by means of CMOSIS5 technology.
* To verify if the circuit can perform with all the possible combinations of the inputs alongside the logic function which it is designed for.
* To evaluate the quality of the output signals in terms of voltage levels.
* To assess the performance of the circuit in terms of speed, area and power dissipation.

## The Need

The CMOSIS5 package incorporates the “Cadence Schematic Editor and Analog Environment” software used to create a schematic diagram and a simulation of our implementation. Moreover, it contains the Cadence Virtuoso Editor which will allows us to design the layout of the 4-bit subtractor, as well as an option known as “HSPICE Netlist” which automatically performs the assessment of several performance parameters for the circuit. In addition, both transient and DC analysis will be performed in conjunction with “HSPICE Netlist” in order to present a meticulous evaluation. The project specifications offered a wide selection varying between two types of implementations, each with an analogous kind of difficulty. Nevertheless, we chose the design of a 4-bit subtractor in order to understand the concept of cascading and how the power dissipation in static CMOS circuits can be minimized while trying to maintain the area as much as possible.

## System Requirements

A 4-bit subtractor is not an extremely complex circuit to be implemented in VLSI. The latter circuit will be designed and implemented to have two outputs such as  and  with three inputs such as ,  and . Furthermore,  is said to be the “borrow-in” while  is known as “borrow-out” bit. The two inputs X and Y are to be subtracted while outputs D or “Difference” and bout are all 4-bit numbers.

Furthermore, the simulation is to be implemented via the “Cadence Schematic Editor and Analog Environment” to provide a testing coverage of all possible cases that can be encountered in order to make sure that the design is operational. **Figure 1** below illustrates the block diagram pertaining to our design:

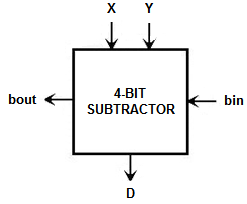


Figure : 4-bit Subtractor Block Diagram

More specifically, the 4-bit subtractor consists of four single-bit cascaded subtractors. One can clearly notice from **Figure 2** how the “borrow-in” bit navigates throughout the circuit:

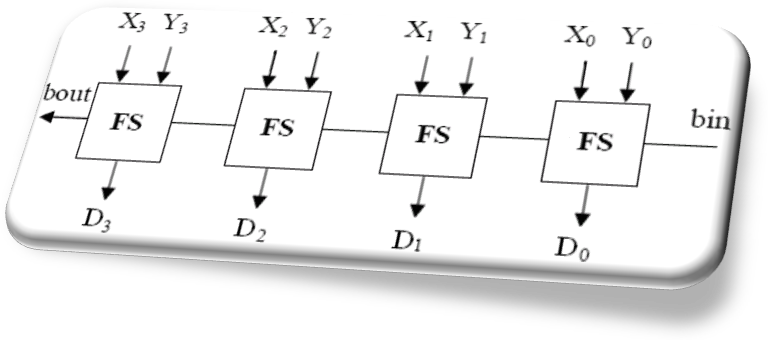


Figure : Logic Diagram of the 4-Bit Full-Subtractor

Overall, the truth table describing the operation of a single 1-bit subtractor schematic is depicted in **Table 1** below:

Table : Truth Table of a 1-bit Subtractor

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **bin** | **X** | **Y** | **bout** | **D** | **Comment** |
| 0 | 0 | 0 | 0 | 0 | 0-0-0 = 0, No Borrow |
| 0 | 0 | 1 | 1 | 1 | 0-0-1 = -1, Borrow 2 and 2-1 = 1 |
| 0 | 1 | 0 | 1 | 1 | 1-0-0 = 1, No Borrow |
| 0 | 1 | 1 | 0 | 0 | 1-0-1 = 0, No Borrow |
| 1 | 0 | 0 | 1 | 1 | 0-1-0 = -1 (bin=1), Borrow 2 and 2-1 = 1 |
| 1 | 0 | 1 | 0 | 0 | 0-1-1=-2, Borrow 2 and 2-2 = 0 |
| 1 | 1 | 0 | 0 | 0 | 1-1-0 = 0, No Borrow |
| 1 | 1 | 1 | 1 | 1 | 1-1-1 = -1, Borrow 2 and 2-1 = 1 |

## Performance Assessment

As previously discussed, the implementation of a circuit must be validated by several performance parameters which can be gathered from the “HSPICE Netlist” and both transient and DC analysis. Additionally, the assessment of the performance of each circuit in our project will be limited to: the speed relationship, propagation delay, voltage variation, power dissipation and overall circuit performance. In this section, we will briefly explain the methodology of each analysis and the concept of power dissipation.

### Transient Analysis

We will further understand the transient characteristics of the 4-bit subtractor by observing and comparing the timing measurements such as the propagation delays ,  and the rise time or fall time . The latter parameters are defined respectively below:

* **tr**is the rise time of the output signal.
* **tf** is the fall time of the output signal.
* **tPHL**is the propagation delay high to low.
* **tPLH**is the propagation delay low to high.

Furthermore, the latter parameters are illustrated in **Figure 3** below:

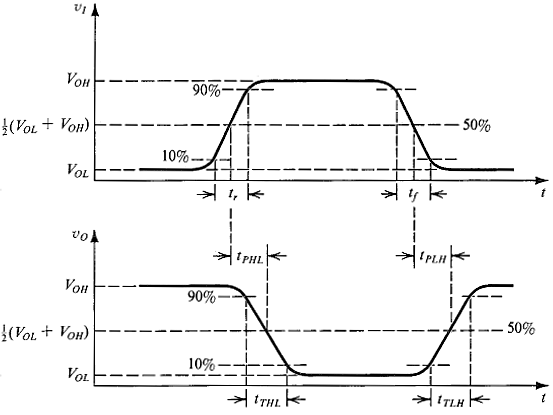


Figure : Propagation Delays and Switching Times of the CMOS Inverter [1]

Transient analysis offers several options which will be described briefly in this section:

Outputs verification:

This verification is achieved by graphically comparing the timing diagrams with the theoretical results for every input combination according to the truth table of the circuit under test.

Voltage levels evaluation:

The evaluation of the output voltage level is performed graphically by means of the “Cursor” tool in the “Cadence Analog Design Environment”. Afterwards, a comparison will be done with the expected output from the truth table.

Propagation delay estimation:

The time delays and  for the outputs can be calculated as soon as the input reaches  until the output reaches as well. Thus, the accuracy of the measurements was additionally increased. The critical input combination was determined by assessing the transient analysis plot for a given output, using the cursors and by finding the combination of inputs yielding optimum  and . The propagation delay was finally calculated using the formula below:

****

### DC Analysis

The functionality and performance of the 4-bit subtractor will be tested by observing and comparing the input and output voltages or its DC characteristics. The study of the input and output signals of a CMOS based circuit is also known as Voltage Transfer Characteristic or VTC. The Voltage Transfer Characteristic is illustrated below in **Figure 4**:

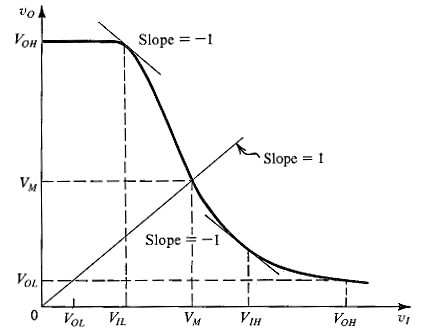


Figure : The Typical Voltage Transfer Characteristic (VTC) of the CMOS Inverter [1]

The DC sweep analysis was performed by replacing the VPULSE voltage source connected to any input by a DC source. The value of the voltage at the other input was changed from  to  in increments of and the voltages at the outputs were monitored. In addition, the plot of the DC voltage transfer characteristic can help us determine several important parameters such as:

* **VOH**corresponds to the output high voltage
* **VOL**corresponds to the output low voltage
* **VIL** also called input low voltage. It is defined as being the maximum value of the input voltage still considered by the inverter as low level. Graphically, VIL corresponds to the slope of value -1.
* **VIH**also known as input high voltage is the minimum value of the input voltage which is considered by the inverter as high level. It is found graphically to correspond to the slope of value -1.
* **VM = Vth** is defined as being the threshold voltage of the CMOS inverter determined at the curve slope of 1.

Moreover, from the data recorded one can find the noise margins using the following equations:

**Noise Margin Low:** 

**Noise Margin High:** 

### Power Dissipation

In this section we will discuss the two main power components such as the static and dynamic power dissipation which in general contribute greatly to the power dissipation in CMOS circuits. The total power is engendered on the basis of four sub-components which are outlined in **Figure 5**. Since optimizing the power consumption in our 4-bit subtractor implementation is the primary objective of our object, we will spend extra time in order to improve this aspect of the circuit. Moreover, the total power consumption can be found by the means of the following formula below:



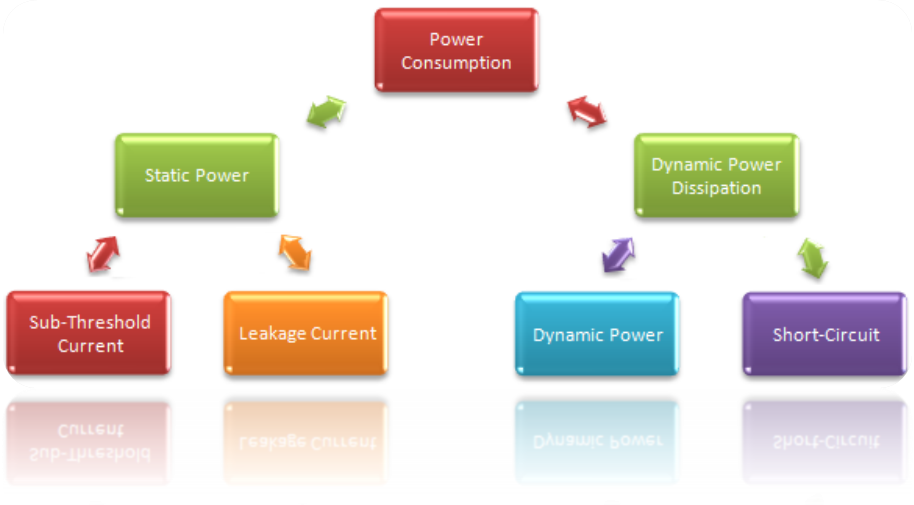


Figure : Power Dissipation Chart

Consequently, one can find the power for the four different components of the total power by means of the following steps and equations:

**Step1: Leakage current**



**Step2: Sub-threshold current**

The sub-threshold current will be neglected.

**Step3: Short-circuit current**

During the transition due to input signal whenever the PMOS and NMOS are both ON, a direct path exits between  and  and therefore . At last, the short circuit power dissipation is given by:



**Step4: Dynamic power**

The dynamic power dissipation is a phenomenon that arises when charging or discharging power dissipation. This latter can be calculated by means of the following equation:

 where:

 Parasitic Capacitance

 Supply Voltage

 Activity rate

 Switching Frequency

 Period

Although several performance parameters are available, our implementation and conceptual goals will be focused on providing a system which will have the bare minimum power dissipation while maintaining efficient clocking capability.

**Step5: Total static power consumption**

The static power dissipation is the average static power dissipated by each of the circuits. Moreover, this latter arises from the sub-threshold current or the leakage current which is due to junction reverse biased currents. The static power dissipation can be calculated by means of the equation shown below:

, where 

## Research Overview and Limitations

After introducing the theory relevant to the project, we will introduce in details the concepts and methodologies behind the implementation of the 4-bit subtractor by segregating the latter circuit in small components. Next, we will present the design and simulation results obtained for the entire circuit. Afterwards, we will discuss the simulation or experimental results obtained by comparing these to the anticipated outcome, and by assessing the performance of our circuit in terms of speed and power dissipation. Finally, we will conclude the simulation project by summarizing the objectives, simulation results and the errors encountered during the design and implementation of the circuitry.

1. CONCEPTUAL DESIGN AND METHODOLOGY

In this section, we will discuss in details the implementation of each component of the 4-bit subtractor. In addition, the logic design and diagram of the 4-bit subtractor will be discussed and the basic components needed to perform such implementation will be meticulously enumerated.

## Logic Design Analysis

This section discusses the basics of digital subtraction. In fact, we generated two different Karnaugh-Maps with one for each output as shown in **Figure 6** below:

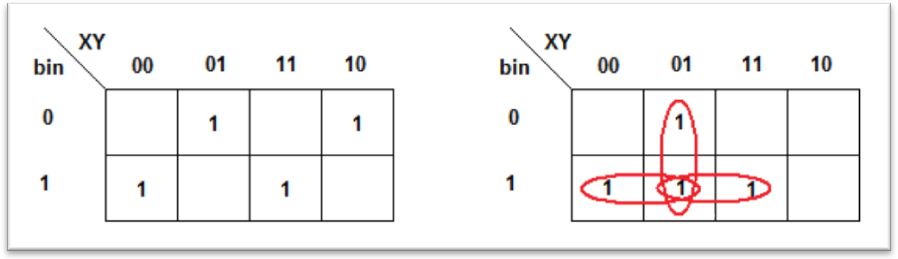


Figure : Karnaugh-Maps of 1-bit Subtractor

Furthermore, from the Karnaugh-Maps above we were able to obtain the state equations. The resulting equations for a 1-bit subtractor are shown below:

**For the difference or D:**



**For the borrow-out or bout:**



The concept here is very simple: we are looking to implement a 4-bit subtractor by means of a series of *four* 1-bit subtractors as shown in **Figure 2** previously. Moreover, there are two possible implementations of the transfer functions; however, we chose only the one which had fewer transistors since it will be more power efficient. The implementation of the 1-bit subtractor is represented in **Figure 7** below:

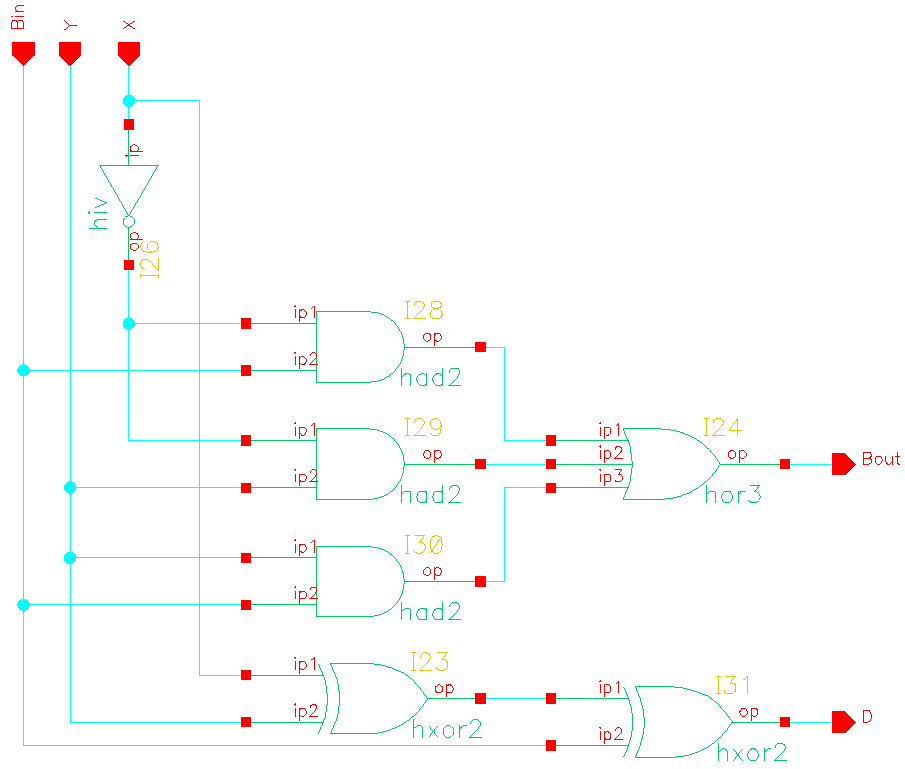


Figure : Implementation of a 1-bit Subtractor

## 4-bit Full Subtractor Synthesis

In addition, the derived 4-bit subtractor circuit is illustrated in **Figure 8** below:

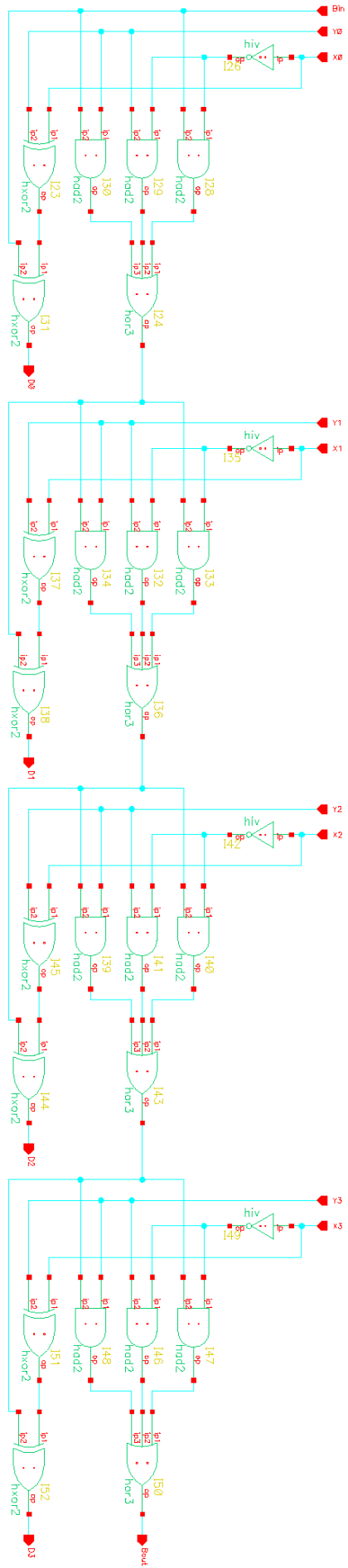


Figure : Conceptual 4-bit Subtractor Implementation

The design of the 4-bit subtractor might seem a little bit more complex than what it looks like in reality due to the complexity of **Figure 8**. Indeed, we can clearly observe that the quantity of several instances is quadrupled in order to obtain a 4-bit subtractor. The inventory of the type and amount of gates needed is show below in **Table 2**:

Table : Table of Primitive Components

|  |  |  |  |
| --- | --- | --- | --- |
| **Table of Primitive Components** | | | |
| **Gate** | **Quantity** | **Transistors** | **Total** |
| **Inverter NOT** | 4 | 8 | 32 |
| **2- input AND** | 12 | 72 | 864 |
| **2- input XOR** | 8 | 80 | 640 |
| **3- input OR** | 4 | 32 | 128 |
| **Total** |  |  | 1664 |

From **Table 2** above, we can clearly see that the 4-bit subtractor implementation consists of 1664 transistors such as: NOT, AND-2, OR-3 and XOR-2 gates. In the subsequent section, we will examine each component independently.

## Basic Components

Our implementation consists of *four* types of logic components such as such as inverters, 2-input AND gates, 3-input OR gates and 2-input XOR gate. We will further and briefly investigate the operation of each gate in function of their operation, PUN or Pull-Up Network, PDN or Pull-Down Network and logic implementations.

### Inverter (NOT)

An inverter gate usually output signals either representing a “true” or “false”. In this case, the inverter’s output  is true when the input  is “false”. Therefore, we can write the inverter logic equation which is given by the following equation:

, where  is the inverted input and  the output.

Moreover, the truth table below shows the function of the inverter logic gate:

Table : Truth Table of an Inverter

|  |  |
| --- | --- |
| **IN** | **OUT** |
| 0 | 1 |
| 1 | 0 |

The inverter logic gate will be implemented using CMOSIS5 technology as show in **Figure 9** below:

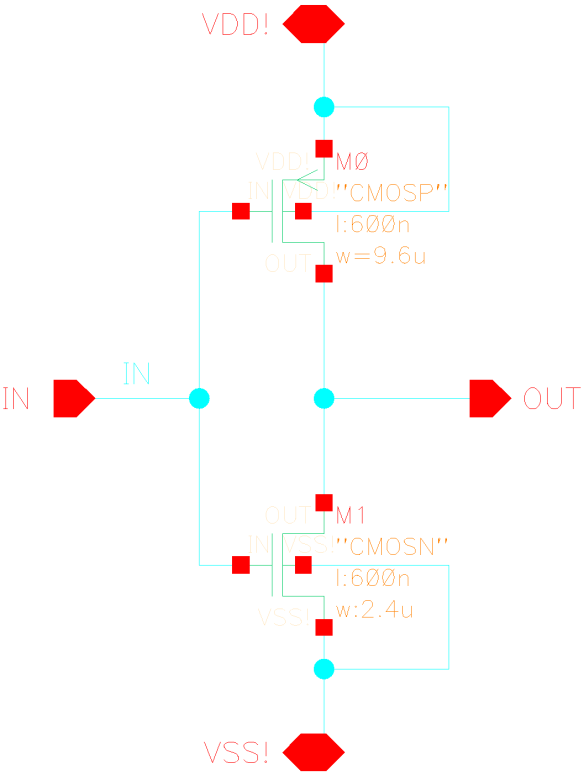


Figure : CMOS Inverter Circuit

### 2-input AND (AND-2)

A 2-input AND gate usually output signals as “true” when inputs  and  are both “true”. Therefore, we can write the 2-input AND logic equation which is simply provided by the following equation below:

, where  and  are the inputs and  being the output.

Moreover, the truth table below shows the operation of the 2-input AND logic gate:

Table : Truth Table of a 2-input AND Gate

|  |  |  |
| --- | --- | --- |
| **IN1** | **IN2** | **OUT** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The 2-input AND logic gate will be designed by means of CMOSIS5 as show in **Figure 10** below:

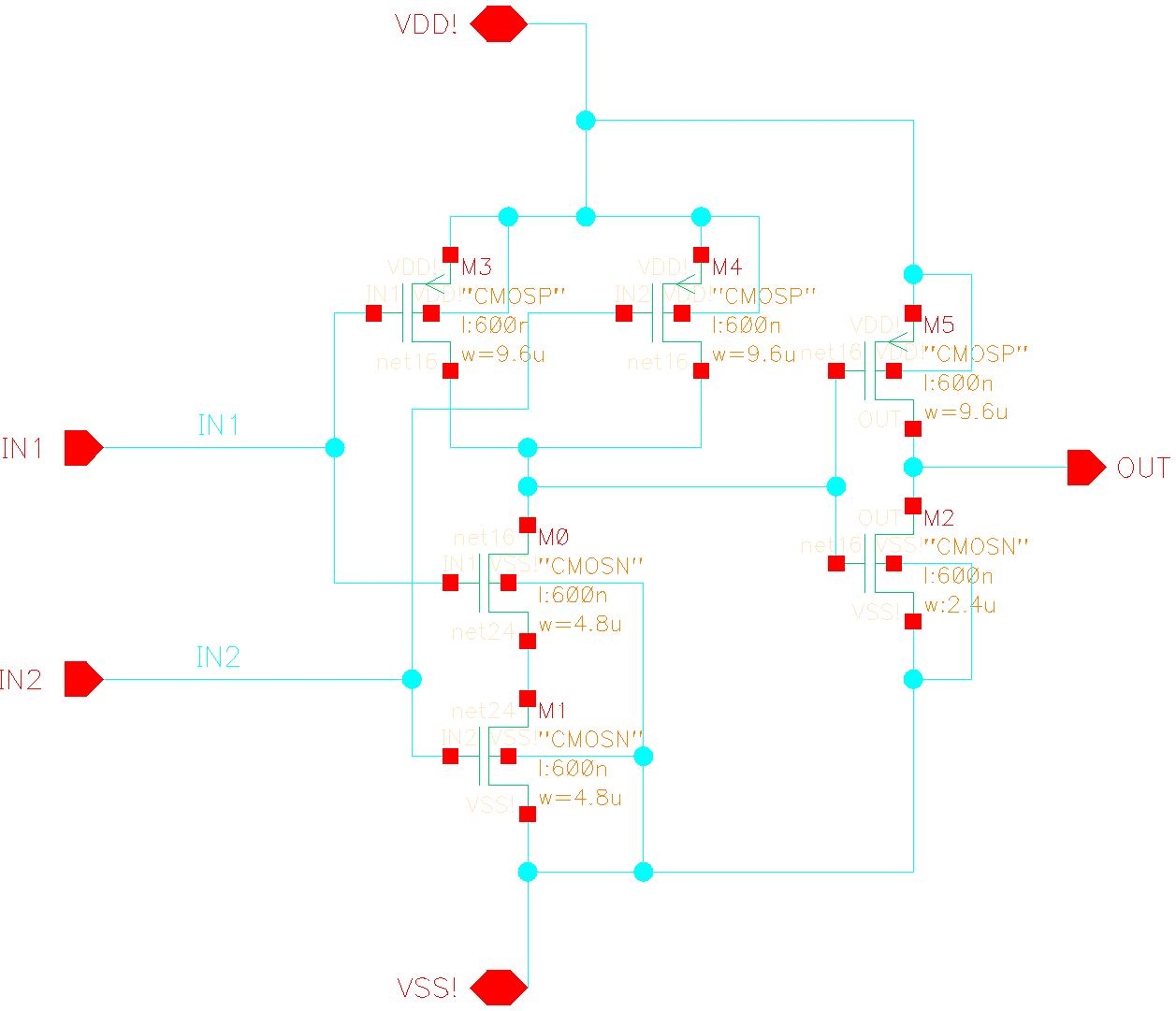


Figure : 2-input AND Gate (AND-2)

### 2-input XOR (XOR-2)

The 2-input XOR logic equation is basically provided by the following equation below:

, where  and  are the inputs and  being the output.

Moreover, the truth table below shows the operation of the 2-input XOR logic gate:

Table : Truth Table of a 2-input XOR Gate

|  |  |  |
| --- | --- | --- |
| **IN1** | **IN2** | **OUT** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The 2-input XOR logic gate will be designed in CMOSIS5 as show in **Figure 11** below:

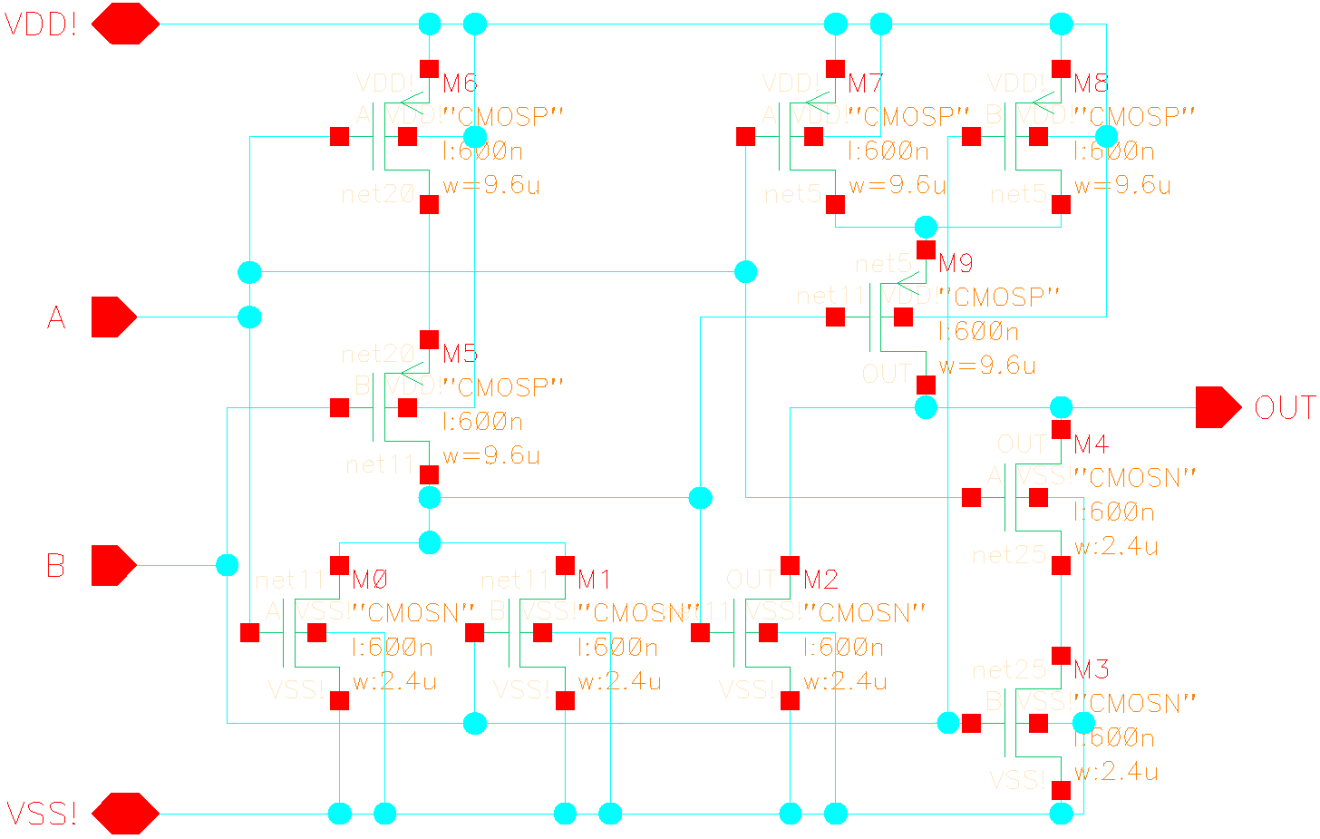


Figure : 2-input XOR Gate (XOR-2)

### 3-inputs OR (OR-3)

The 3-input OR logic equation is basically provided by the equation below which describes its mode of operation:

, where , and  are the inputs and  the output. Moreover, the truth table below shows the operation of the 3-input OR logic gate:

Table : Truth Table of a 2-input XOR Gate

|  |  |  |  |
| --- | --- | --- | --- |
| **IN1** | **IN2** | **IN3** | **OUT** |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

The 2-input XOR logic gate will be designed in CMOSIS5 as show in **Figure 12** below:

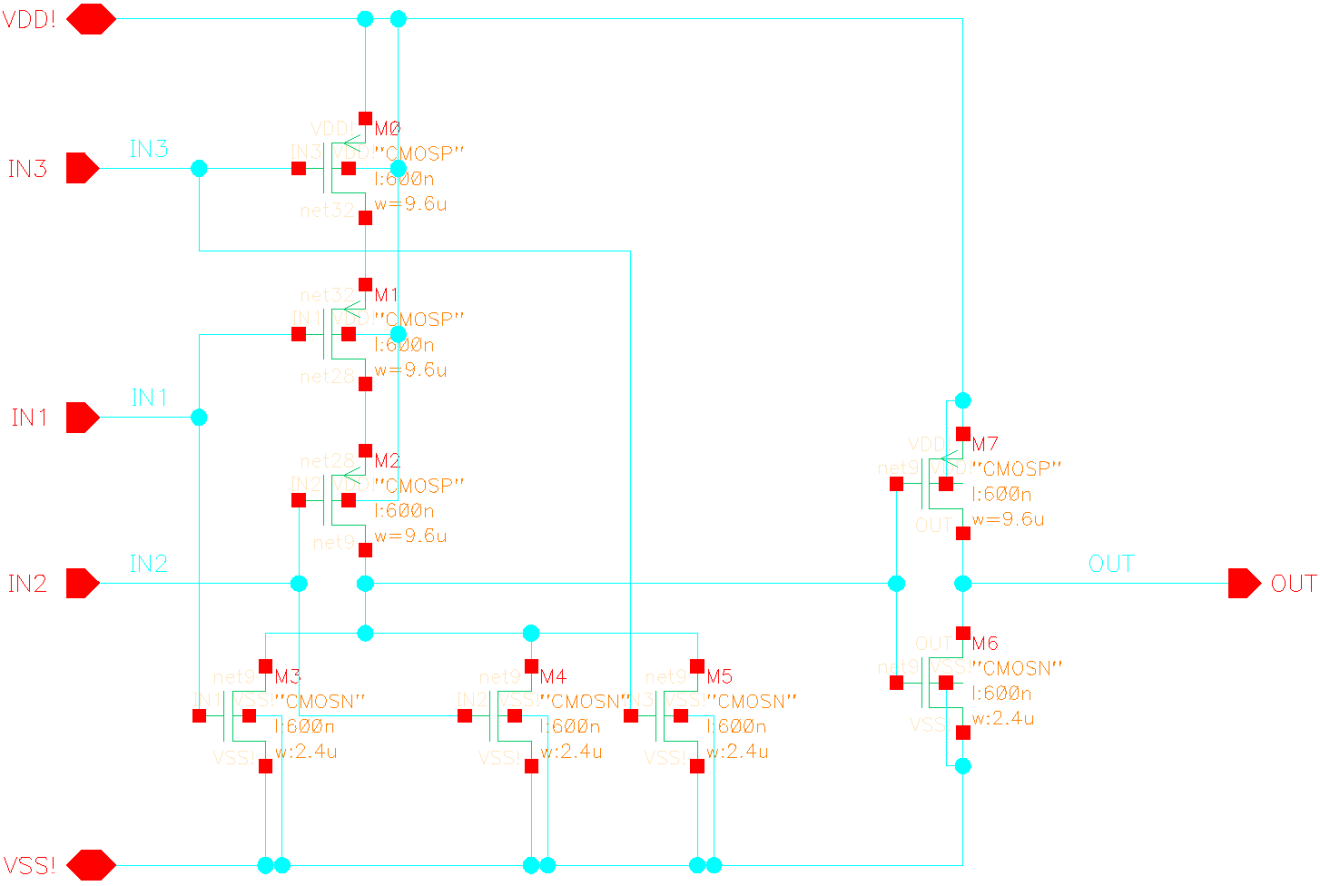


Figure : 3-input OR Gate (OR-3)

## Theoretical Transistor Sizing

In this section we will perform the computation of the width and length parameters or  for the PMOS and NMOS transistors that should be expected for a simple inverter. Subsequently, the latter parameters will be used to globally size the PUN and PDN transistors across the 4-bit subtractor. In addition, one needs to correctly size the NMOS and PMOS transistors of the subtractor in order to improve the performance of the circuit whether it is for:

* Equal rise time and fall time .
* Optimum Area
* Optimum Speed

In this case, we will choose to have an equal rise time  and fall time . Afterwards, we took into consideration the area and the power dissipation. Therefore, we obtained:



The ratio of the transistor for the CMOSIS5 technology was found to be:



Finally, the length and width of both the NMOS and PMOS transistor were found accordingly and represented in **Table 7** below:

Table : Sizing Parameters for the NMOS and PMOS Transistors

|  |  |  |
| --- | --- | --- |
| **Sizing Parameters (µm)** | **NMOS Transistor** | **PMOS Transistor** |
| **Length** | 0.6 | 0.6 |
| **Width** | 2.4 | 9.6 |

1. SIMULATION RESULTS

In the third task of our experiment, the implementation of the 4-bit subtractor circuit will be performed progressively by implementing and creating instances of the components independently. Subsequently, we will merge all the components together to create the 1-bit subtractor. At last, we will obtain the 4-bit subtractor by cascading four instances of the 1-bit subtractor created.

This section will be broken into two main parts. First, we will perform the step by step implementation and simulation of the 4-bit subtractor by means of the “Cadence Schematic Editor and Analog Environment”. Secondly, we will achieve the same implementation by designing gradually the layout of the 4-bit subtractor by means of the “Cadence Virtuoso Editor”. Finally, we will record the transient and DC experimental results for both simulations.

## Cadence Schematic Editor Simulation

The implementation of the 4-bit subtractor circuit was performed by means of the “Cadence Schematic Editor and Analog Environment” by progressively designing and simulating the inverter, 2-input AND, 2-input XOR, 3-input OR logic gates separately and progressively as described below.

### Inverter

First the implementation of an inverter schematic was carried out through the editor by generating the component as shown in **Figure 13** below:

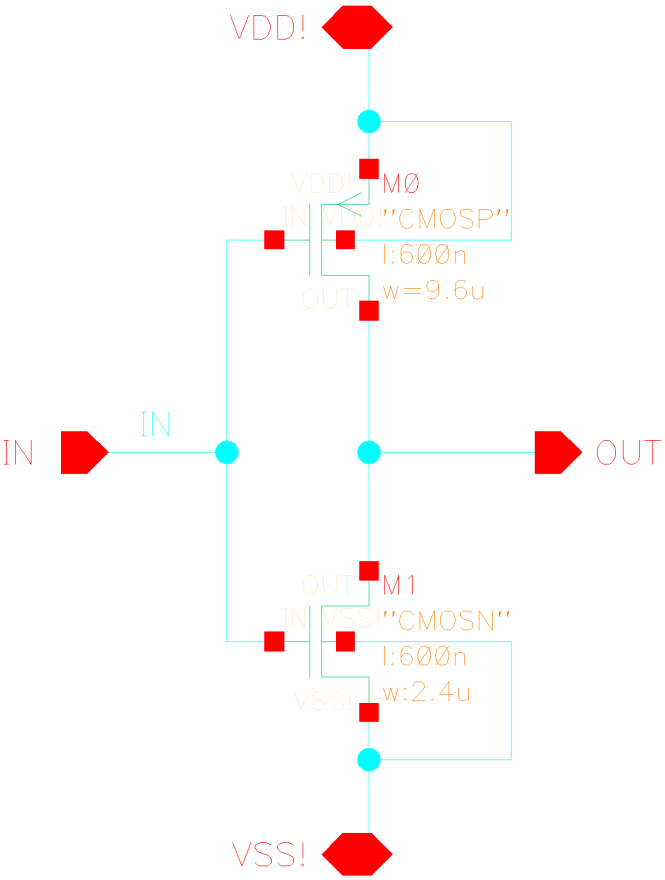


Figure : Inverter Circuit

The inverter was subsequently simulated to ensure its correct functionality. After performing a transient simulation we obtained the output waveform in **Figure 14** below:

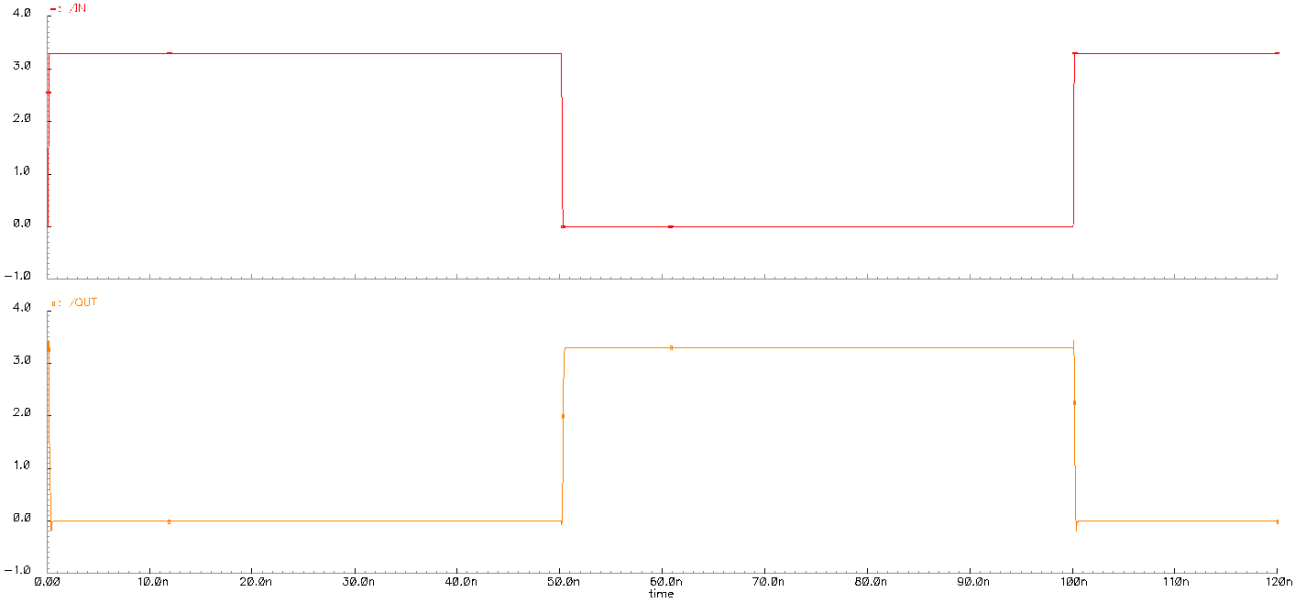


Figure : Inverter - Transient Response

### 2-Input AND Gate

Afterwards, the implementation of the 2-input AND gate circuit was performed through the editor by generating its component as shown in **Figure 15** below:

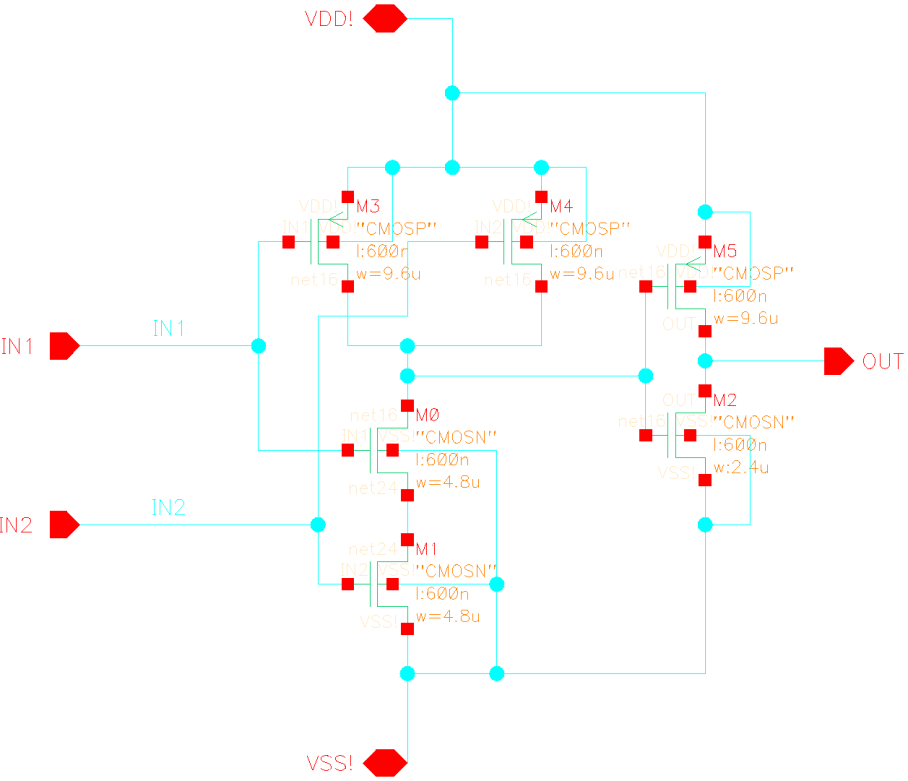


Figure : 2-Input AND Gate Circuit

The 2-input AND gate was subsequently simulated. After performing a transient simulation we obtained the output waveform in **Figure 16** below:

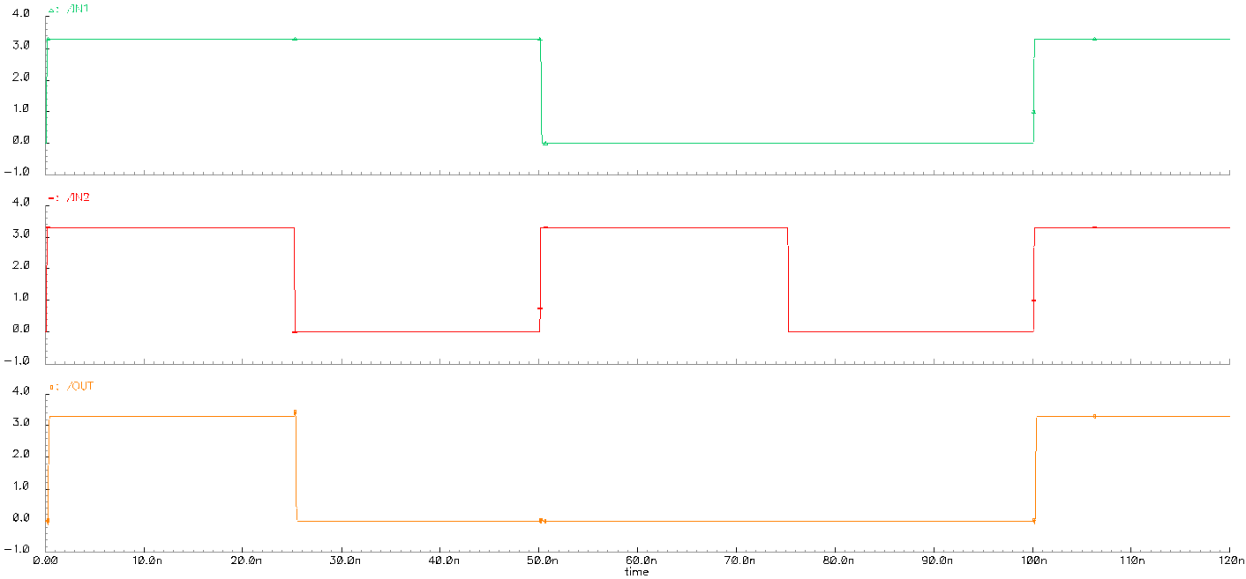


Figure : 2-Input AND Gate - Transient Response

### 2- Input XOR Gate

Subsequently, the design of the 2-input XOR gate circuit was performed as shown in **Figure 17** below and its component was generated:

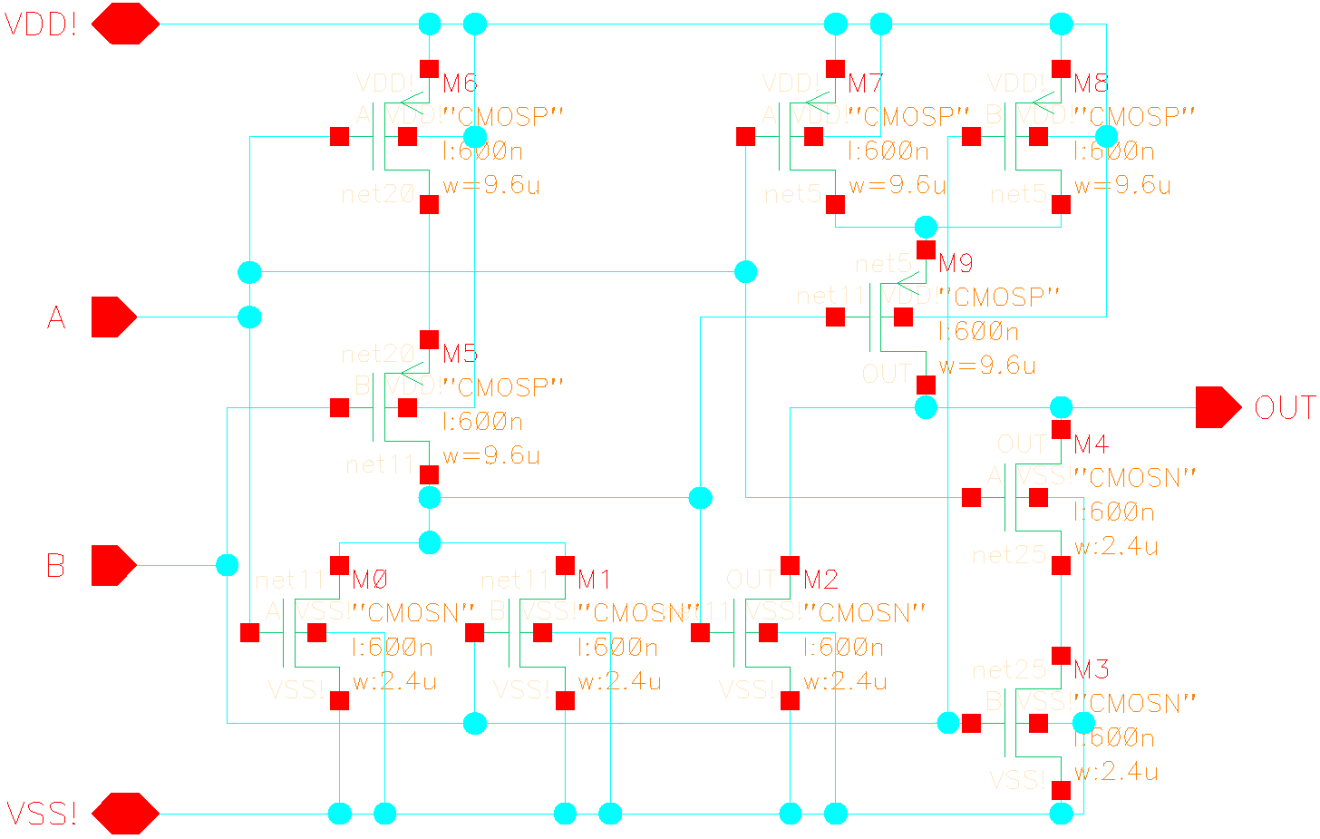


Figure : 2-Input XOR Gate Circuit

A transient simulation was performed in order to obtain the output waveform as shown in **Figure 18** below:

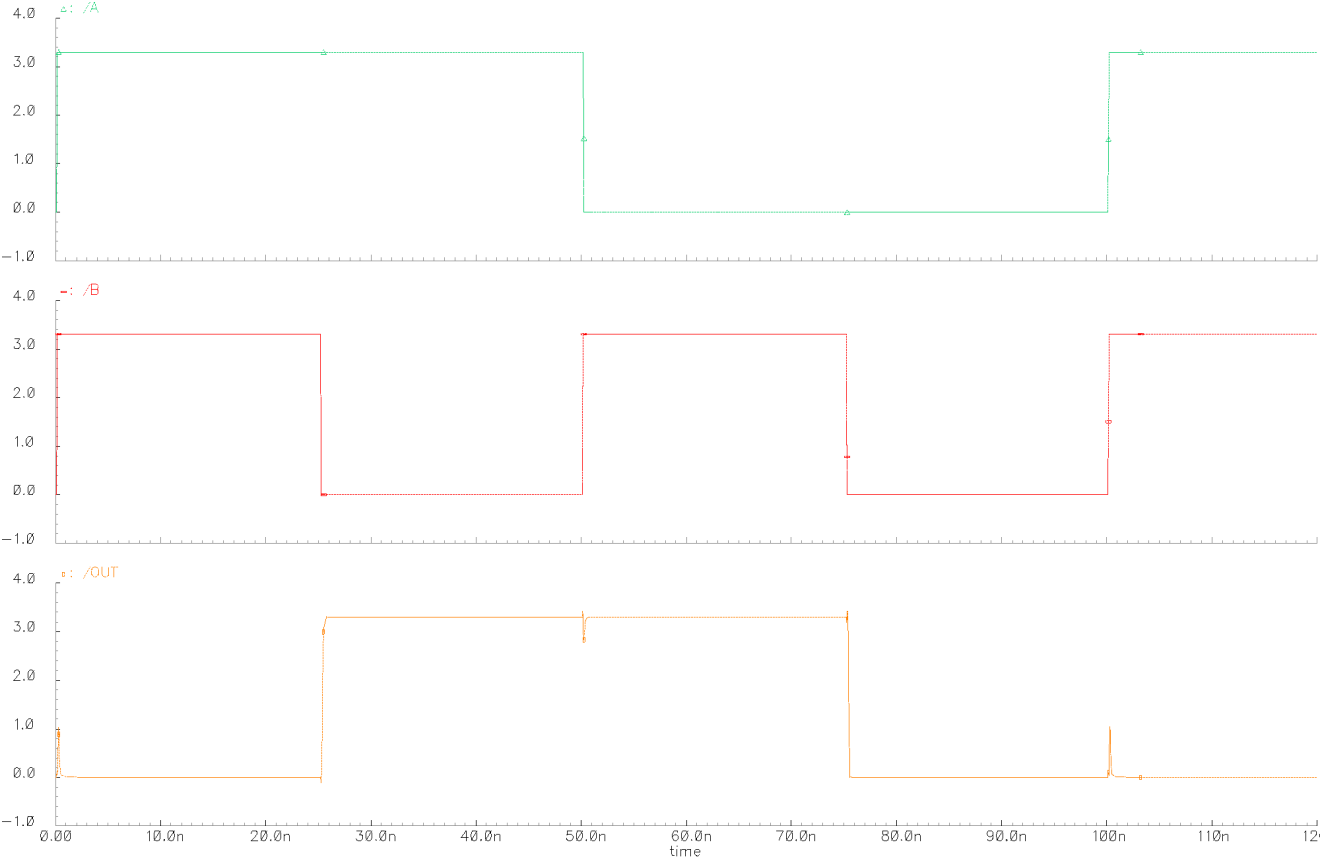


Figure : 2-Input XOR Gate – Transient Response

### 3- Input OR Gate

The design of the 3-input OR gate circuit was performed as shown in **Figure 19** below and its component was generated:

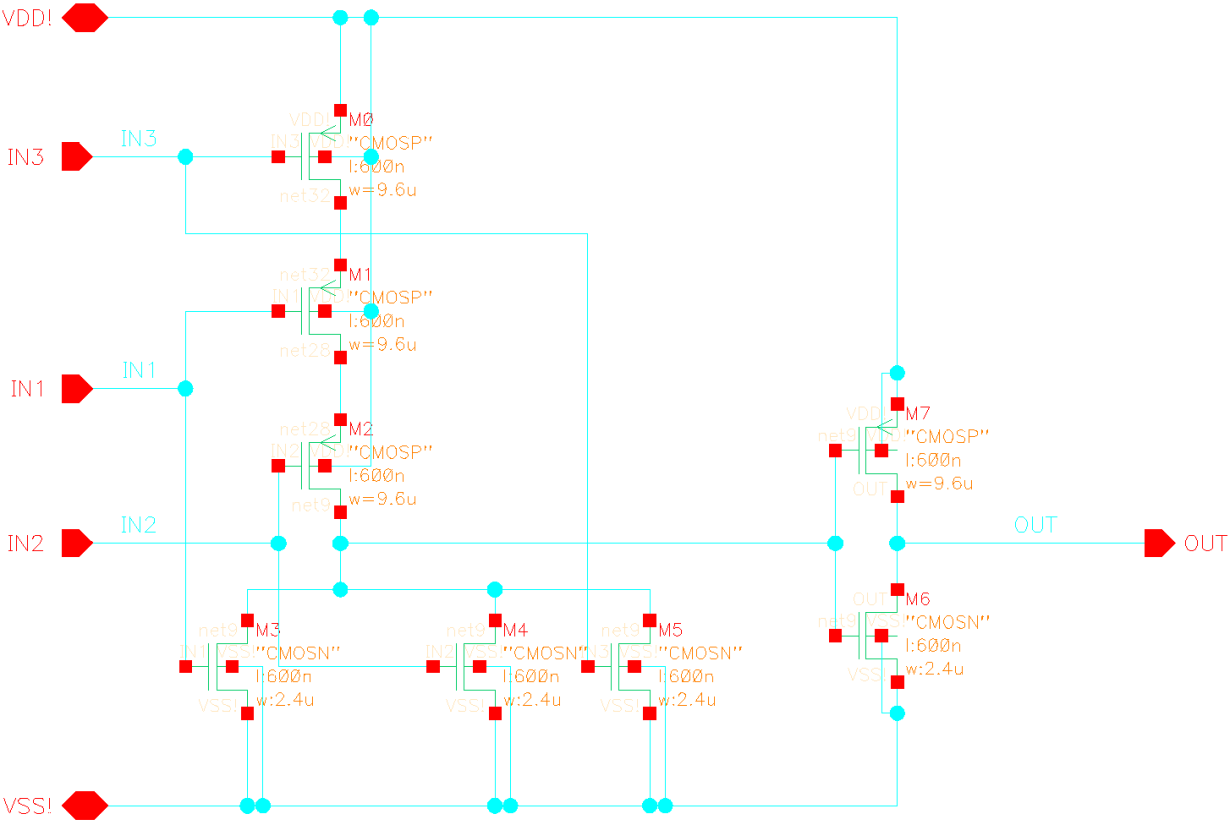


Figure : 3-Input OR Gate Circuit

A transient simulation was then performed to obtain the output waveform below:

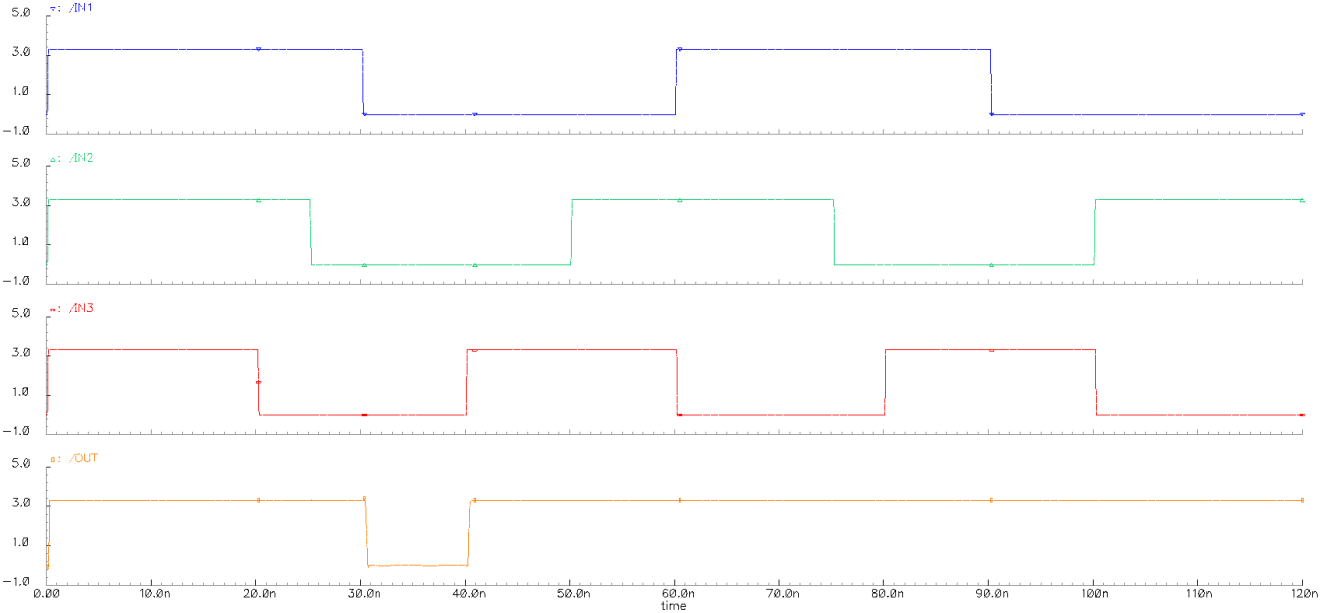


Figure : 3-input OR Gate - Transient Response

### 1-bit Subtractor

The 1-bit subtractor was generated by implementing the circuit of **Figure 7**. The resulting circuit is a circuit containing all the previous instances as shown below in **Figure 21**:

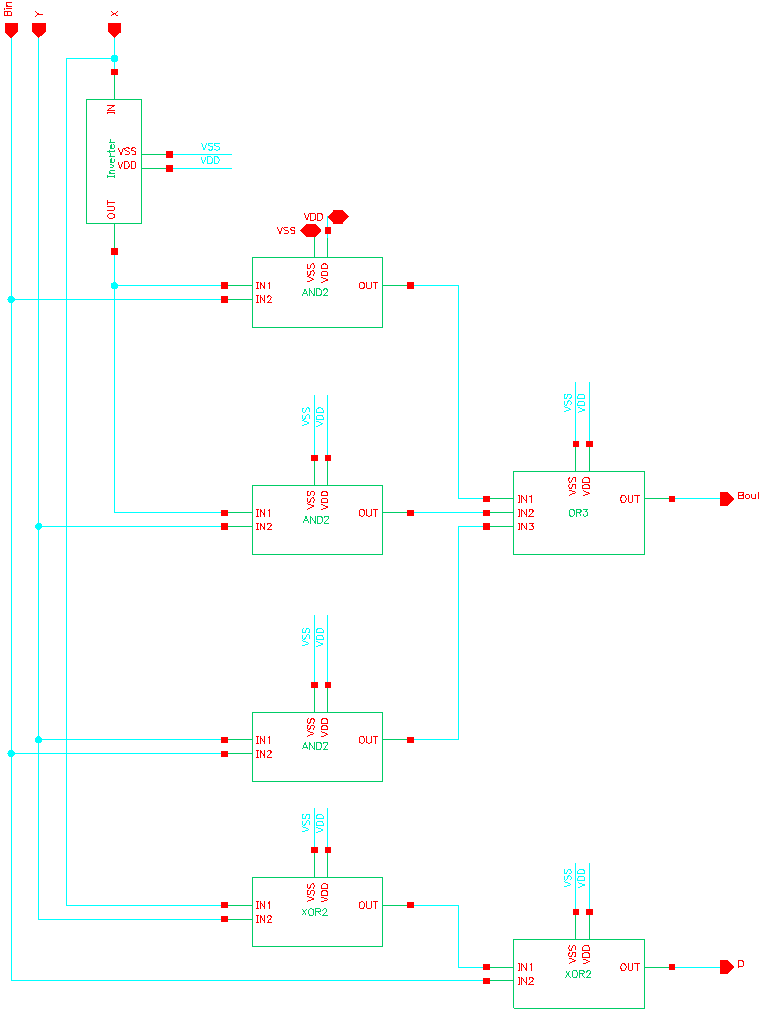


Figure : 1-bit Subtractor Implementation

A transient simulation was then performed to obtain the output waveform:

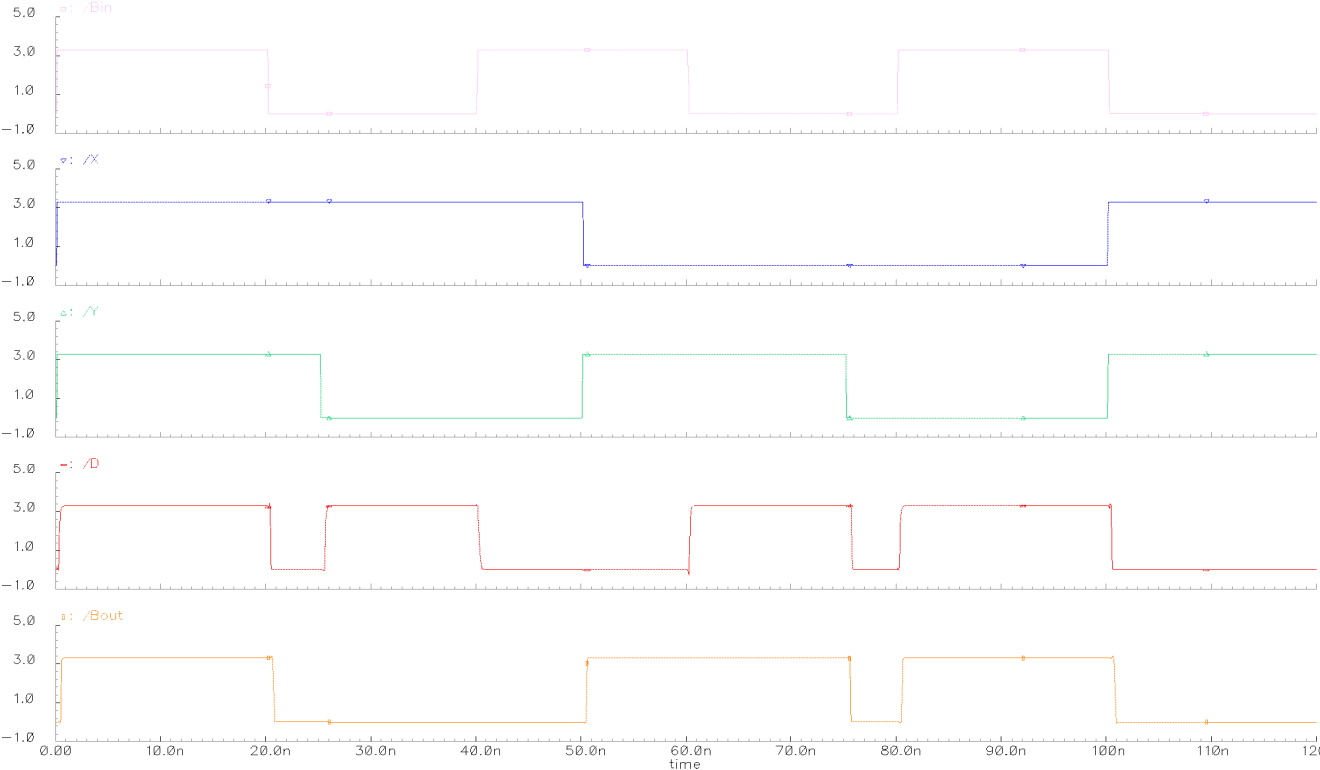


Figure : 1-bit Subtractor - Transient Response

Afterwards, the instance obtained for the 1-bit subtractor is shown in **Figure 23** below. Four units of this latter will be used to generate the 4-bit subtractor final design which will be discussed in the following page.

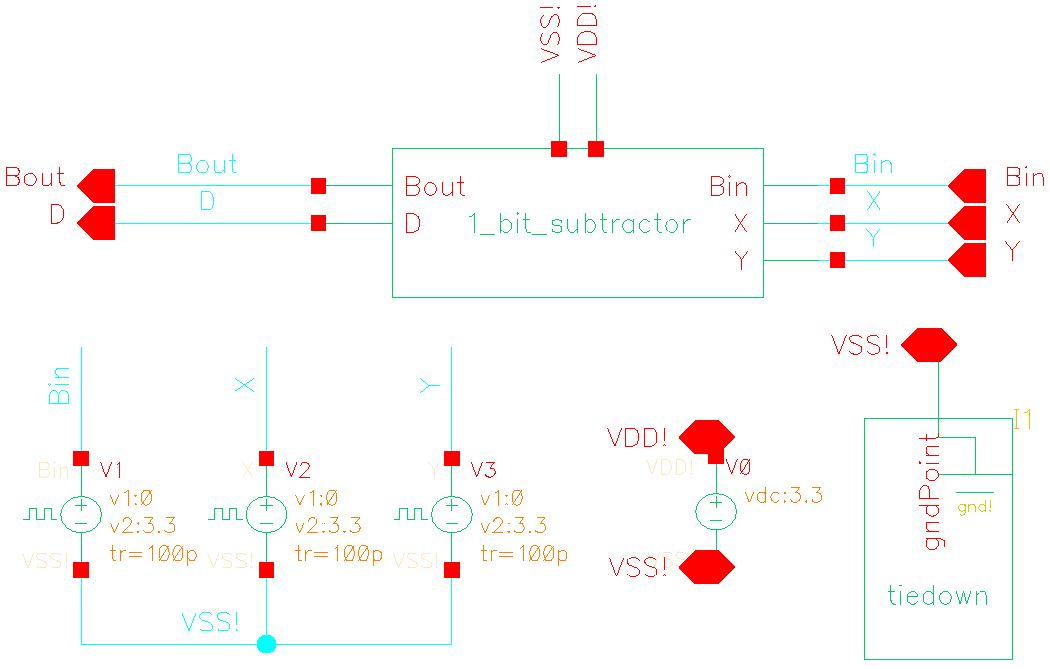


Figure : 1-bit Subtractor Instance

### 4-bit Subtractor

Finally, *four instances* of the 1-bit subtractor were placed in cascade in order to implement the 4-bit subtractor as shown in **Figure 24** below:

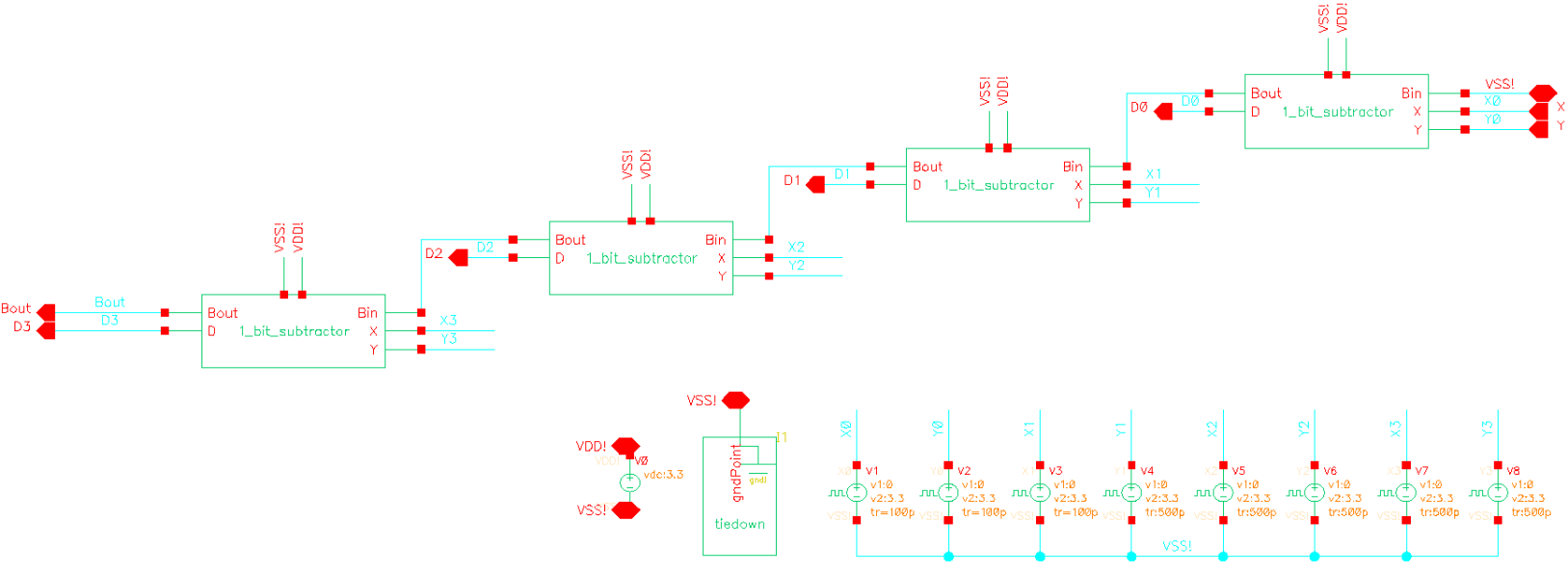
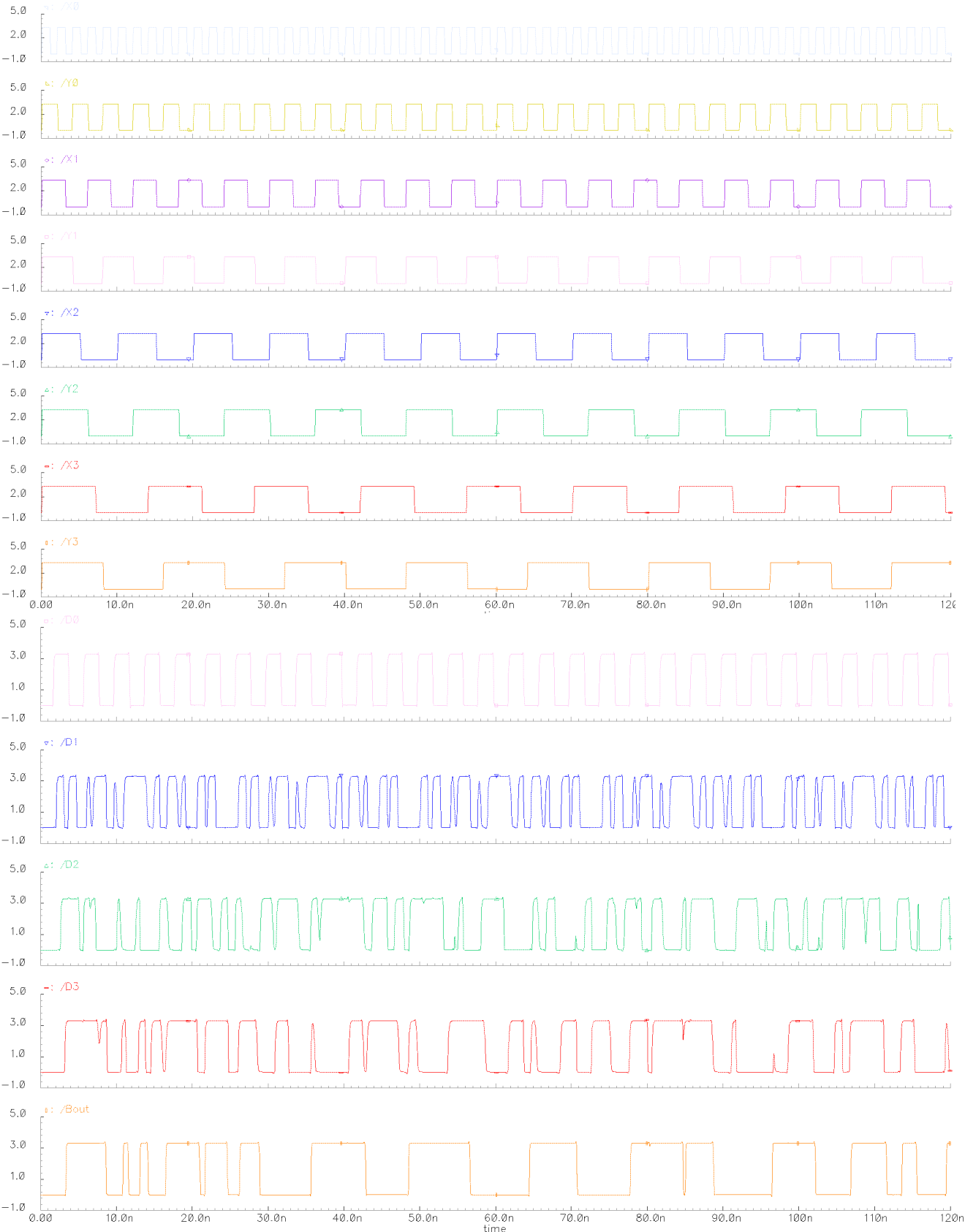


Figure : 4-bit Subtractor Circuit Schematic Diagram

Transient Analysis

In fact, after performing a transient simulation we obtained the following input and output waveforms as shown in **Figure 25** below:

Figure : 4-bit Subtractor - Transient Response



Graphically, the waveform above was used to determine the propagation delays ,  and the rise time or fall time  in order to record the results in **Table 8** below:

Table : 4-bit Subtractor - Propagation Delays and Switching Times Results

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Switching Times** | | **Propagation Delays** | | |
| **outputS** | **tr (ns)** | **tf (ns)** | **tPLH (ps)** | **tPHL (ps)** | **tP (ps)** |
| **Bout** | 24.15 | 3.25 | 146.34 | 520.34 | 333.34 |

DC Analysis

Using the Cadence Analog Design environment, a DC Analysis of a 4-bit subtractor was simulated. Additionally, the “Voltage Transfer Characteristic” or VTC was plotted and is shown in **Figure 26** below:

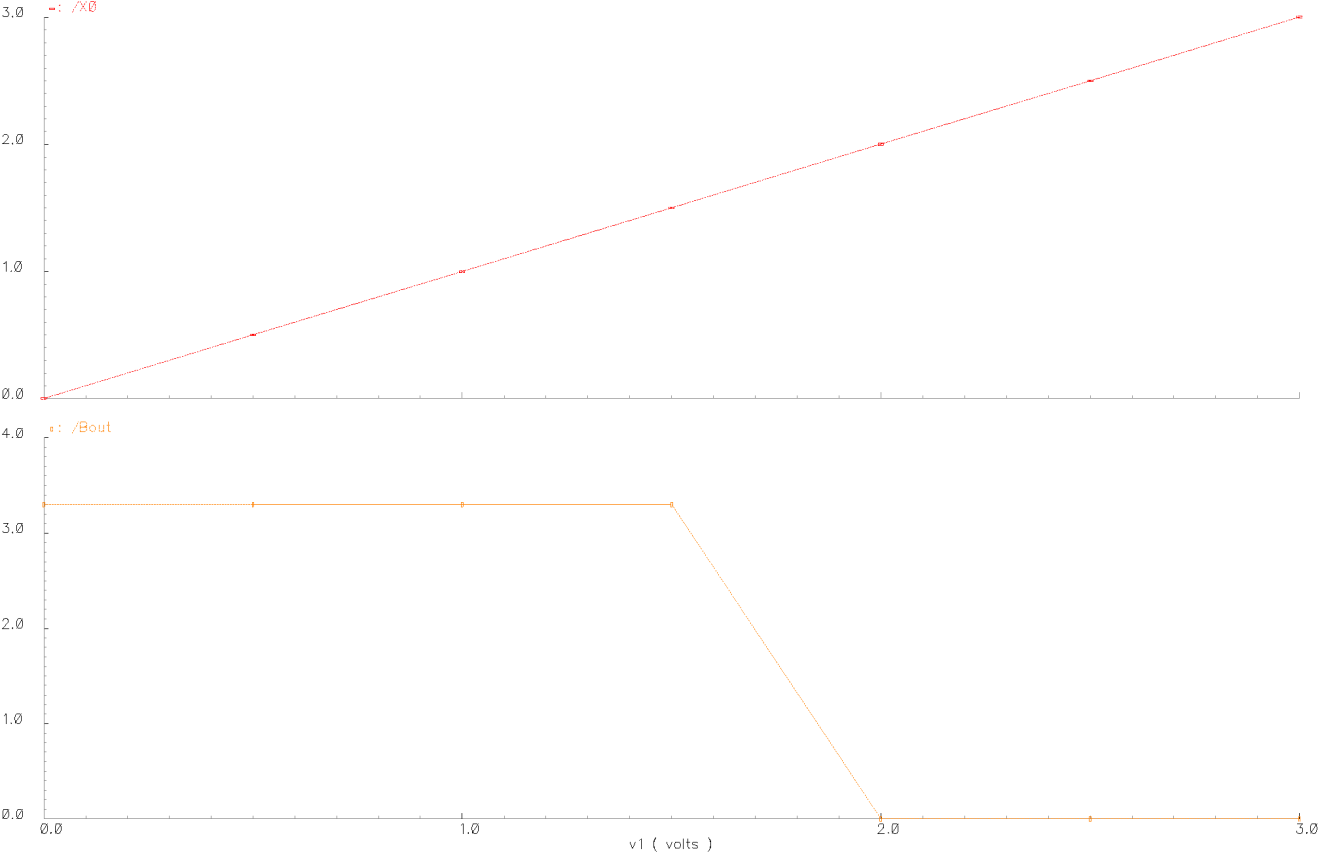


Figure : 4-bit Subtractor DC Sweep Response

Graphically from **Figure 26** above, one can easily derive several essential voltage parameters such as , , , , and  which are shown in **Table 9** below:

Table : 4-bit Subtractor - DC Voltage Transfer Characteristics and Parameters

|  |  |
| --- | --- |
| **Parameters** | **VX0 = 0 to 3.3V and all Other Inputs fixed to 3.3V** |
| **Bout** |
| **VOH** | 3.3V |
| **VOL** | 0V |
| **VIL** | 1.5V |
| **VIH** | 2.0V |
| **VM** | 1.75V |

Finally, we determined and recorded the noise margins in **Table 10** below:

Table : 4-bit Subtractor - Noise Margins Results

|  |  |
| --- | --- |
| **Noise Margins** | **VX0 = 0 to 3.3V and all Other Inputs fixed to 3.3V** |
| **4-bit Subtractor** |
| **NML = VIL - VOL** | 1.5V |
| **NMH = VOH - VIH** | 1.3V |

### Experimental Power Dissipation

Obtaining the total power dissipation at the source was fairly easy as the “HSPICE Netlist” can automatically perform the assessment of several performance parameters. For the 4-bit subtractor, the total voltage source power dissipation was found to be:



## Cadence Virtuoso Editor Simulation

To ensure that the implementation of the 4-bit subtractor circuit would be synthesizable, we also performed a layout simulation with the “Cadence Virtuoso Editor” by gradually designing and simulating the inverter, 2-input AND, 2-input XOR, 3-input OR logic gates separately as described below.

### Inverter

First the implementation of a XOR layout was readied using the editor as shown in **Figure 27** below:

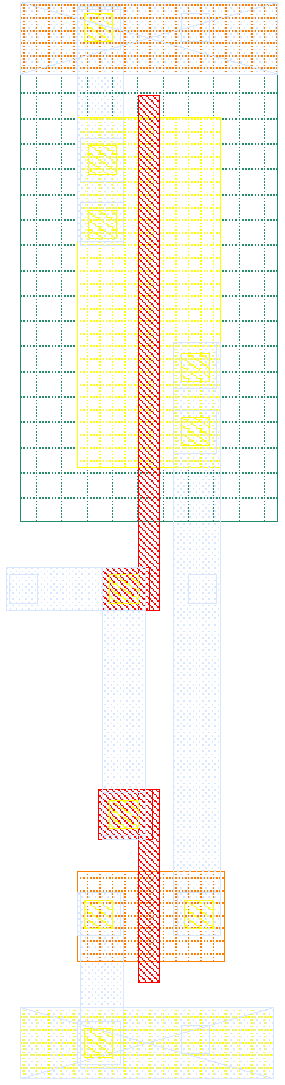


Figure : Inverter Layout

The inverter was subsequently simulated to ensure its correct functionality. This was done by generating the pins from the layout and than creating an instance out of it. After performing a transient simulation we obtained the output waveform in **Figure 28** below:

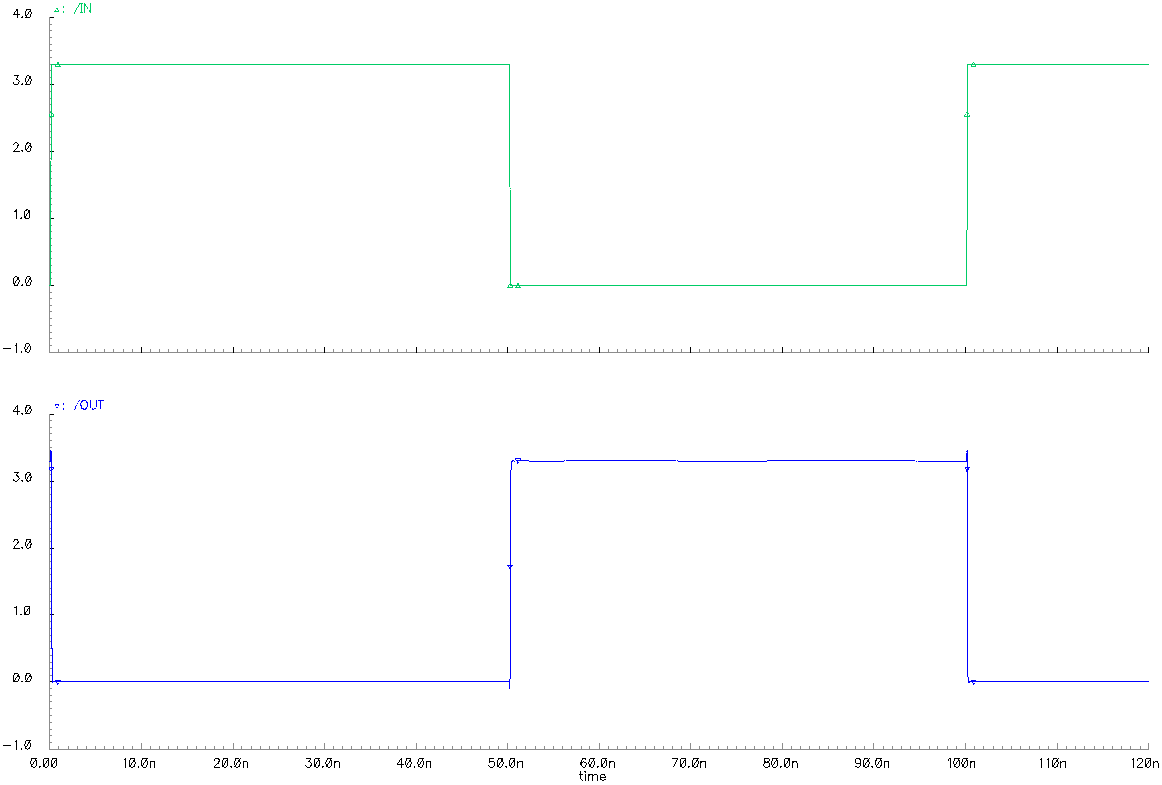


Figure 28: Inverter Layout- Transient Response

### 2-Input AND Gate

Afterwards, the implementation of the 2-input AND layout was performed by the means of the “Virtuoso Editor” as shown in **Figure 29** below:

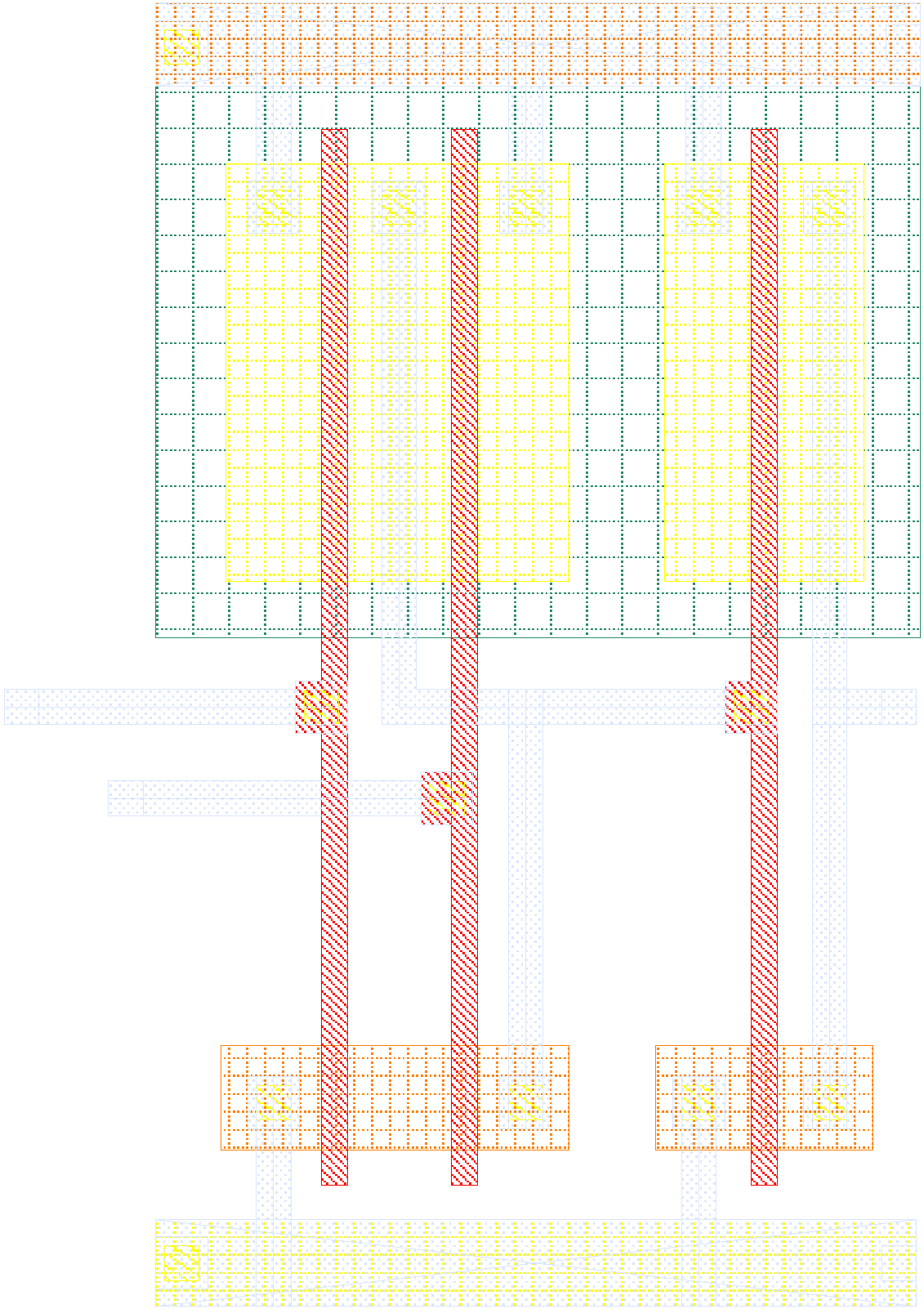


Figure : 2-Input AND Gate Layout

The 2-input AND layout was then simulated by generating the pins from the layout and than creating its instance. Moreover, by performing a transient simulation we obtained the output waveform in **Figure 30** below:

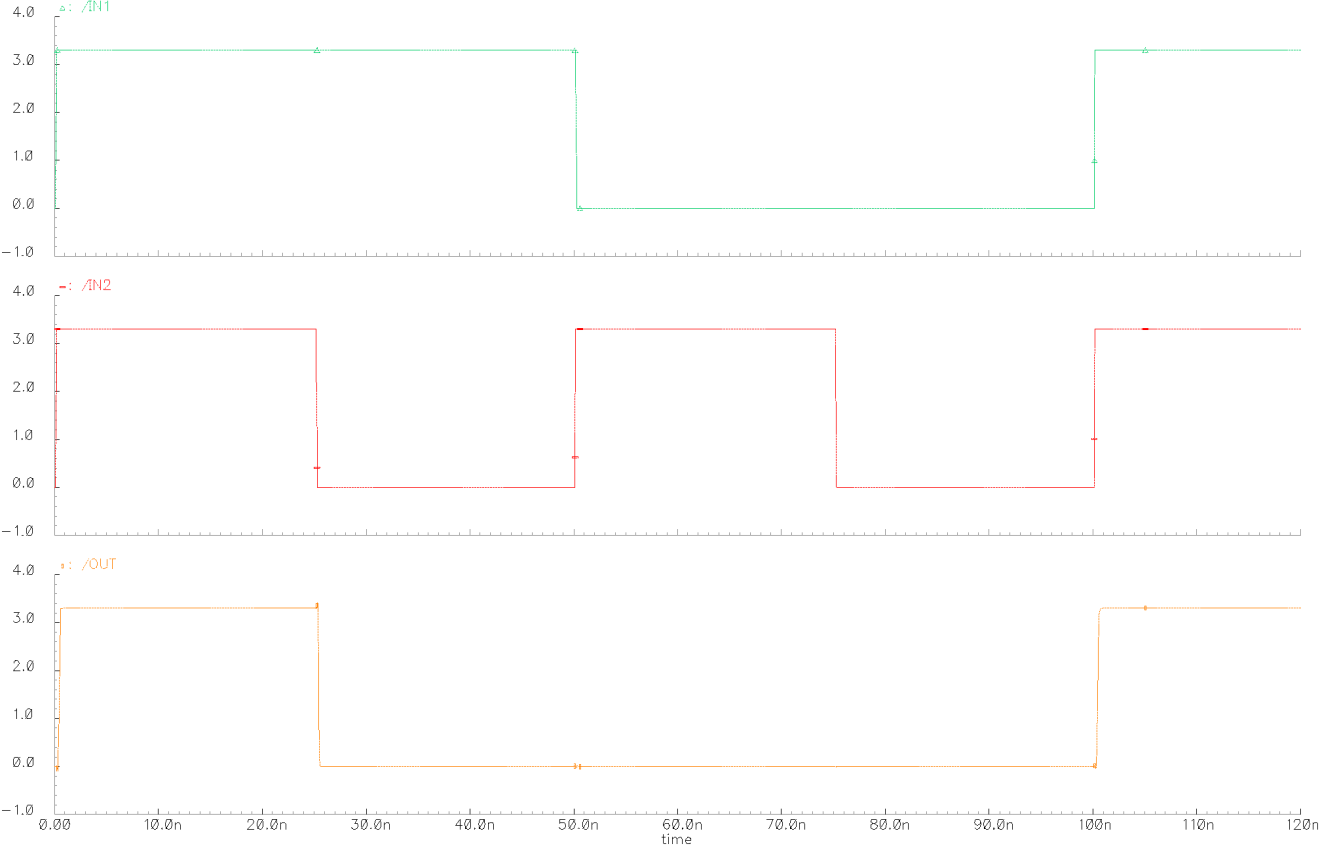


Figure : 2-Input AND Layout - Transient Response

### 2- Input XOR Layout

Subsequently, the design of the 2-input XOR layout was implemented as shown in **Figure 31** below:

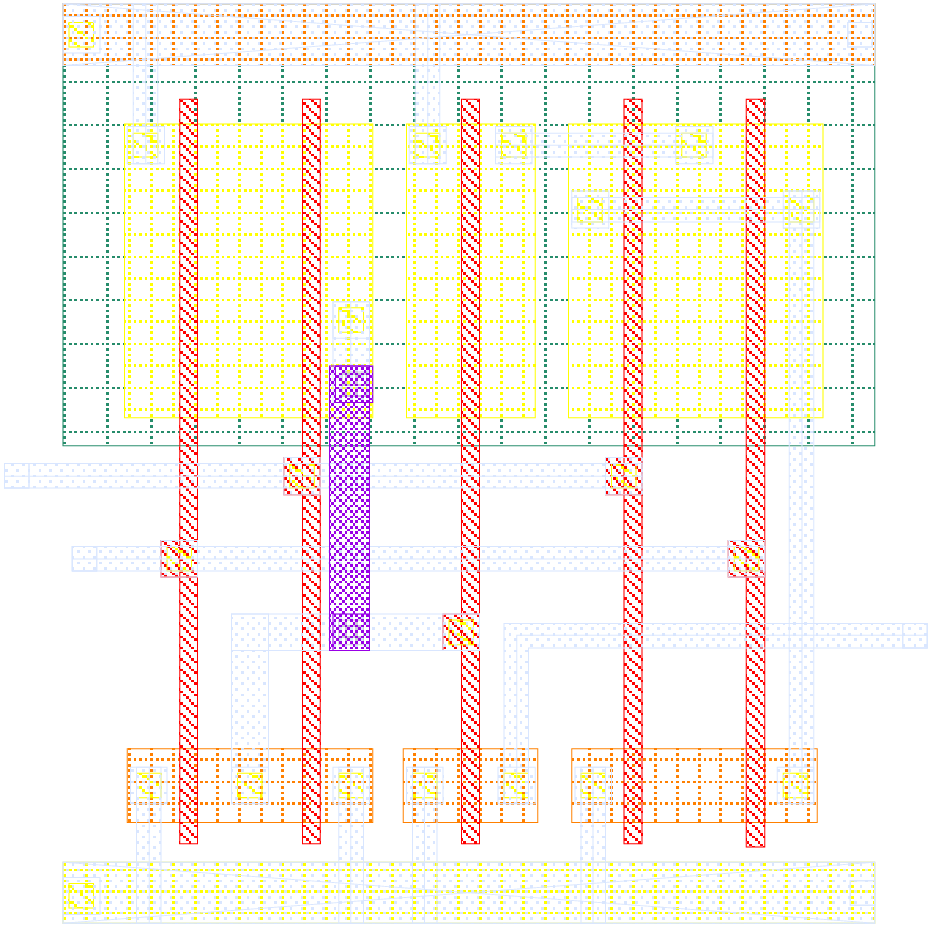


Figure : 2-Input XOR Gate Layout

A transient simulation was performed in order to obtain the output waveform as shown in **Figure 32** below:



Figure 32: 2-Input XOR Layout – Transient Response

### 3- Input OR Layout

Finally, the design of the 3-input OR layout circuit was done as shown in **Figure 33** below and its simulation result shown in **Figure 34**:

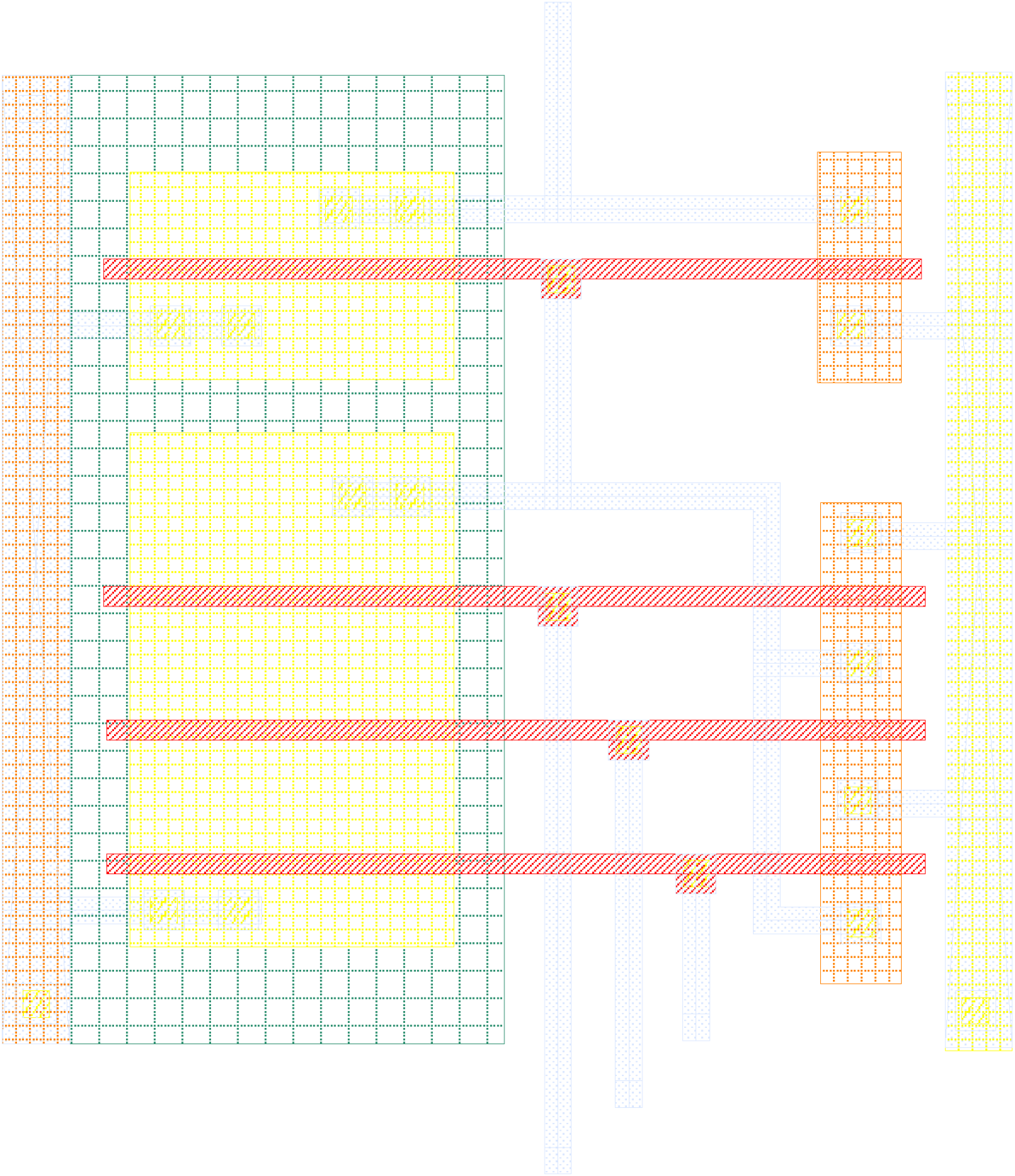


Figure : 3-Input OR Gate Layout



Figure 34: 3-input OR Layout - Transient Response

### 1-bit Subtractor

The 1-bit subtractor layout was then generated by implementing the circuit of **Figure 7**. The resulting layout is a circuit containing all the previous instances such as the inverter, 2-input AND, 2-input XOR, 3-input OR logic gates as shown below in **Figure 35**:

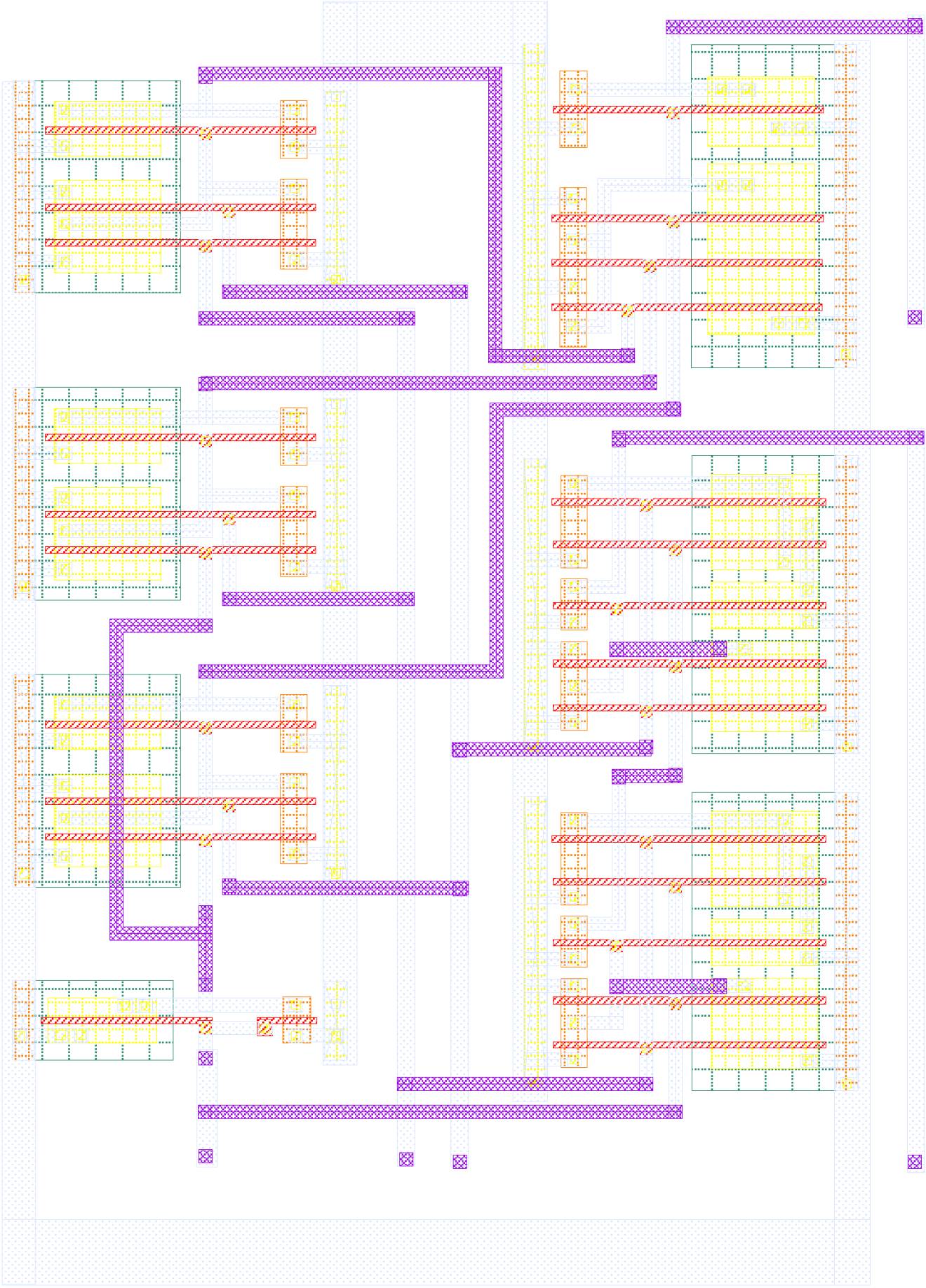


Figure : 1-bit Subtractor Layout Implementation

A transient simulation was then performed to obtain the output waveform:



Figure : 1-bit Subtractor - Transient Response

Afterwards, the instance obtained for the 1-bit subtractor is shown in **Figure 37** below:

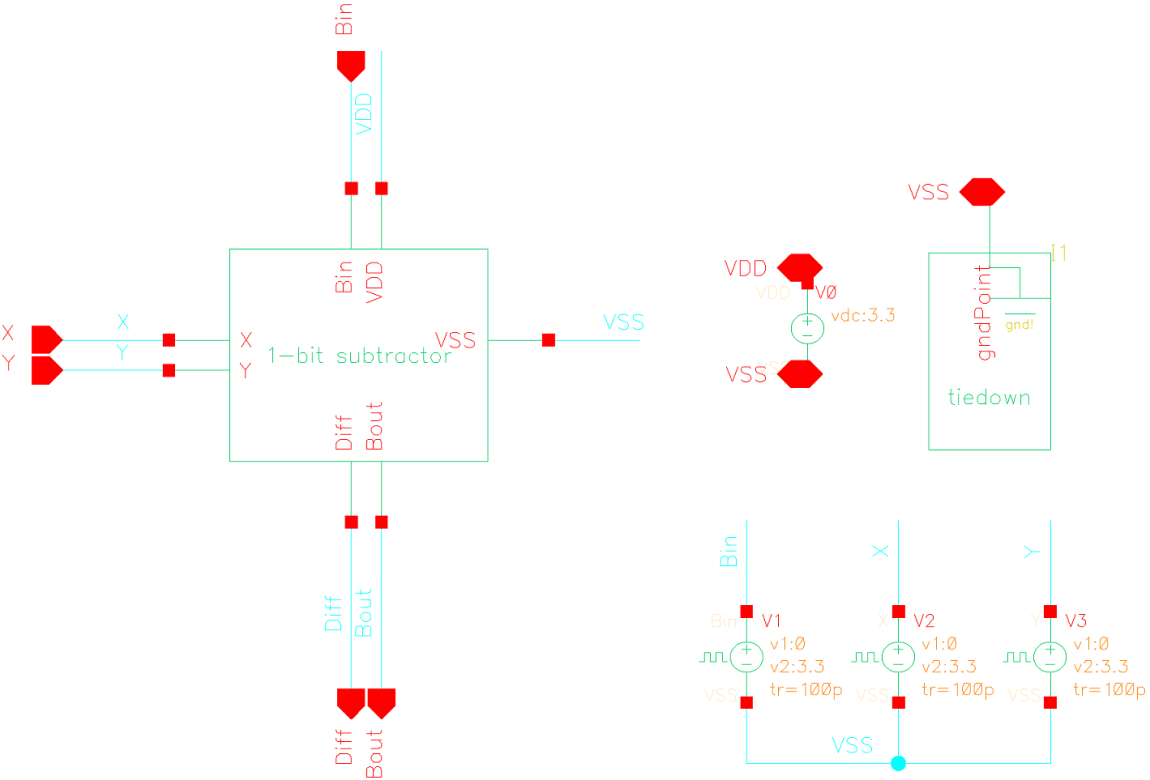
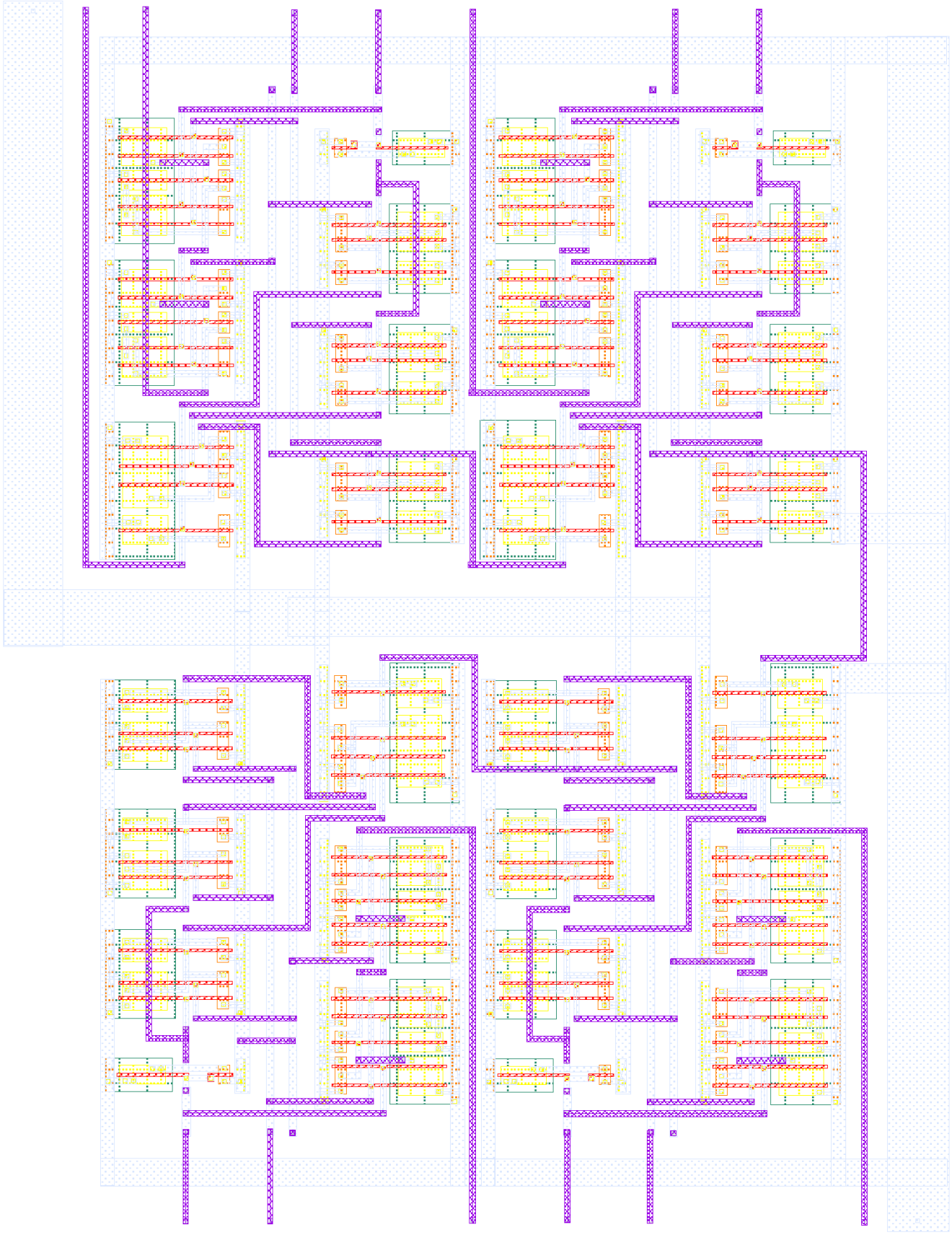


Figure : 1-bit Subtractor Instance

### 4-bit Subtractor Layout

Finally, *four instances* of the 1-bit subtractor were placed in cascade in order to generate the final 4-bit subtractor layout as shown in **Figure 38** below:

Figure : 4-bit Subtractor Circuit Layout



Transient Analysis

The transient response of the 4-bit subtractor has been studied by means of the “HSPICE” analog circuit simulator. In fact, after performing a transient simulation we obtained the following input and output waveforms as shown in **Figure 39** below:

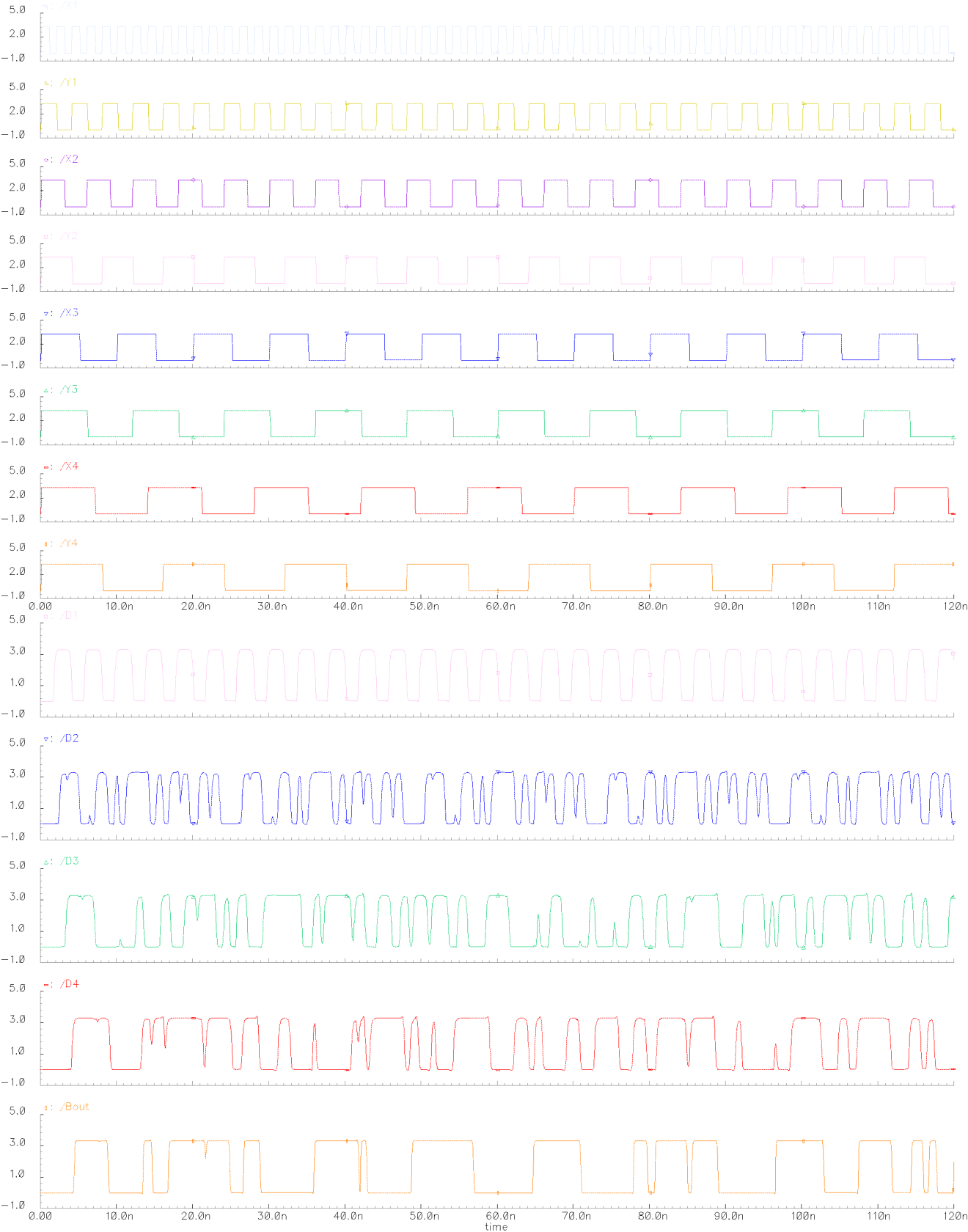


Figure : 4-bit Subtractor - Transient Response

Graphically, the waveform above was used to determine the propagation delays ,  and the rise time or fall time  in order to record the results in **Table 5** below:

Table : 4-bit Subtractor - Propagation Delays and Switching Times Results

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **Switching Times** | | **Propagation Delays** | | |
| **outputS** | **tr (ns)** | **tf (ns)** | **tPLH (ps)** | **tPHL (ps)** | **tP (ps)** |
| **Bout** | 24.15 | 4.25 | 233.19 | 775.14 | 504.16 |

DC Analysis

Using the Cadence Analog Design environment, a DC Analysis of a 4-bit subtractor was simulated. Additionally, the “Voltage Transfer Characteristic” or VTC was plotted and is shown in **Figure 40** below:

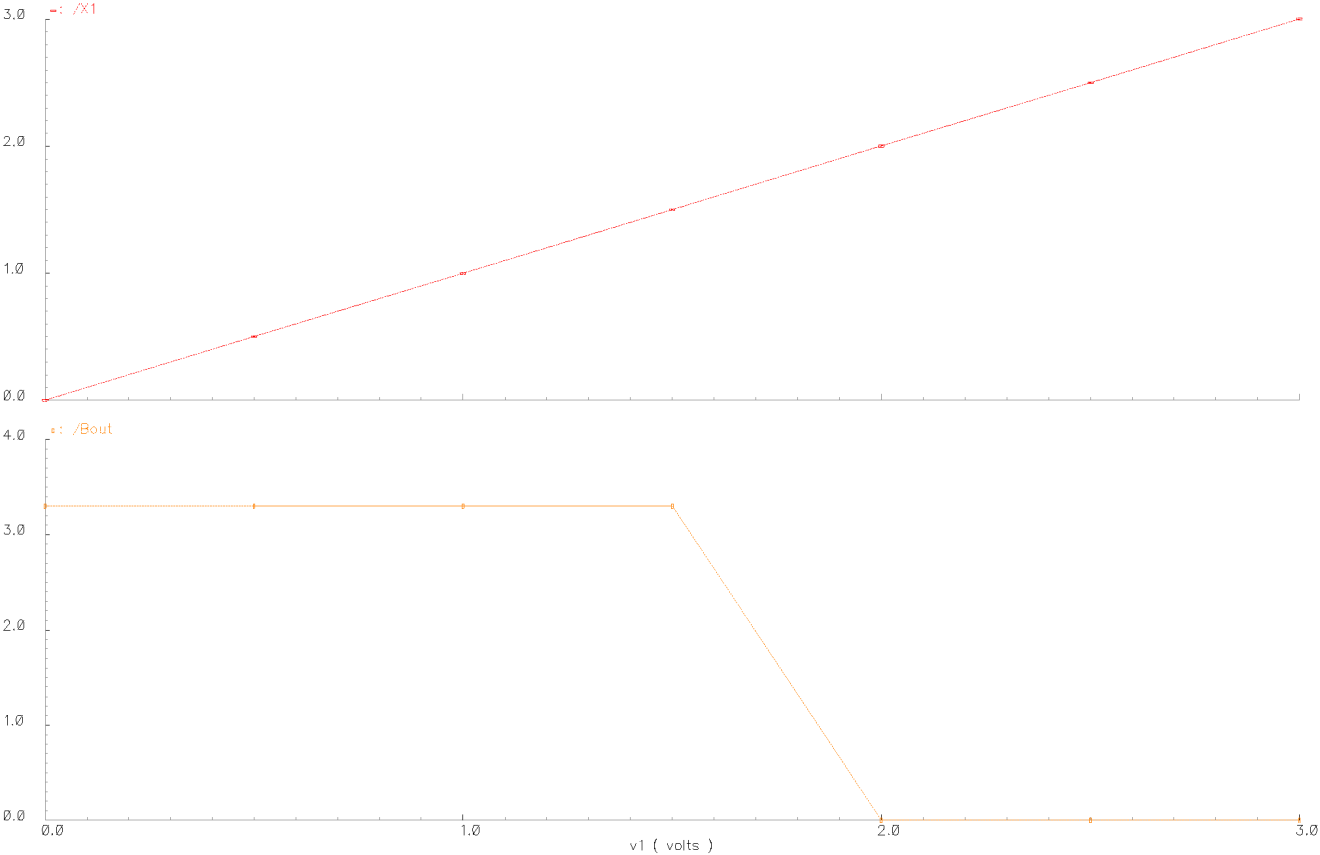


Figure : 4-bit Subtractor DC Sweep Response

Graphically from **Figure 40** above, one can easily derive several essential voltage parameters such as , , , , and  which are shown in **Table 12** below:

Table : 4-bit Subtractor - DC Voltage Transfer Characteristics and Parameters

|  |  |
| --- | --- |
| **Parameters** | **VX1 = 0 to 3.3V and all Other Inputs fixed to 3.3V** |
| **Bout** |
| **VOH** | 3.3V |
| **VOL** | 0V |
| **VIL** | 1.5V |
| **VIH** | 2.0V |
| **VM** | 1.75V |

Finally, we determined and recorded the noise margins in **Table 13** below:

Table : 4-bit Subtractor - Noise Margins Results

|  |  |
| --- | --- |
| **Noise Margins** | **VX0 = 0 to 3.3V and all Other Inputs fixed to 3.3V** |
| **4-bit Subtractor** |
| **NML = VIL - VOL** | 1.5V |
| **NMH = VOH - VIH** | 1.3V |

### Experimental Power Dissipation

Obtaining the total power dissipation at the source was fairly easy as the “HSPICE Netlist” can automatically perform the assessment of several performance parameters. For the 4-bit subtractor, the total voltage source power dissipation was found to be:



### Padframe and Routing

“Once the circuit’s implementation reaches completion at the layout level and its simulation tested, the final step in a full-custom design is to construct a padframe and establish the interconnections between the input/output and power supply pads of the padframe and the inputs/outputs and supply connections of the circuit layout [2]”. Therefore, to make the 4-bit subtractor factory ready we implemented the padframe and attached it to **APPENDIX B** at the end of the report.

1. DISCUSSION

The diagram of a 4-bit subtractor circuit was implemented and simulated by means of two different methods. The first method involved using the “Cadence Schematic Editor and Analog Environment” software used to create a schematic diagram and a simulation of our implementation. The second method entailed the use of the “Cadence Virtuoso Editor” to implement the layout of the subtractor. To summarize the excessive experimental results obtained, we will record the transient analysis results in **Table 14**, the DC sweep analysis in **Table 15,** the Noise Margins in **Table 16** and the area with the power in **Table 17** below:

Table : Transient Analysis Comparison

|  |  |  |
| --- | --- | --- |
|  | **4-bit Subtractor Transient** |  |
| **Timing Parameters** | **Schematic** | **Layout** |
| **tr (ns)** | 24.15 | 24.15 |
| **tf (ns)** | 3.25 | 4.25 |
| **tPLH (ps)** | 146.34 | 233.19 |
| **tPHL (ps)** | 520.34 | 775.14 |
| **tP (ps)** | 333.34 | 504.16 |

Table : DC Sweep Analysis Comparison

|  |  |  |
| --- | --- | --- |
|  | **4-bit Subtractor DC** | |
|  | **VX0 = 0 to 3.3V and all Other Inputs fixed to 3.3V** | |
| **Parameters** | **Schematic** | **Layout** |
| **VOH** | 3.3V | 3.3V |
| **VOL** | 0V | 0V |
| **VIL** | 1.5V | 1.5V |
| **VIH** | 2.0V | 2.0V |
| **VM** | 1.75V | 1.75V |

Table : Noise Margins Comparison

|  |  |  |
| --- | --- | --- |
| **Noise Margins** | **VX0 = 0 to 3.3V and all Other Inputs fixed to 3.3V** | |
| **Schematic** | **Layout** |
| **NML = VIL - VOL** | 1.5V | 1.5V |
| **NMH = VOH - VIH** | 1.3V | 1.3V |

Table : Area and Power Performance

|  |  |  |  |
| --- | --- | --- | --- |
|  | **4-bit Subtractor Performance** | | |
| **Schematic** | **Layout with Pads** | **Layout without Pads** |
| **Area** | - | 2.8258mm2 | 53130µm2 |
| **Power Dissipation** | 5.2nW | 4.8nW | 4.8nW |

First and foremost, the transient analysis of both simulations was performed and shown in **Figure 25** **and 39**. From the latter figures, we can clearly see that the graph’s inputs and outputs are completely similar to each other as expected. Similarly, we can notice that the theoretical 1-bit subtractor truth table results depicted in **Table 1** match perfectly both simulation results obtained graphically in **Figure 22 and 36**. Plus, from **Table 4** we notice that the rise time  or fall time for both implementations are identical as anticipated due to the fact that their transistors were similarly sized and the circuits have the same functionality. Nevertheless, the propagation delay  and  are slightly higher for the subtractor simulated via the layout than the one done schematically because the layout has bigger area and more capacitances. From the analysis of the DC Sweep Response shown in **Table 15**, one can notice that ,, ,  and  are all identical for the schematic and layout simulations. The power dissipation was found to be slightly lower for the subtractor implemented through the layout; however, for a difference of 0.4nW we will consider it negligible. Therefore, we can clearly see from the above that the implementation of the 4-bit subtractor was successful.

1. CONCLUSION

Overall, in this experiment different skills and techniques were gained and applied in a fundamental part. Indeed, we were able to design, implement and successfully analyze the characteristics of a 4-bit subtractor circuit. The completion of this main task was entirely satisfactory since the theoretical expectations matched our experimental results. Moreover, the use of the transient response and DC Sweep analysis for the circuit helped us in correctly comparing and validating our results while reaching a rational conclusion. In fact, we were able to evaluate the quality of the output signals in terms of several voltage parameters such as ,,, and . We also evaluated the quality of the output signals by comparing the timing measurements of each circuit by means of the propagation delays,  and the rise time or fall time . The performance of the 4-bit subtractor was assessed in terms of area, speed while putting the emphasis on the optimization of the circuit in terms of power consumption. Finally, we now master the CMOSIS5 package alongside the “Cadence Schematic Editor and Analog Environment” software as we are now able to create schematic diagram, simulate our implementations, and sketch the layout of the components independently to finally create the padding of the implementation.

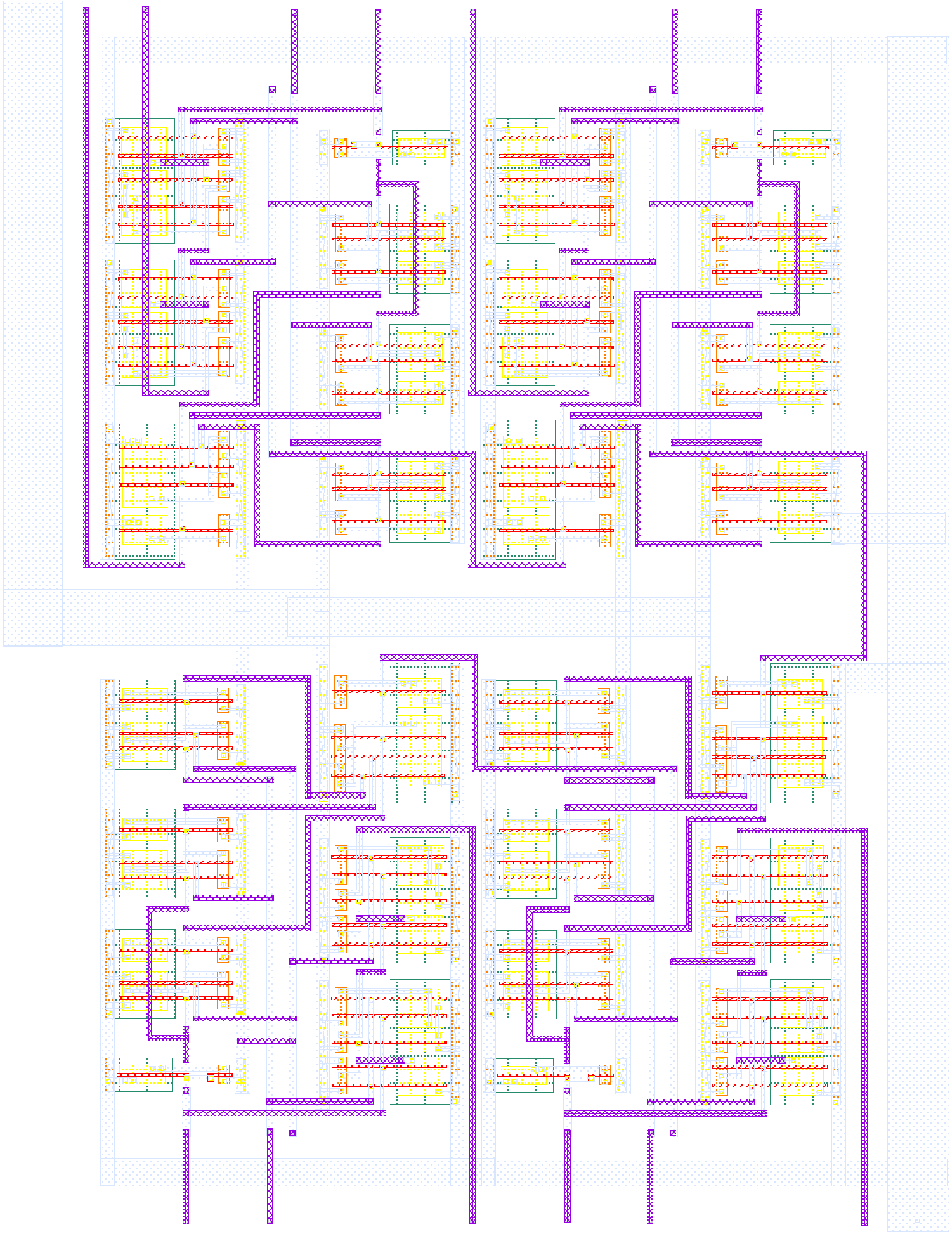
# REFERENCES

1. Microelectronic Circuits by Adel S. Sedra and K. C. Smith. Oxford University Press; Fourth Edition.
2. Ted Obuchowicsz. *A Tutorial on Using the Cadence Schematic Editor and Analog Environment to Create and Simulate a CMOS Onverter at the Transistor Level using CMOSIS5 Technology*. < http://users.encs.concordia.ca/~ted/>.

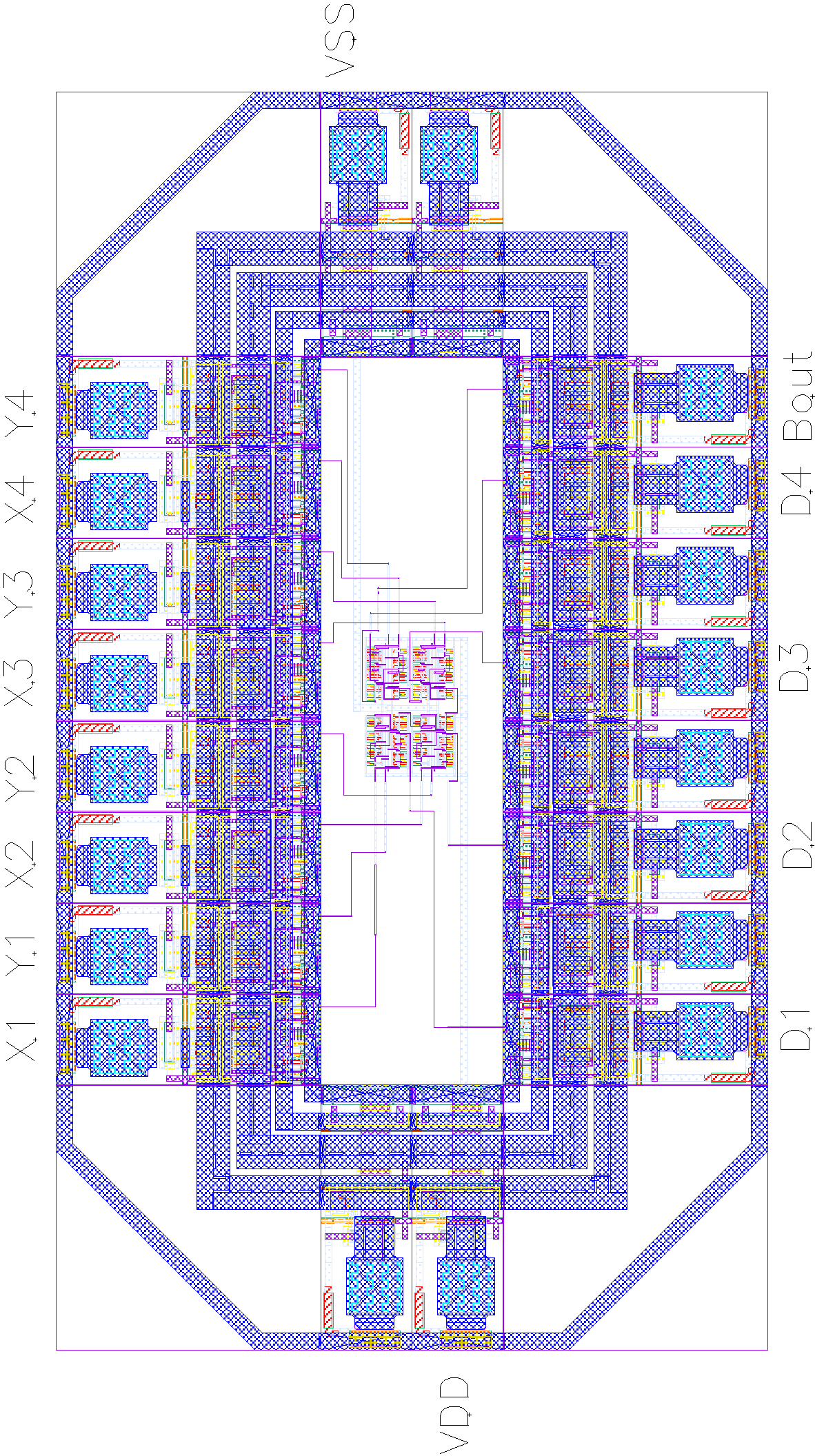
# 

# APPENDICES

## APPENDIX A: 4-BIT SUBTRACTOR LAYOUT



## APPENDIX B: 4-BIT SUBTRACTOR PADDING



## APPENDIX C: EXPECTATION OF ORIGINALITY FORM