

CONCORDIA UNIVERSITY  
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

**ELEC 691GG Electronics for Silicon-Photonic Design**  
**Course Outline**

**INSTRUCTOR/ORGANIZER:**

Glenn Cowan, Associate Professor, Electrical and Computer Engineering  
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Office Hours: TBD

**LECTURES:**

Mon-Fri August 31<sup>st</sup> to September 4<sup>th</sup>, 8:45 AM to 5:30 PM.

**USEFUL TEXTBOOKS WORTH CONSULTING:**

- R. J. Baker, "CMOS Circuit Design, Layout, and Simulation," 3<sup>rd</sup> edition, Wiley, 2010.
- B. Razavi, "Design of Integrated Circuits for Optical Communications," McGraw-Hill, 2002.

**WORK SHOP FORMAT:**

This course will run full days over a 5-day week. Hands-on activities will be interspersed throughout the time. Instruction and presentation will be given by a variety of faculty members and industrial designers.

**CALENDAR DESCRIPTION: ELEC 691GG *Electronics for Silicon-Photonic Design* (4 credits)**

Prerequisite: Permission of the department. CMOS high-frequency analog design fundamentals, including use of computer-aided design tools. Compact models for optical devices. Link budget analysis. Receiver circuits. Transmitter circuits. Tuning circuits. Packaging considerations. A project.

**PERMISSION OF THE DEPARTMENT:**

Permission will be granted to students who have the required background and interest in the material. The course is aimed at thesis-based MASc and PhD students for whom this material will form a component of their research. Evidence of required background material would be a course equivalent to Concordia's ELEC 312 Electronics II, ELEC 423/6051: Introduction to Analog VLSI, or ELEC 498N/691N: Mixed-signal VLSI for communication systems.

**OVERALL COURSE OBJECTIVES:**

This course prepares students for designing the electronic portion of silicon electronic photonic integrated circuits.

**TENTATIVE LECTURE SCHEDULE:**

Topics	Lecture hours	Topics
1	7	CMOS analog design fundamentals
2	3.5	Compact models for optical devices
3	3	Optical link budget analysis
4	10	Receivers
5	8	Transmitters
6	1.5	Tuning circuits
7	1.5	Packaging considerations
Total	34.5	

**PROJECT:**

A design project will be given at the beginning of the semester. The project will involve system and transistor level simulation as well as the integrated-circuit layout of part of a communication link.

**GRADING SCHEME:**

Project = 100 %

The project grade will be based on several intermediate milestones with feedback given after each one. The due date for the milestones will be spread out over the term.

<b>Component</b>	<b>Weighting</b>
3-min presentation of a proposed design topic	5
3-page proposal of design project, with preliminary literature review	10
Architecture review including proposed circuit topologies and per-block specifications	15
Final schematic review	15
Layout review	15
Final report and completed layout, December 15 <sup>th</sup>	40

The project must be accompanied by a signed copy of ENCS's Expectations of Originality form. See: <http://www.encs.concordia.ca/current-students/forms-and-procedures/expectation-of-originality/>