CHAPTER 5

5.1 (a)  
\[ R = D'C \]
\[ S = DC \]

(b)  
\[ R = (D + C)' = D'C \]
\[ S = (D' + C')' = D'C \]

(c)  
\[ R = (DC)' = D' + C' \]
\[ S = ((DC)' C)' = D'C + C' \]
\[ = (D + C) = (D'C)' \]

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Present state | Input | Next state | Output
---|---|---|---
0 | 0 | 0 | 0
0 | 0 | 1 | 0
0 | 1 | 0 | 0
0 | 1 | 1 | 0
1 | 0 | 0 | 0
1 | 0 | 1 | 0
1 | 1 | 0 | 0
1 | 1 | 1 | 0
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 0
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1

(b) $A(t+1) = xy' + xB$
(c) $B(t+1) = xA + xB'$

Present state | Input | Next state | Output
---|---|---|---
0 | 0 | 0 | 0
0 | 0 | 1 | 0
0 | 1 | 0 | 0
0 | 1 | 1 | 0
1 | 0 | 0 | 0
1 | 0 | 1 | 0
1 | 1 | 0 | 0
1 | 1 | 1 | 0
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1

5.7

Present state | Input | Next state | Output
---|---|---|---
0 | 0 | 0 | 0
0 | 0 | 1 | 0
0 | 1 | 0 | 0
0 | 1 | 1 | 0
1 | 0 | 0 | 0
1 | 0 | 1 | 0
1 | 1 | 0 | 0
1 | 1 | 1 | 0
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1
1 | 0 | 0 | 1
1 | 0 | 1 | 1
1 | 1 | 0 | 1
1 | 1 | 1 | 1

$S = x \oplus y \oplus Q$
$Q(t+1) = xy + xQ + yQ$
5.8 A counter with a repeated sequence of 00, 01, 10.

<table>
<thead>
<tr>
<th>Present</th>
<th>Next</th>
<th>FF inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A B A B</td>
<td></td>
<td>T_a T_b</td>
</tr>
<tr>
<td>0 0 0 0</td>
<td></td>
<td>0 1</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td></td>
<td>1 1</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td></td>
<td>1 0</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td></td>
<td>1 1</td>
</tr>
</tbody>
</table>

\[ T_a = A + B \]
\[ T_b = A' + B \]

Repeated sequence:

\[ 00 \rightarrow 01 \rightarrow 10 \]

5.9

\[ J_a = x \quad K_a = B \]
\[ J_b = x \quad K_b = A' \]

\[ A(t+1) = J_a A' + K_a A = xA' + B'A \]
\[ B(t+1) = J_b B' + K_b B = xB' + AB \]

\[ x \quad A \quad B \quad xA' + B'A \quad xB' + AB \]
\[ 0 \quad 0 \quad 0 \quad 0 \quad 0 \]
\[ 0 \quad 0 \quad 1 \quad 0 \quad 0 \]
\[ 0 \quad 1 \quad 1 \quad 1 \quad 0 \]
\[ 0 \quad 1 \quad 1 \quad 0 \quad 1 \]
\[ 1 \quad 0 \quad 1 \quad 1 \quad 1 \]
\[ 1 \quad 0 \quad 1 \quad 0 \quad 1 \]
\[ 1 \quad 1 \quad 0 \quad 1 \quad 1 \]

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5.10

(a) \( J_A = Bx + B'y' \)
\( J_B = A'y' \)

(b) \( K_A = B'x'y' \)
\( K_B = A + xy' \)

(c) \( z = Axy + Bx'y' \)

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5.11  
(a)  
<table>
<thead>
<tr>
<th>Present</th>
<th>00 00 0 1 11 00 01 11 10 00 01 11 10 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>state:</td>
<td>0 1 1 0 1 1 0 1 1 0 1 1 1 0</td>
</tr>
<tr>
<td>Input:</td>
<td>0 1 0 1 0 1 1 0 1 1 1 1 0</td>
</tr>
<tr>
<td>Output:</td>
<td>0 0 1 0 0 1 0 0 1 0 0 0 0 1</td>
</tr>
<tr>
<td>Next</td>
<td>00 01 00 01 11 00 01 11 10 00 01 11 10 10 00</td>
</tr>
<tr>
<td>state:</td>
<td>0 1 1 0 1 1 0 1 1 0 1 1 1 0</td>
</tr>
</tbody>
</table>

(b)  
State labels:  
a: 00, b: 10, c: 11, d: 01  
c is equivalent to b  
d is equivalent to c

(c)  
<table>
<thead>
<tr>
<th>input</th>
<th>state</th>
<th>next st</th>
<th>output</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

State machine: D-flop with direct input of the input to the original machine;  
output logic: \( y = (\text{input}) \& \& (\text{state} == \text{b}) \)

5.12  
<table>
<thead>
<tr>
<th>Present</th>
<th>Next state</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 1</td>
<td>0 1</td>
</tr>
<tr>
<td>a</td>
<td>f b</td>
<td>0 0</td>
</tr>
<tr>
<td>b</td>
<td>d a</td>
<td>0 0</td>
</tr>
<tr>
<td>d</td>
<td>g a</td>
<td>1 0</td>
</tr>
<tr>
<td>f</td>
<td>f b</td>
<td>1 1</td>
</tr>
<tr>
<td>g</td>
<td>g d</td>
<td>0 1</td>
</tr>
</tbody>
</table>
5.13 (a) State: \( a f b c e d g h g h a \)
Input: 0 1 1 1 0 0 1 0 0 1 1
Output: 0 1 0 0 0 1 1 1 0 1 0

(b) State: \( a f b a b d g g d a \)
Input: 0 1 1 1 0 0 1 0 0 1 1
Output: 0 1 0 0 0 1 1 0 1 0

5.14

<table>
<thead>
<tr>
<th>Present state</th>
<th>Next state</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABCDE</td>
<td>x=0 x=1 x=0</td>
<td></td>
</tr>
<tr>
<td>a 00001</td>
<td>0001 0010 0 0</td>
<td></td>
</tr>
<tr>
<td>b 00010</td>
<td>00100 01000 0 0</td>
<td></td>
</tr>
<tr>
<td>c 00100</td>
<td>00001 01000 0 0</td>
<td></td>
</tr>
<tr>
<td>d 01000</td>
<td>10000 01000 0 1</td>
<td></td>
</tr>
<tr>
<td>e 10000</td>
<td>00001 01000 0 1</td>
<td></td>
</tr>
</tbody>
</table>

5.15 \( D_Q = Q'J + QK' \)

5.16 (a) \( D_A = Ax' + Bx \)
\( D_B = A'x + Bx' \)
The output is 0 for all 0 inputs until the first 1 occurs, at which time the output is 1. Thereafter, the output is the complement of the input. The state diagram has two states. In state 0: output = input; in state 1: output = input'.

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6.6 First stage of register:

![Diagram of shift load serial input](image)

6.7 First stage of register:

![Diagram of 4x1 Mux](image)

6.8 \( A = 0010, 0001, 1000, 1100 \). Carry = 1, 1, 1, 0

6.9 (a) In Fig. 6.5, complement the serial output of shift register B (with an inverter), and set the initial value of the carry to 1.

(b) Present state inputs Next state output FF inputs

<table>
<thead>
<tr>
<th>Present state</th>
<th>Inputs</th>
<th>Next state</th>
<th>Output</th>
<th>FF inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q x y</td>
<td></td>
<td>Q D J K Q</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0 0</td>
<td>0</td>
<td>0 0 1 0 0</td>
<td>0 1 0 0</td>
<td>x</td>
</tr>
<tr>
<td>0 0 0 1 1</td>
<td>1</td>
<td>1 1 1 1 1</td>
<td>1 1 1 1</td>
<td>x</td>
</tr>
<tr>
<td>0 1 0 0 1</td>
<td>0</td>
<td>0 0 1 0 0</td>
<td>0 0 1 0</td>
<td>x</td>
</tr>
<tr>
<td>0 0 1 0 0</td>
<td>0</td>
<td>0 0 1 0 0</td>
<td>0 0 1 0</td>
<td>x</td>
</tr>
<tr>
<td>1 1 0 1 1</td>
<td>1</td>
<td>1 1 0 1 1</td>
<td>1 1 0 1</td>
<td>x</td>
</tr>
<tr>
<td>1 1 0 1 0</td>
<td>0</td>
<td>0 0 1 0 0</td>
<td>0 0 1 0</td>
<td>x</td>
</tr>
<tr>
<td>1 1 1 0 0</td>
<td>1</td>
<td>1 1 1 0 0</td>
<td>1 1 1 0</td>
<td>x</td>
</tr>
<tr>
<td>1 1 1 1 1</td>
<td>1</td>
<td>1 1 1 1 1</td>
<td>1 1 1 1</td>
<td>x</td>
</tr>
</tbody>
</table>

\[ J_0 = xy' \]

\[ K_0 = xy^* * \]

\[ D = Q * xy \]
6.16  Q8 Q4 Q2 Q1 :  
Next state:  1010  1100  1110  Self correcting
Next state:  1011  1101  1111
1010 → 1011 → 0100
1100 → 1101 → 0100
1110 → 1111 → 0000

6.17  With \( E \) denoting the count enable in Fig. 6.12 and D-flip-flops replacing the J-K flip-flops, the toggling action of the bits of the counter is determined by: \( T_0 = E, T_1 = A_0E, T_2 = A_0A_2E, T_3 = A_0A_2A_3E. \) Since \( D_0 = A \oplus T_0 \) the inputs of the flip-flops of the counter are determined by: \( D_{Q0} = A_0 \oplus E; D_{Q1} = A_0 \oplus (A_2E); D_{Q2} = A_0 \oplus (A_2A_3E); D_{Q3} = A_0 \oplus (A_2A_3A_4E). \)

6.18  When \( up = down = 1 \) the circuit counts up.

\[
\begin{array}{cccc|c}
\text{up} & \text{down} & x & y & \text{Operation} \\
0 & 0 & 0 & 0 & \text{No change} \\
0 & 1 & 0 & 0 & \text{Count down} \\
1 & 0 & 1 & 0 & \text{Count up} \\
1 & 1 & 0 & 0 & \text{No change} \\
\end{array}
\]

6.19  (b) From the state table in Table 6.5:

\[
\begin{align*}
D_{Q0} &= Q_1' \\
D_{Q2} &= \sum (1, 2, 5, 6) \\
D_{Q4} &= \sum (3, 4, 5, 6) \\
D_{Q8} &= \sum (7, 8) \\
\text{Don't care: } d &= \sum (10, 11, 12, 13, 14, 15) \\
\end{align*}
\]

Simplifying with maps:

\[
\begin{align*}
D_{Q2} &= Q_2Q_1' + Q_2Q_1O_1 \\
D_{Q4} &= Q_2Q_1' + Q_2Q_2O_2 + Q_2Q_1O_1 \\
D_{Q8} &= Q_2Q_1' + Q_3Q_1O_1 \\
\end{align*}
\]