

## Chapter 5

### OUTPUT STAGES IN A VOLTAGE AMPLIFIER SYSTEM

#### 5. Output Stage, desirable characteristics

The output stage is supposed to deliver the final output to an appropriate receiving device, i.e., a lamp, human ear, loud speaker, etc. Within the limits of given DC power supplies, the output stage should provide maximum amount of signal power to the load without large dissipation of electrical signal energy as heat. In a voltage amplifier system, the output resistance should be very low. Further, the output signal waveform should be very close replica of the input signal which means that the output should have very small *distortion* characteristic. Usually when devices deliver high power, the operation creeps into the domain of nonlinear characteristics and hence harmonics of the signal are generated at the output. A measure of these harmonics is expressed by Total Harmonic Distortion (THD). A high fidelity audio amplifier will perhaps have a THD of the order of a fraction of a percent i.e., 0.1%.

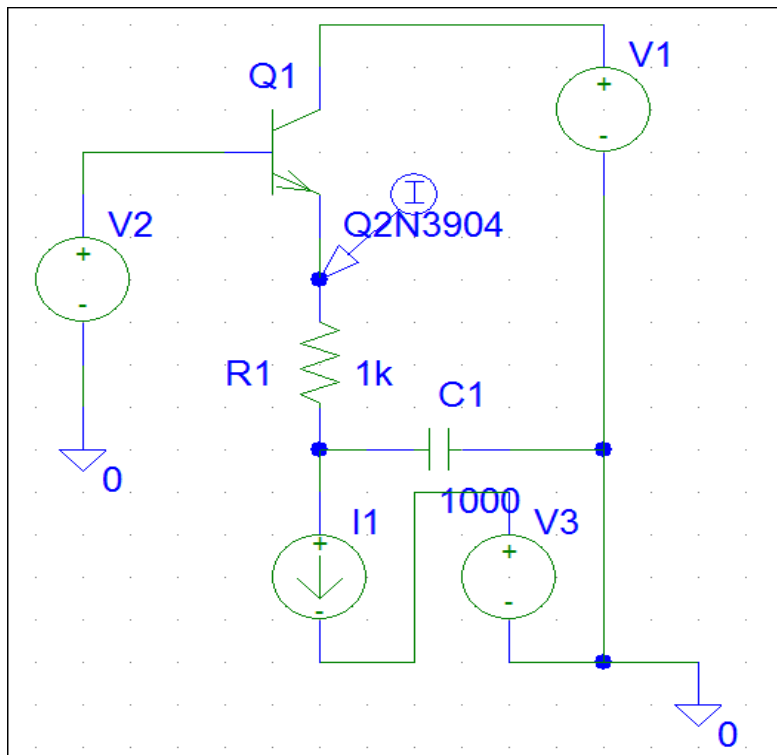
The most challenging task in the design of the output stage is that it delivers the required amount of power to the load in an efficient manner i.e., with as little as possible of power dissipation in the transistors at the output stage. The efficiency depends upon the way the output stage conducts upon application of the signal power. This is achieved by special DC biasing of the transistor. Thus we come across class A, class B and class AB stages. The following are discussed in this chapter.

- Different DC biasing of output stages and associated characteristics
- Special circuits for class AB biasing
- Short circuit protection technique
- Thermal considerations
- Power transistors

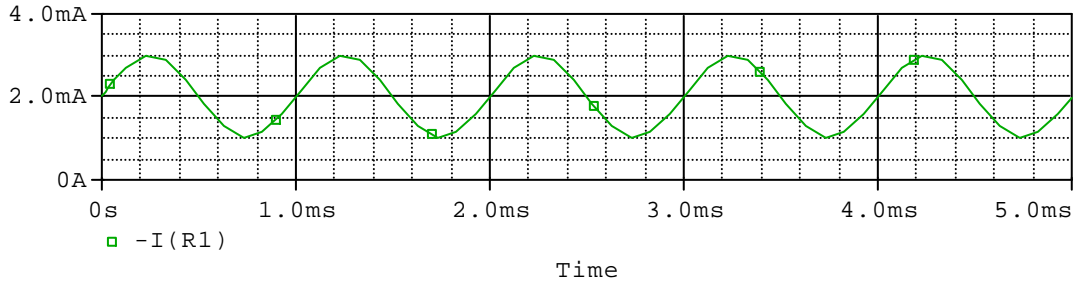
#### 5.1: Operation by Different Biasing

##### 5.1.1: Class A operation

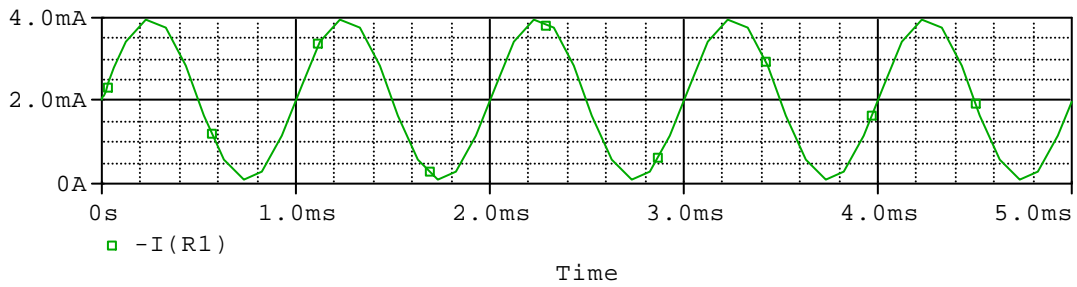
In class A operation, the output stage is biased at a DC current level  $I_C$  which is greater than the peak signal component of the current  $I_m$ . Thus, if the signal is sinusoidal, the instantaneous current through the device never falls below zero over the entire cycle of the input signal. That means the conduction angle of the output stage is  $360^\circ$ , i.e. full cycle. Figures 5.1(a)-(c) demonstrate the concept. The device Q1 is biased with  $I=2\text{mA}$ . The capacitor  $C1$  is for isolating the DC signal and is assumed as a *short circuit* for *ac* signals. When an input signal  $v_I$  of value  $V_m$  is applied, the current  $i_E$  through the emitter resistance  $R1$  follows the input sinusoidal variation as  $v_I/R1$ . As long as  $|V_m/R1|$  is less than  $I$ , the waveform of  $i_E$  resembles that of  $v_I$  (Figs. 5.1(b)-(c)). When  $|V_m/R1|$  exceeds the DC bias current  $I$ ,  $i_E$  becomes *zero* during the negative going excursion of  $v_I$ . Thus, the condition of class A operation is violated (Fig.5.1(d)). The current through  $R1$  and hence the output signal voltage suffers distortion.



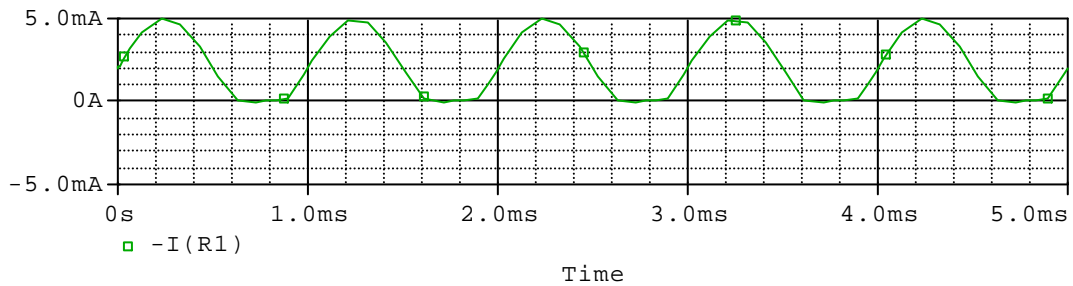
(a)



(b)



(c)

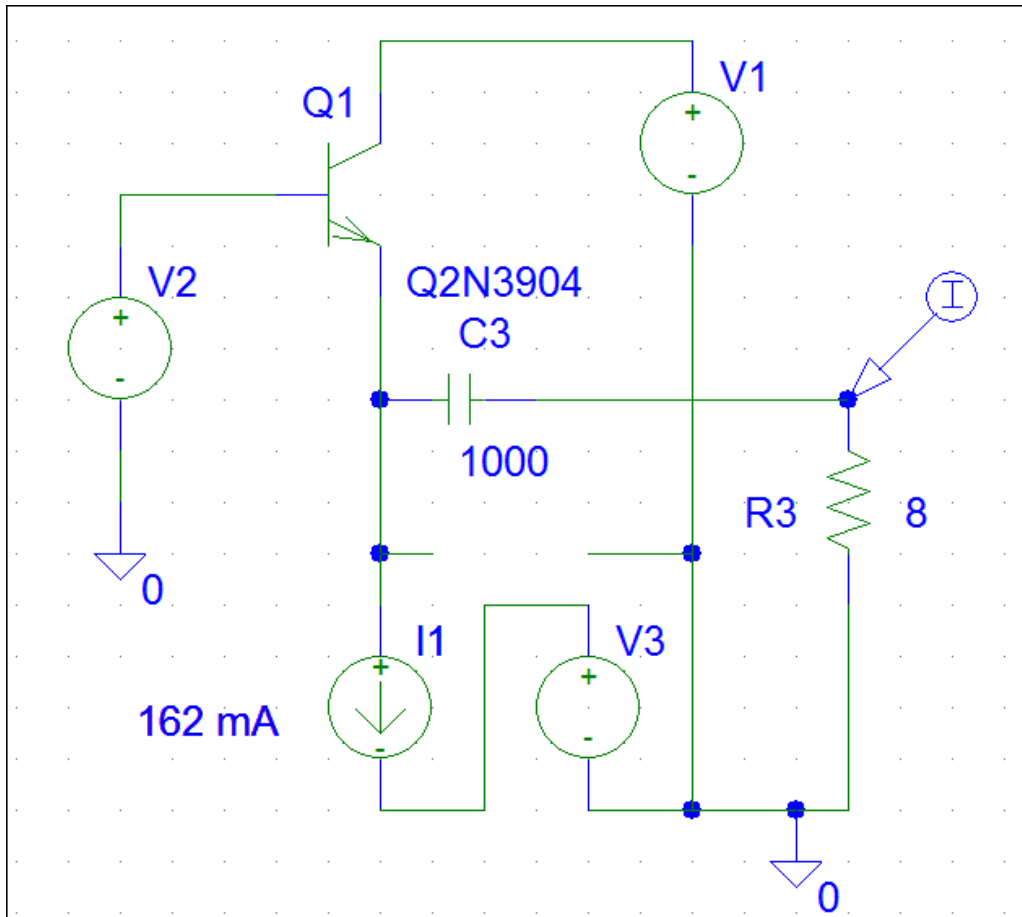


(d)

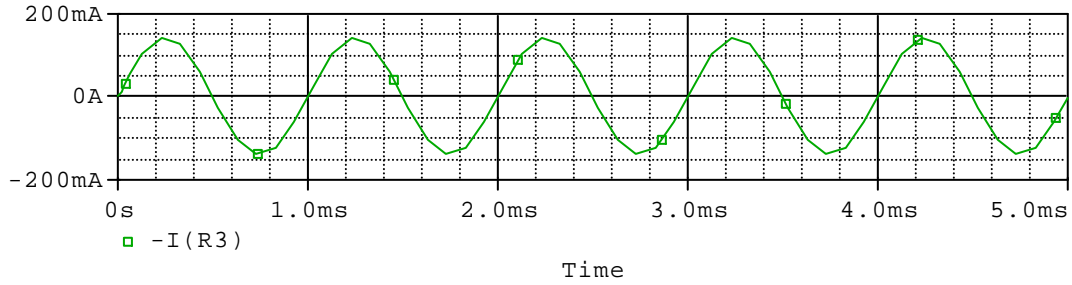
Figure 5.1: DC bias current vs. signal handling capability of Class A output stage (a) the schematic with NPN-BJT device biased for  $I_E=2$  mA, (b)  $V_{SIN}=1$ V peak,  $i_E=1$  mA (peak) sinusoidal around 2 mA DC bias, (c)  $V_{SIN}=2$ V peak,  $i_E=2$  mA (peak) sinusoidal around 2 mA DC bias, (d)  $V_{SIN}=3$ V peak,  $i_E=3$  mA positive peak but cutting off toward the negative peak, being limited by the 2 mA DC bias.

Considering from output side, if the amplifier is required to deliver a given level of voltage (say,  $v_{om}$ ) across the output load (say,  $R_L$ ), the DC bias level should be sufficient ( i.e.,  $> |v_{om}/R_L|$ ) so that the transistor never cuts off (i.e.,  $i_E$  becoming=0) for class A operation. Figure 5.2(a)-(c) illustrate the situation. The schematic in Fig.5.2(a) shows a CC-BJT amplifier output stage biased by a current source and having a load of 8 ohms. It is intended for an output signal power

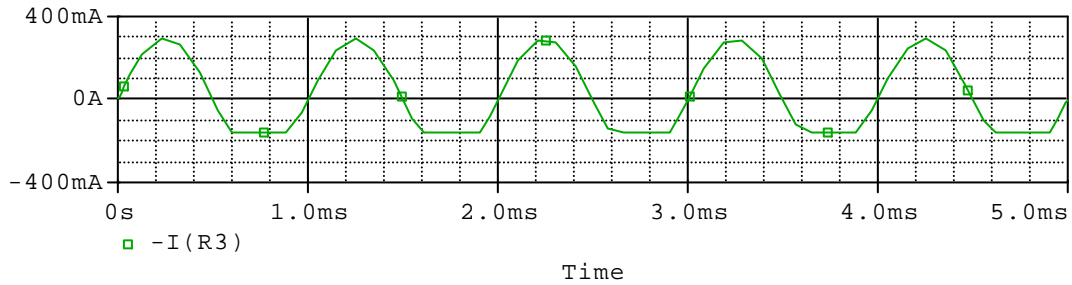
of 100 mW. This corresponds to a peak *ac* current of  $I_m=160$  mA. The capacitor  $C3$  is for isolating the DC signal and is assumed as a *short circuit* for *ac* signals. The DC bias current is set for 162 mA (i.e.,  $> I_m=160$  mA). Figure 5.2(b) shows the case for a load current drive of 150 mA ( $v_{in}=1.2$ V peak Sine-wave), while Fig.5.2(c) depicts the case for a load current drive exceeding the DC bias current of 162 mA. This happens for an input signal drive of 2.5V peak Sine-wave requiring the load current to be (noting that the CC stage has a voltage gain close to unity) 312.5 mA. This current exceeds the DC bias current arranged in Fig.5.2(a). The BE junction of the BJT device cuts off for the duration when the signal current remains below -162 mA (see Fig.5.2(d)). Hence, the output signal (current/voltage) encounters distortion over this duration of time.



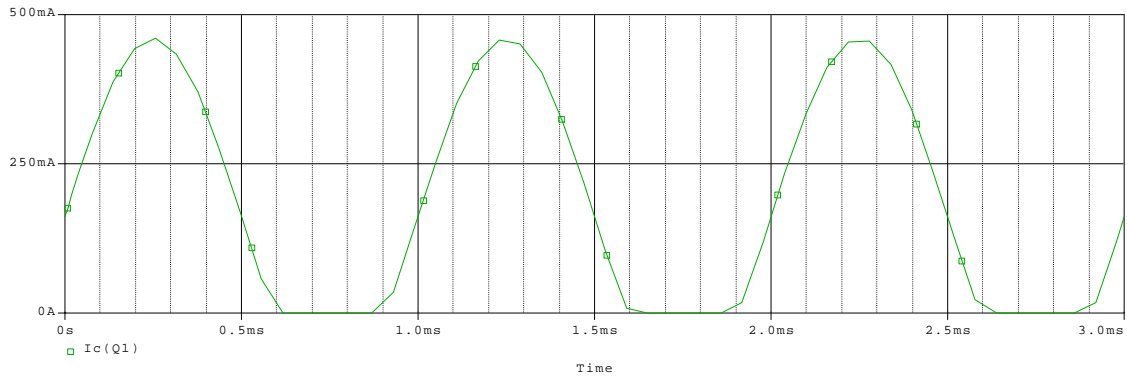
(a)



(b)



(c)



(d)

Figure 5.2: A CC-BJT output stage rated for 100 mW of output power ( $v_L=1.28V$  peak); (a) the schematic, (b) output current for  $v_L=v_{in}=1.2V$  peak, (c) output current for  $v_L=v_{in}=2.5V$  peak, (d) current through the BJT device for  $v_L=v_{in}=2.5V$  peak

### 5.1.1.1: Bias current circuit design

Consider a CC-BJT amplifier in an IC environment where the device  $Q_1$  (an NPN BJT device) is biased by the current-mirror circuit comprised of  $Q_2$  and  $Q_3$  (see Figure 5.3). The instantaneous load current is  $i_L$ , and the dc bias current is  $I$ . Then

$$i_{E1} = I + i_L$$

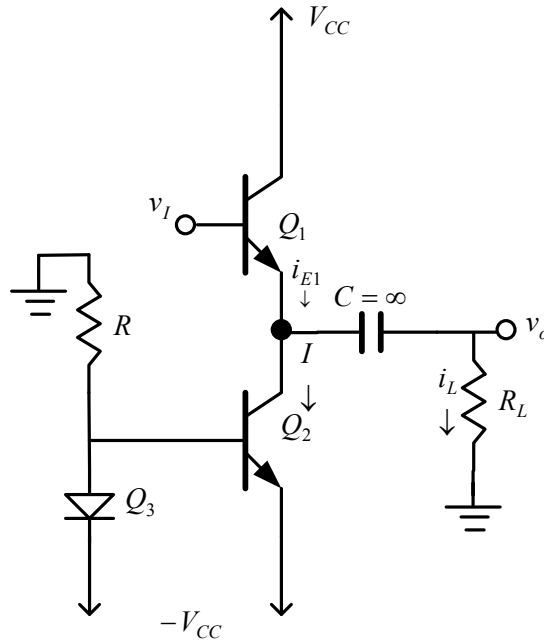


Figure 5.3: Class A output stage biased by a diode connected transistor  $Q_3$ .  $Q_2$  serves as a bias source for  $Q_1$ .

For class A operation,  $i_{E1}$  is always  $> 0$  ie  $I > i_L$ . In the linear operation region, maximum positive output is  $v_o^+ |_{\max} = V_{CC} - v_{CE,sat} |_{Q1}$ . Similarly, maximum negative output is  $v_o^- |_{\max} = -V_{CC} + v_{CE,sat} |_{Q2}$

Corresponding to the worst case negative swing at the output, the load current will be

$i_L = \frac{-V_{CC} + v_{CE,sat} |_{Q2}}{R_L}$ , where  $R_L$  is the load resistance. Since, for class A operation  $I > i_L$ , then

$I > i_L = \frac{-V_{CC} + v_{CE,sat} |_{Q2}}{R_L}$ , gives a guideline for designing the proper DC bias current for class A

operation. On the positive swing side:  $I \leq \frac{V_{CC} - v_{CE,sat} |_{Q1}}{R_L}$ . In a practical case one need to choose

higher of the two possible values of  $I$ . The biasing resistance in the reference current source transistor ( $Q_3$ ) can now be chosen as (ignoring the effect of finite  $\beta$  of the BJT)

$$R \leq \frac{0 - (-V_{CC} + 0.7)}{I}$$

*Example 5.1.1.1:* In Fig.5.3 consider  $V_{CC} = 15\text{V}$ ,  $V_{CE(sat)} = 0.2\text{V}$ ,  $V_{BE} = 0.7\text{V}$ , and that  $h_{FE}$  is very high. Find  $R$  to allow for the largest possible output signal swing across the load  $R_L = 1\text{k}\Omega$ . Determine the minimum and maximum currents through the device  $Q_1$ .

*Solution/hints:*

Maximum signal swing  $= 15 - 0.2 = 14.8\text{V}$  peak (both positive and negative)

Peak load current  $i_L = 14.8\text{V}/1\text{k}\Omega = 14.8\text{ mA}$  (both positive and negative)

For class A operation,  $i_{E1} = i_L + I$  will always be  $> 0$ , so  $I = 14.8\text{ mA}$ .

With  $h_{FE}$  very high,  $I_{REF} = I_C$  in  $Q_3$  will be  $= I = 14.8\text{ mA}$ .

With  $V_{BE} = 0.7\text{V}$ ,  $R = [(-15) + 0.7]/14.8\text{ mA} = 0.97\text{k}\Omega$ .

Minimum (instantaneous) current through  $Q_1 = 0$

Maximum (instantaneous) current through  $Q_1 = 14.8$  times  $2 = 29.6\text{ mA}$  (assuming a sinusoidal input signal).

### 5.1.1.2: Power conversion efficiency

In the class A amplifier the DC power consumption is  $= I(V_{CC} \text{ in } Q_1 - (-V_{CC} \text{ in } Q_2)) = 2IV_{CC} \rightarrow$  both carrying average current  $I$  and bus to bus voltage being  $2V_{CC}$ . Let  $P_s = 2IV_{CC}$  be the power drawn from the supply bus.

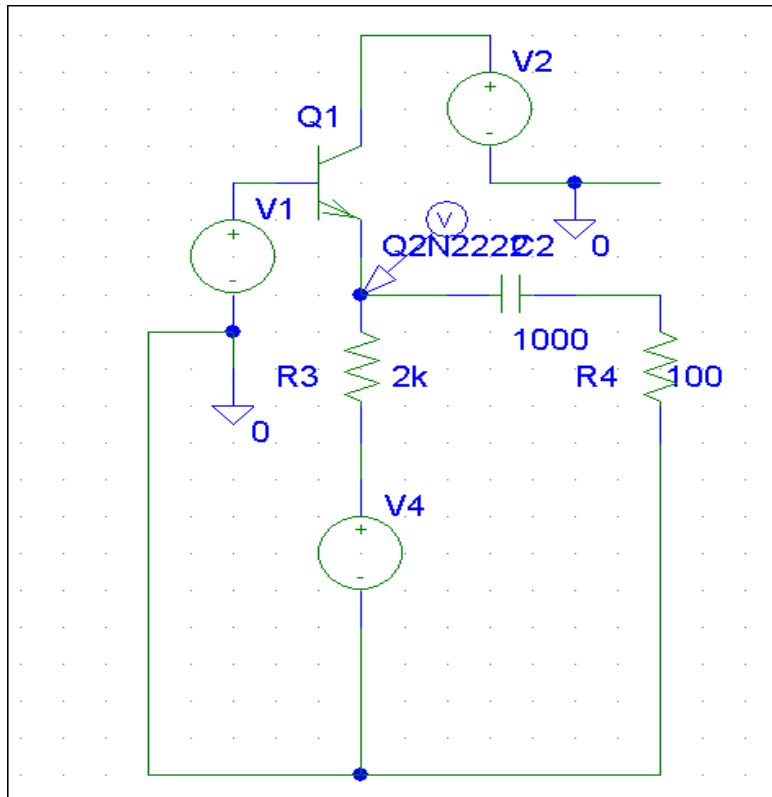
Average ac (sinusoidal) signal power delivered to the load is :  $P_L = \frac{\hat{v}_o^2}{2R_L}$ , where  $\hat{v}_o$  is the peak output ac voltage.

Efficiency of power conversion  $\eta = \frac{P_L}{P_s} = \frac{1}{4} \frac{\hat{v}_o^2}{V_{CC} IR_L}$ .

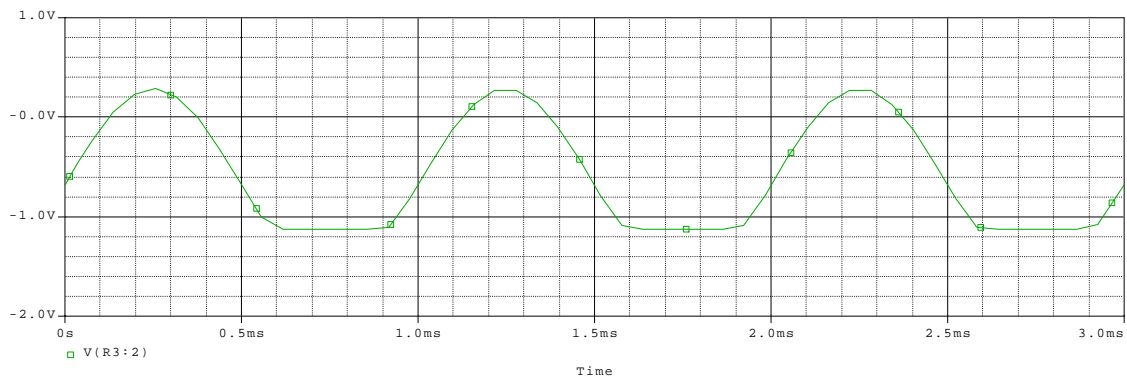
The highest value of the efficiency will be  $1/4$ , i.e., 25% when  $\hat{v}_o = V_{CC} = IR_L$ . In general, since  $\hat{v}_o < V_{CC}$ , and  $\hat{v}_o < IR_L$  the power conversion efficiency will be  $< 1/4$ , i.e., 25%. The best case efficiency that can be obtained in a Class A operation is thus 25%.

### 5.1.2 : Class B operation

In class B operation, the DC bias current through the device (Fig.5.4(a)) is kept at zero. So the device conducts current for only  $1/2$  of the input signal cycle (Fig.5.4(b)). The conduction angle is thus, 180. The output signal is highly non-linear. To overcome this drawback a complementary pair of PNP and NPN transistors is used in practice.



(a)



(b)

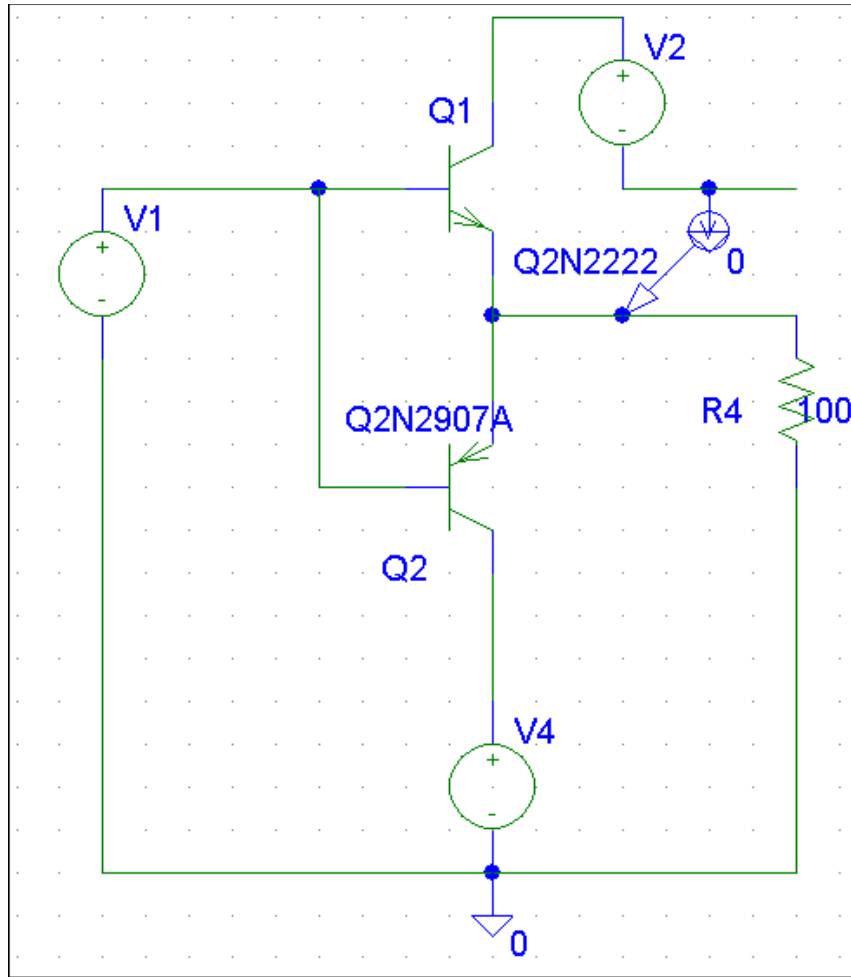
Figure 5.4: Class B amplifier stage (a) schematic (in PSpice), (b) output waveform at the emitter of the BJT.

#### 5.1.2.1: Practical Class B output stage

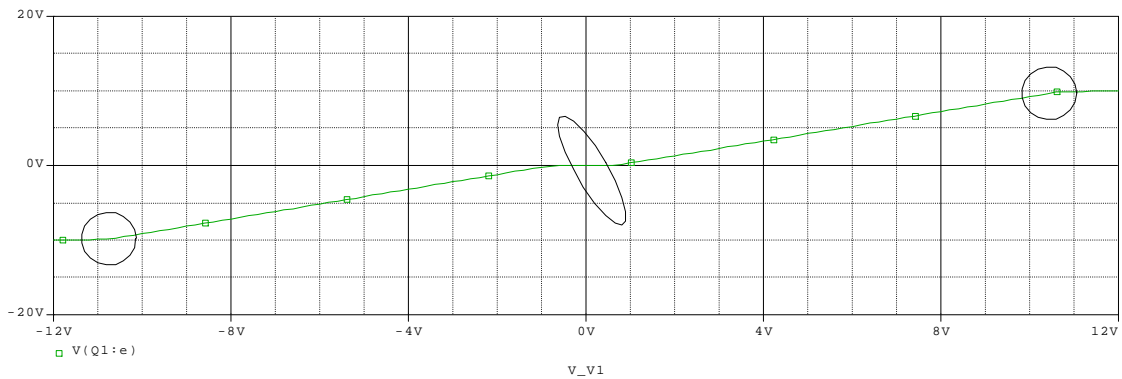
A practical class B amplifier using BJT devices appears as in Fig.5.5(a). The linearity characteristic of the amplifier is shown in Fig.5.5(b) and the output waveform with a sinusoidal



input signal appears as in Fig.5.5(c). The linearity characteristic (Fig.5.5(b)) shows saturation at the limits of the DC supply voltages ( $\pm 10\text{V}$  in this case) and a no-conduction zone (shown by an *elliptic* curve in Fig.5.5(b)) when the input is within  $\pm V_\gamma$ , where  $V_\gamma$  is the cut-in voltage of the emitter-base junction of the transistors.



(a)



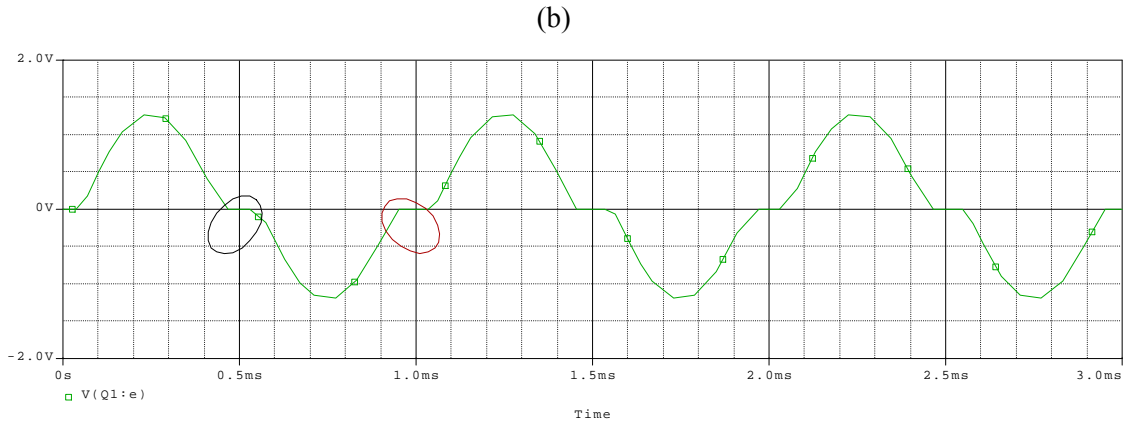


Figure 5.5: (a) Schematic of a class B output stage using BJT devices, (b) large signal output-input characteristic, (c) output with sinusoidal input.

Figure 5.5(c) shows the output for an input sinusoidal signal. The region of no (or poor) conduction corresponds to zero (or very small) output (shown by elliptic enclosure). This produces distortion components at the output. The distortion is referred to as *crossover* distortion since the distortion occurs when the current conduction changes over from one transistor (say, the NPN) to the other (i.e., the PNP) and vice versa. SPICE analysis of the

#### FOURIER COMPONENTS OF TRANSIENT RESPONSE V(R\_R4)

DC COMPONENT = -3.004535E-02

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.070E+00	1.000E+00	1.796E+02	0.000E+00
2	2.000E+03	1.806E-02	1.687E-02	9.215E+01	-2.670E+02
3	3.000E+03	2.128E-01	1.988E-01	2.249E+00	-5.364E+02
4	4.000E+03	1.557E-02	1.454E-02	8.659E+01	-6.317E+02
5	5.000E+03	7.293E-02	6.813E-02	1.817E+00	-8.960E+02
6	6.000E+03	1.375E-02	1.285E-02	8.499E+01	-9.924E+02
7	7.000E+03	2.218E-02	2.072E-02	6.019E+00	-1.251E+03
8	8.000E+03	1.340E-02	1.252E-02	8.185E+01	-1.355E+03
9	9.000E+03	9.838E-03	9.191E-03	3.431E+01	-1.582E+03

TOTAL HARMONIC DISTORTION = 2.132541E+01 PERCENT

circuit in Fig.5.5(a) indicates a total harmonic distortion (THD) of of 21.32%. The principal contribution to the THD comes from the crossover distortion.

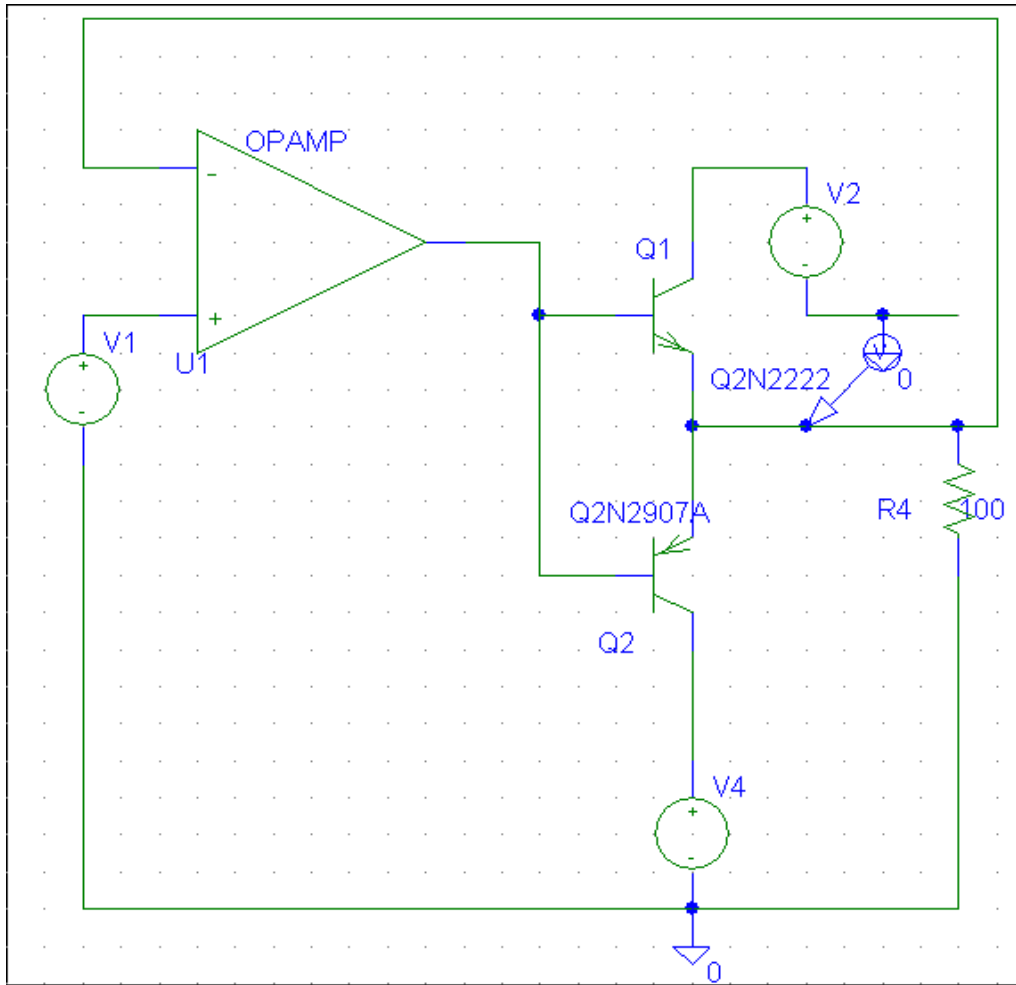
The crossover distortion can be reduced by including the class B stage in a negative feedback loop with a high gain amplifier (i.e., an operational amplifier). The circuit is shown in figure 5.6(a). The output waveform now appears as in figure 5.6(b). The Fourier analysis data shows a THD of only 0.093%.

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(R\_R4)

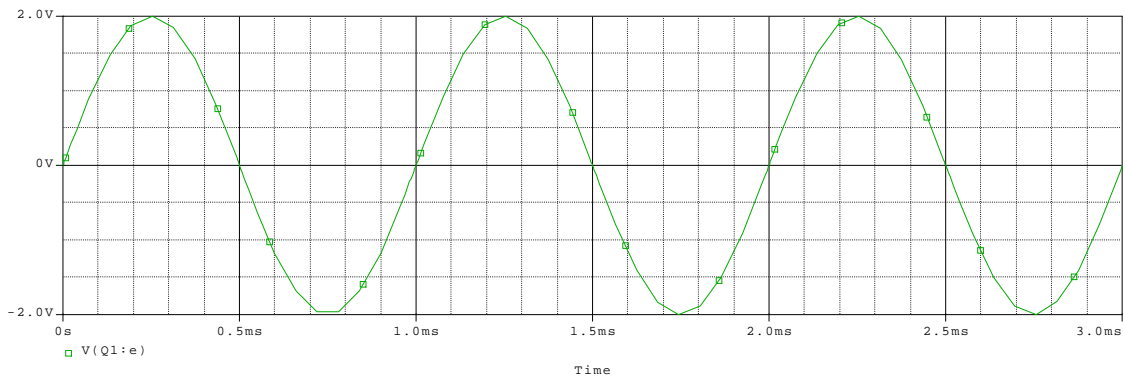
DC COMPONENT = -7.467272E-05

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.977E+00	1.000E+00	-1.800E+02	0.000E+00
2	2.000E+03	1.595E-04	8.070E-05	1.850E+01	3.784E+02
3	3.000E+03	1.154E-03	5.839E-04	-1.329E+02	4.070E+02
4	4.000E+03	2.000E-05	1.012E-05	-1.010E+01	7.098E+02
5	5.000E+03	9.928E-04	5.023E-04	-1.613E+02	7.385E+02
6	6.000E+03	1.960E-05	9.914E-06	-8.828E+01	9.915E+02
7	7.000E+03	8.112E-04	4.104E-04	1.667E+02	1.426E+03
8	8.000E+03	3.022E-05	1.529E-05	-1.319E+02	1.308E+03
9	9.000E+03	6.182E-04	3.128E-04	1.272E+02	1.747E+03

TOTAL HARMONIC DISTORTION = 9.308423E-02 PERCENT



(a)



(b)

Figure 5.6: Class B output stage with reduced crossover distortion arrangement (a) the schematic, (b) the output waveform.

### 5.1.2.2: Power Conversion Efficiency

Consider the illustrations shown in Fig. 5.7. The traces in *red* corresponds to conduction by the NPN BJT and the traces in blue are due to conduction of the PNP BJT. We have ignored the crossover distortion zone (*dead-zone*) in this case. If  $\hat{v}_o$  is the peak value of the output voltage  $v_o$ , the average signal power output is  $\hat{v}_o^2 / 2R_L$  (ignoring the dead-zone effect). For the positive half of  $v_i$ , the load current comprise of half sinusoids (ignoring the dead zone) like in a half-wave rectifier (*red* traces). So the average current will be  $\frac{1}{\pi} \frac{\hat{v}_o}{R_L}$  (as obtained by Fourier Series expansion). Similarly, for the negative half of

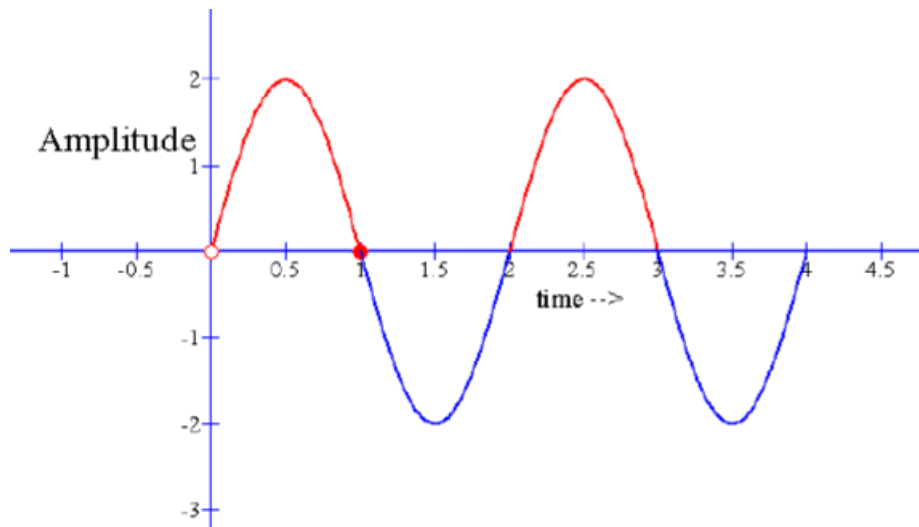


Figure 5.7: Output wave shapes in class B operation (*red* trace due to  $Q_1$ , and *blue* trace due to  $Q_2$ ). The crossover distortion component has been assumed negligible.

$v_i$ , the load current will appear as a half-wave rectified form, but all the lobes will be in the negative direction now (*blue* traces in Fig.5.7). So the average dc current in this case will be

$$-\frac{1}{\pi} \frac{\hat{v}_o}{R_L}$$

When  $v_I$  is  $>0$ , the dc power is consumed from  $+V_{CC}$  supply. So the average power consumed is:

$V_{CC} \frac{1}{\pi} \frac{\hat{v}_o}{R_L}$ . When  $v_I$  is  $<0$ , the dc power is consumed from  $-V_{CC}$  supply. So the average power

consumed is  $(-V_{CC})(-\frac{1}{\pi} \frac{\hat{v}_o}{R_L})$ .

Net average power consumed over the entire period of  $v_I = 2 V_{CC} \frac{1}{\pi} \frac{\hat{v}_o}{R_L}$ . Then, power conversion

efficiency is: (average signal power in  $R_L$ ) / (average power consumed from the DC supply rails)

$$= (\hat{v}_o^2 / 2R_L) / (2V_{CC}\hat{v}_o / \pi R_L)$$

In an ideal case (ignoring  $v_{CE,sat}$  of the BJT devices),  $\hat{v}_o \cong V_{CC}$ . So the best case efficiency  $\eta$  will

be  $\pi/4$ , i.e., about 78.5%. Maximum average signal power available from a class B output stage

is obtained by putting  $\hat{v}_o \cong V_{CC}$ , and is  $(1/2)(V_{CC}^2 / R_L)$ .

### 5.1.2.3: Power Dissipation in the Devices (i.e., transistors) for class B operation

In class B stage, no power is dissipated under quiescent (no signal) condition. When a signal is applied, a certain part of the power is dissipated as heat in the device. This can be figured out as follows.

$$P_D = P_{sup} - P_L = \text{DC supply power} - \text{average signal power at load.}$$

Since (for sinusoidal output signal)  $P_L|_{avg} = v_o^2 / 2R_L$ , and  $P_{sup} = 2\hat{v}_o V_{CC} / \pi R_L$ ,

$$P_D = \frac{2}{\pi} \frac{\hat{v}_o}{R_L} V_{CC} - \frac{1}{2} \frac{\hat{v}_o^2}{R_L}. \text{ Thus, } P_D \text{ depends on } v_o \text{ by a non-linear (i.e., quadratic) relation.}$$

So, a maximum or minimum of  $P_D$  is possible, as a function of  $v_o$ . This can be formed, by letting

$\partial P_D / \partial \hat{v}_o = 0$ , and checking the sign of  $\partial^2 P_D / \partial \hat{v}_o^2$ . The procedure leads to an optimum value for

$v_o$ ,  $v_o|_{opt} = (2/\pi) V_{CC}$  for a maximum of  $P_D$ . Then,  $P_D|_{max}$  (by substituting  $v_o = (2/\pi) V_{CC}$ ) in

the above expression) =  $\frac{2}{\pi^2} \frac{V_{CC}^2}{R_L}$  (see Fig.5.8).

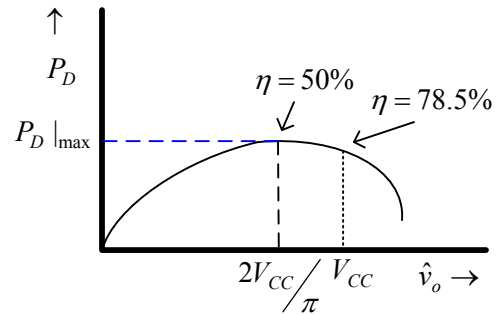


Figure 5.8: Plot of power dissipation with output voltage magnitude

One- half of this power is dissipated in each of the P-and N type BJT. So each transistor dissipates a maximum power of  $P_{D|_{\max}}/2$ , i.e.,  $\frac{1}{\pi^2} \frac{V_{CC}^2}{R_L}$ ; a fact to be considered to choose proper BJT devices for the design of the output stage.

When the transistors dissipates maximum power, the efficiency drops. Thus,

$$\eta = \frac{\pi}{4} \frac{\hat{v}_o}{V_{CC}} \Big|_{\hat{v}_o = \frac{2}{\pi} V_{CC}} = \frac{1}{2}, \text{ i.e., } 50\% \text{ only.}$$

*Example 5.1.2.1:*

*Example 5.1.2.1:* In a class B output stage we need the average output signal power to be 20W across an 8Ω load. The DC supply should be about 5V greater than the peak output voltage.

Determine

- (i) DC supply required.
- (ii) Peak current drawn from each supply.
- (iii) Total power drawn from the DC supplies.
- (iv) Power conversion efficiency.
- (v) Power dissipation in each transistor of the class B circuit.

*Solution/hints:* (i)  $P_L = \frac{1}{2} \frac{\hat{v}_o^2}{R_L} = 20$ , gives  $\hat{v}_o = 17.9$  V. Then  $V_{CC} = |-V_{CC}| = 5 + 17.9 \cong 23$  V.

(ii) Peak current  $= \frac{17.9}{8} = 2.24$  A drawn from each supply.

(iii) Average current drawn from each supply is  $\frac{\hat{i}_L}{\pi} = 0.713$  A. So average DC power drawn from the two DC supplies is  $2 \times 23 \times 0.713 = 32.79$  W.

(iv) Power conversion efficiency  $\eta = \frac{20}{32.79} \rightarrow 61\%$

(v) Power dissipation in each transistor  $(32.79 - 20)/2 = 6.4$  W. The maximum power

dissipation in each transistor will be  $\frac{V_{CC}^2}{\pi^2} \frac{1}{R_L} \cong 6.7$  W

### 5.1.3: Class AB Operation

#### 5.1.3.1: *Principle of operation*

In class AB operation, a small DC bias is added to the base of a complementary (i.e., PNP-NPN BJT, or PMOS-NMOS devices) pair. As a result, with input signal  $v_I = 0$ , a small quiescent current  $I_Q$  flows. The load current  $i_L$  remains = 0. Thus consider the schematic in Fig. 5.9. For  $v_I = 0$ ,  $i_L = 0$ ,  $i_P = i_N = I_Q = I_S e^{V_{BB}/2V_T}$ , where we have assumed  $I_S$  for both NPN and PNP device as same. The bias voltage  $V_{BB}$  is set up to produce the required  $I_Q$ .

When  $v_I$  increases  $Q_N$  conducts more since  $v_{BEN}$  becomes higher than  $V_{BB}/2$ ; similarly  $Q_P$  conducts less since  $v_{EBP}$ , goes below  $V_{BB}/2$ . The difference  $i_N - i_P = i_L$  flows out as load



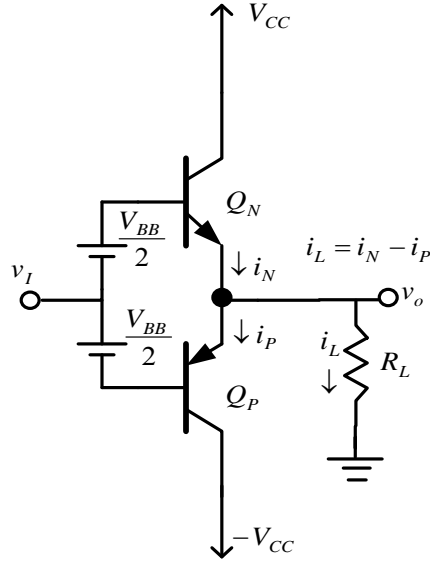


Figure 5.9: Schematic of a basic class AB output amplifier using BJT devices

current  $i_L$  producing the output  $v_o = i_L R_L$ , increasing in the positive direction. Specifically,  $v_o = v_I + V_{BB}/2 - v_{BEN}$ .

The increase in  $i_N$  is accompanied by a corresponding decrease (or vice versa) in  $i_P$  in accordance with the relation as derived below.

$v_{BEN} + v_{EBP} = V_{BB}$ ,  $i_N = I_S e^{v_{BEN}/V_T}$ ,  $i_P = I_S e^{v_{EBP}/V_T}$ . Then,  $v_{BEN} = V_T \ln(i_N / I_S)$ ,  $v_{EBP} = V_T \ln(i_P / I_S)$ , while from  $I_Q = I_S e^{V_{BB}/2V_T}$ , we get:  $V_{BB} = 2V_T \ln(I_Q / I_S)$ . Then,

$V_T \ln(i_N / I_S) + V_T \ln(i_P / I_S) = 2V_T \ln(I_Q / I_S)$ , leading to  $i_N i_P = I_Q^2$ , which holds right from the quiescent point (i.e.,  $v_I = 0$ ). The equation  $i_N i_P = I_Q^2$  can be combined with  $i_L = i_N - i_P$  to solve for either  $i_N$  or  $i_P$  in terms of  $I_Q$  and  $i_L$  in a quadratic equation of the form, for example, in  $i_N$  (substituting  $i_P = i_N - i_L$ ):

$$i_N^2 - i_L i_N - I_Q^2 = 0$$

When  $v_I$  goes negative,  $v_{EBP}$  increases,  $v_{BEN}$  decreases,  $i_N$  decreases,  $i_P$  increases,  $i_L$  reverses sign and  $v_o$  decreases towards negative values thereby following  $v_I$  again. This accounts for the negative going swing of  $v_o$ . Thus the push-pull action as in class B stage continues. Since  $I_Q \neq 0$

, transition of conduction from the NMOS to PMOS occurs in a smooth manner. Cross-over distortion is thereby reduced considerably.

Figure 5.10(a) shows the PSpice schematic of a class AB output stage. Figure 5.10(b) shows the output waveform for an input signal of 1kHz with 2V amplitude. The crossover distortion zone is considerably reduced compared with that in Fig.5.5(c) (class B output stage).

*Example 5.1.3.1:* For a class AB stage shown in figure 5.11, consider the given data:

$V_{CC}=15V$ ;  $R_L=100\Omega$ ;  $v_o=10\sin \omega t$ ; the output devices  $Q_P$  and  $Q_N$  are matched with  $I_S = 10^{-13} A$ ;  $h_{FE}=50$ ; The biasing diodes have  $1/3^{\text{rd}}$  the junction area of the output devices.

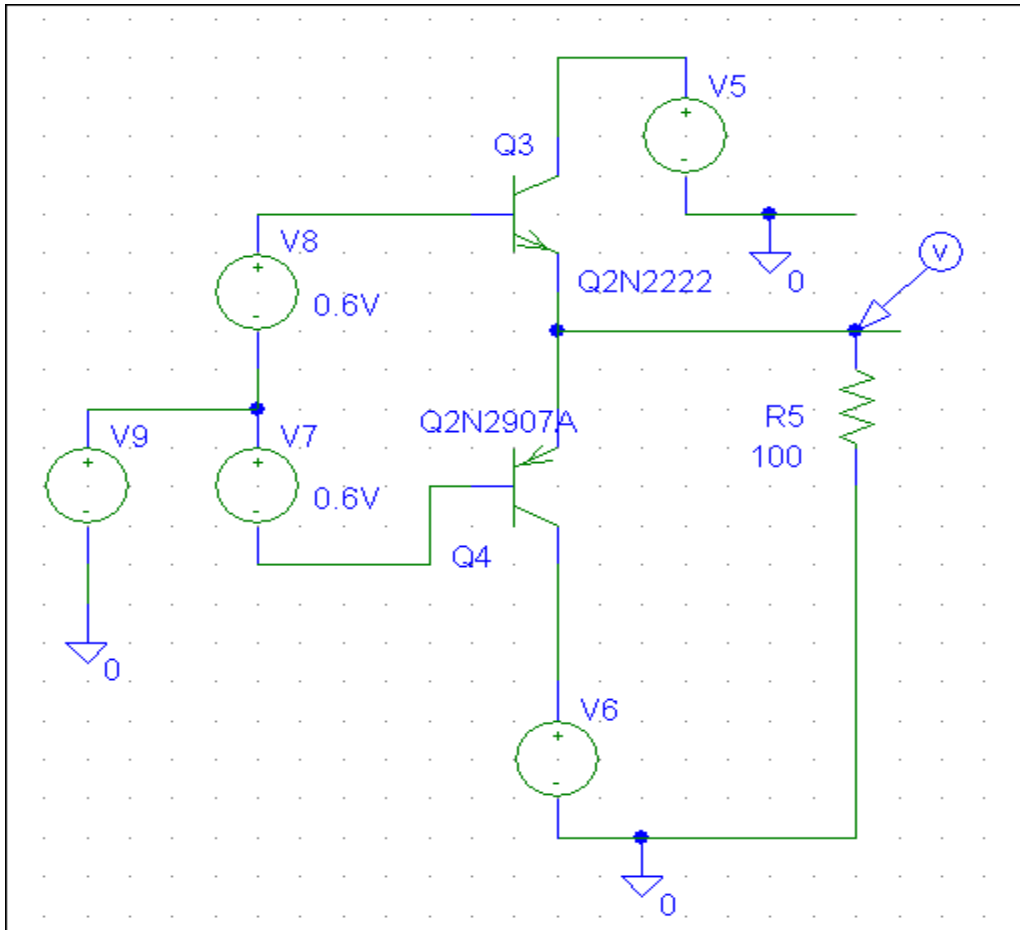
Find (i) The value of required  $I_{Bias}$  so that a minimum of 1mA current flows through the biasing diodes *all the time*.

(ii) The *zero signal* (i.e., quiescent) bias current through the output devices.

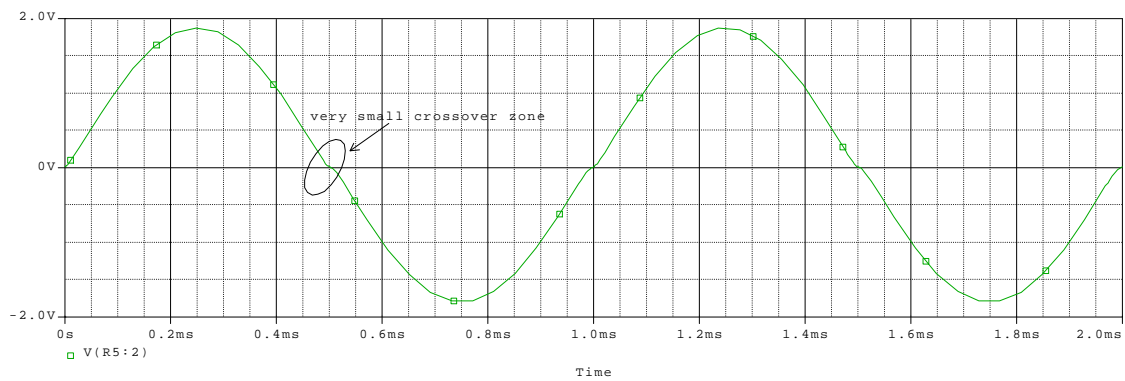
(iii) Quiescent power dissipation in the devices.

(iv)  $V_{BB}$  for  $v_o = 0$

(v)  $V_{BB}$  for  $v_o = 10V$  peak



(a)



(b)

Figure 5.10: Performance of a class AB output stage; (a) PSpice schematic, (b) output waveform for 1kHz input sinusoidal signal of 2V amplitude.

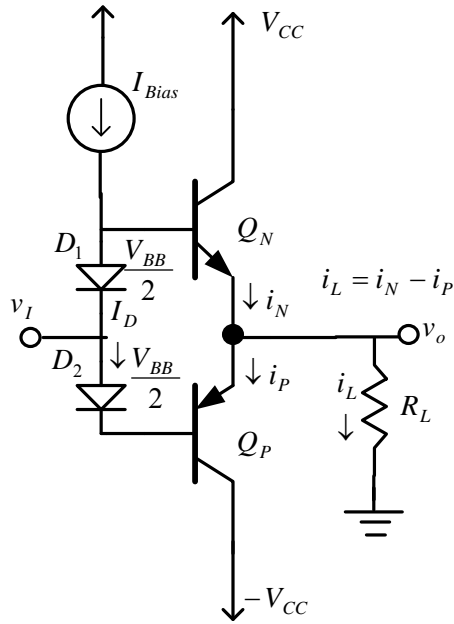


Figure 5.11 (refer *Example 5.1.3.1*)

*Solution/hints:*

(i) Since  $v_o$  (peak) is 10V,  $i_L(\text{peak}) = \hat{i}_L = 0.1 \text{ A}$ .

For maximum positive swing of  $v_o$ ,  $i_N|_{\text{max}} = \hat{i}_L = 0.1 \text{ A} = 100 \text{ mA}$ .

Then  $i_{BN}|_{\text{max}} = \frac{100}{h_{FE}} = 2 \text{ mA}$ . The current through the diode column follows the KCL

equation:  $I_D = I_{Bias} - i_{BN}$ . Then for a minimum value of  $I_D = 1 \text{ mA}$ , we must have  $I_{Bias} \geq 3 \text{ mA}$

(ii) Let  $I_{Bias} = 3 \text{ mA}$ . Since  $Q_N, Q_P$  has three times the junction area relative to the biasing diodes ( $D_1, D_2$ ),  $I_Q$  for the output devices will be *three* times of 3mA, i.e., 9 mA.

(iii) Quiescent power dissipation is  $2 \times 15 \times 9 = 270 \text{ mW}$ .

(iv) For  $v_o = 0$ ,  $i_{BN} = 9/50 = 0.18 \text{ mA}$ . Then  $I_D = 3 - 0.18 = 2.82 \text{ mA}$ . For the diodes

$I'_S = I_S/3 = 0.33 \times 10^{-14} \text{ mA}$ . We now have to use the diode I-V equation

$I_D = I'_S \exp\left(\frac{V_{BB}}{2V_T}\right)$ , with  $V_T = 25 \text{ mV}$  (assumed since no other value is provided). Thus,

$V_{BB} = 1.26 \text{ V}$ .

(v) For  $v_o(\text{peak}) = 10 \text{ V}$ ,  $i_{BN} = 2 \text{ mA}$ ,  $I_D = 1 \text{ mA}$ ,  $V_{BB} = 1.21 \text{ V}$ .

In practice two diode connected transistors can be used for  $D_1$ , and  $D_2$ .

## 5.2: Different techniques for deriving the bias voltage $V_{BB}$

### 5.2.1: Class AB biasing circuit using $V_{BE}$ multiplier

Figure 5.12 shows a popular technique to derive the biasing voltage  $V_{BB}$  in class AB output stage.

In transistor  $Q_1$ , if the base current is neglected, we can see that  $V_{BE1} = I_R \cdot R_1$ . Then,

$$V_{BB} = I_R (R_1 + R_2) = V_{BE1} \left(1 + \frac{R_2}{R_1}\right). \text{ Hence the name } V_{BE}\text{-multiplier. Choosing the ratio } R_2/R_1, \text{ any}$$

suitable  $V_{BB}$  value (greater than  $V_{BE1}$ ) can be generated.

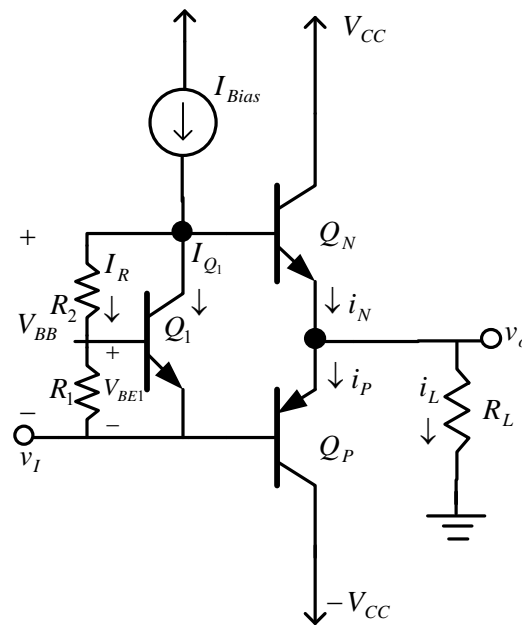


Figure 5.12: Class AB stage with  $V_{BE}$  multiplier circuit.

$V_{BE1}$  is basically related to the collector current of  $Q_1$ . Thus,  $I_{C1} = I_{S1} e^{V_{BE1}/V_T}$ , where  $I_{C1} = I_{Bias} - I_R$  (neglecting  $i_{BN}$ ). Then  $V_{BE1} = V_T \ln(I_{C1}/I_{S1})$ . Another assumption is that during the positive half cycle or positive going swing of  $v_o$ ,  $i_{BN}$  increases and this might compete with  $I_{C1}$  since  $I_{Bias} = I_{C1} + I_R + i_{BN}$ . Since  $i_{BN}$  is very small and even large change in  $I_{C1}$  may cause only little change in  $V_{BE1}$  (because of exponential  $I$ - $V$  relation),  $V_{BE1}$  and hence  $V_{BB}$  remains substantially unchanged.

*Example 5.2.1.1:* For a class AB stage shown in figure 5.12, consider the following:

$V_{CC}=15V$ ;  $R_L=100\Omega$ ;  $v_o=10\sin \omega t$ ; the output devices  $Q_P$  and  $Q_N$  are matched with  $I_S = 10^{-13} A$ ;  $h_{FE}=50$ ; In absence of any signal  $I_{Q_N} = I_{Q_P} = 2mA$ . The transistor  $Q_I$  has  $I_S=10^{-14} A$ . The  $I_{Bias}$  has to drive a minimum of 1mA through the  $V_{BE}$  multiplier circuit when the maximum input signal drive occurs producing a corresponding maximum output voltage level of 10V peak.

Provide a design for the  $V_{BE}$  multiplier circuit.

*Solution/hint:* Following the case for *Example 5.1.3.1*, we see that for peak value of  $v_o$  (i.e., 10V),  $i_L(\text{peak})=\hat{i}_L = 0.1A=i_N |_{\text{max}}$ .

Then  $i_{BN} |_{\text{max}} = \frac{100}{h_{FE}} = 2 \text{ mA}$ . Thus  $I_{Bias} = I_R + I_{Q1} + i_{BN} |_{\text{max}}$  must be  $\geq 3 \text{ mA}$ . The 1mA current through the  $V_{BE}$  multiplier circuit can be distributed as  $I_R = 0.5 \text{ mA}$ , and  $I_{Q1} = 0.5 \text{ mA}$ .

With *minimum signal* drive (i.e.,  $v_o=0$ ) the entire  $I_{Bias}$  of 3mA will be divided between  $I_R$  and  $I_{Q1}$ .

We will assume the distribution as  $I_R = 0.5 \text{ mA}$  and  $I_{Q1} = 2.5\text{mA}$ .

For  $v_o=0$ , the condition  $I_{Q_N} = I_{Q_P} = 2\text{mA}$ , leads to  $V_{BB} = 2V_T \ln(2 \times 10^{-3} / 10^{-13}) = 1.185V$ . This being the voltage drop across  $R_1, R_2$  in series with  $I_R = 0.5 \text{ mA}$ , we can deduce  $R_1 + R_2 = 2.38 \text{ k}\Omega$ .

At the same time the value  $I_{Q1} = 2.5\text{mA}$  provides  $V_{BE1} = V_T \ln(2.5 \times 10^{-3} / 10^{-14}) = 0.66V$ . Hence  $R_1 = 0.66V / 0.5\text{mA} = 1.32 \text{ k}\Omega$ . Then  $R_2 = 1.06 \text{ k}\Omega$ .

### 5.2.2: Class AB biasing circuit using complementary CC stages

Figure 5.13 shows an arrangement where a complementary pair of common collector (CC) BJT devices are used to provide the  $V_{BB}$  bias to the output transistors  $Q_P$  and  $Q_N$ . The resistances  $R_{E1}$ ,  $R_{E2}$  ensure to stabilize the DC bias current through  $Q_N$ ,  $Q_P$  transistors. The resistances  $R_1$ , and  $R_2$  are designed to provide the required  $V_{BB} = V_{E1} - V_{E2}$ , where  $V_{E1}$  and  $V_{E2}$  are dependent upon the DC bias component in  $v_i$ , the input signal.

### 5.2.3: Class AB output stage using compound transistors

Figures 5.14(a)-(b) show two compound transistor stages each of which is equivalent to a single transistor with an effective current gain factor equal to the product of the individual current gain factor of the constituent transistors. The arrangement in Fig.5.14(a) is also known as *Darlington* pair, while Fig.5.14(b) presents a compound PNP transistor.

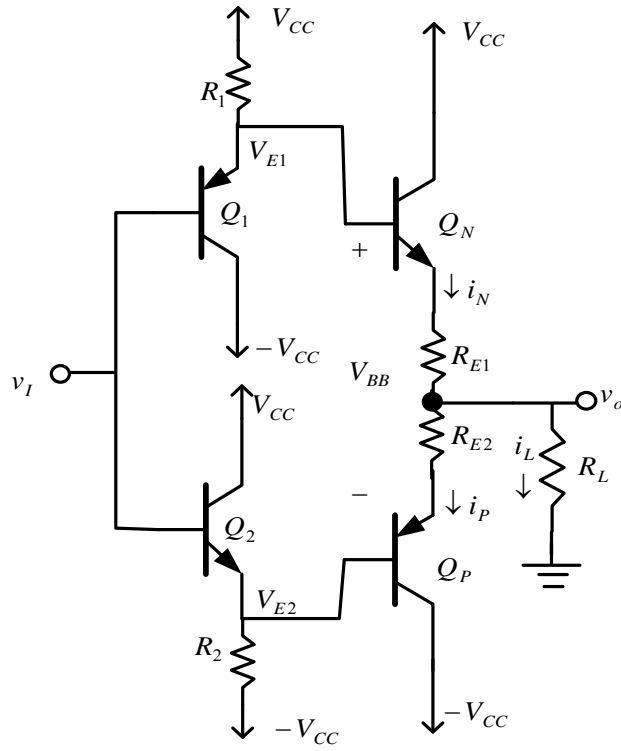


Figure 5.13: Class AB stage with  $V_{BB}$  biasing by complementary CC stages

For either of the cases, the current gain factor is  $h_{FE} = h_{FE1}h_{FE2}$ , where  $h_{FE1}$ ,  $h_{FE2}$  are the current gain factors of  $Q_1$  and  $Q_2$  respectively.

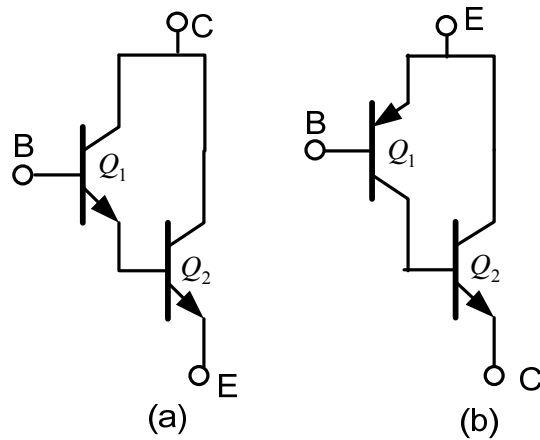


Figure 5.14: Compound transistors; (a) Darlington pair, (b) Compound PNP transistor

A class AB output stage employing the compound transistors and a  $V_{BE}$  multiplier circuit is shown in figure 5.15.

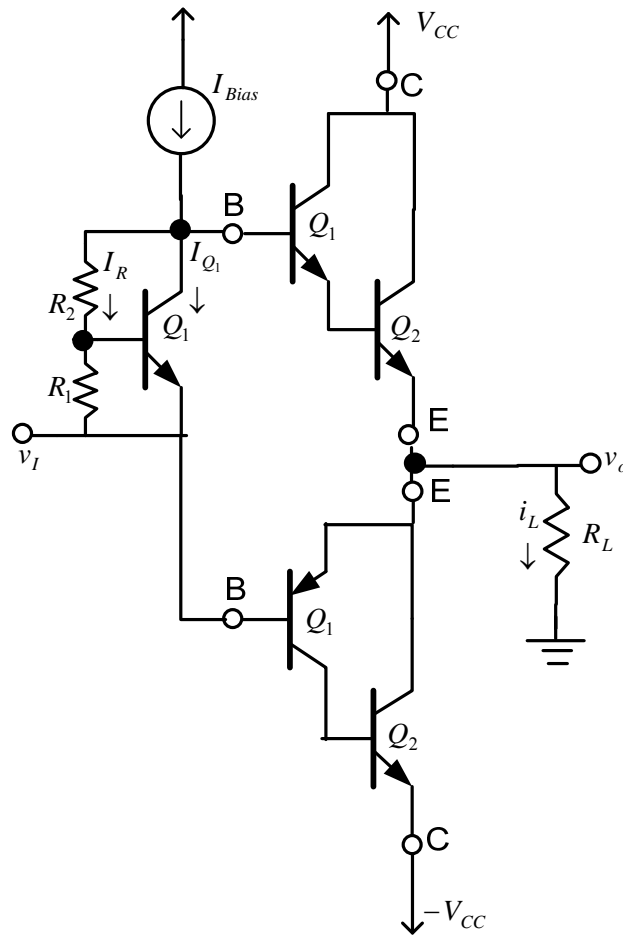


Figure 5.15 A class AB output stage with compound transistors biased by a  $V_{BE}$  multiplier circuit.

### 5.3 Short Circuit Protection in Output Power Stages

Protecting the output stage from burn out because of accidental short circuit is an important concern in high output power system. Short circuit means  $R_L \rightarrow 0$  by accident. A short circuit protection scheme for a class AB output stage is shown in Fig.5.16.



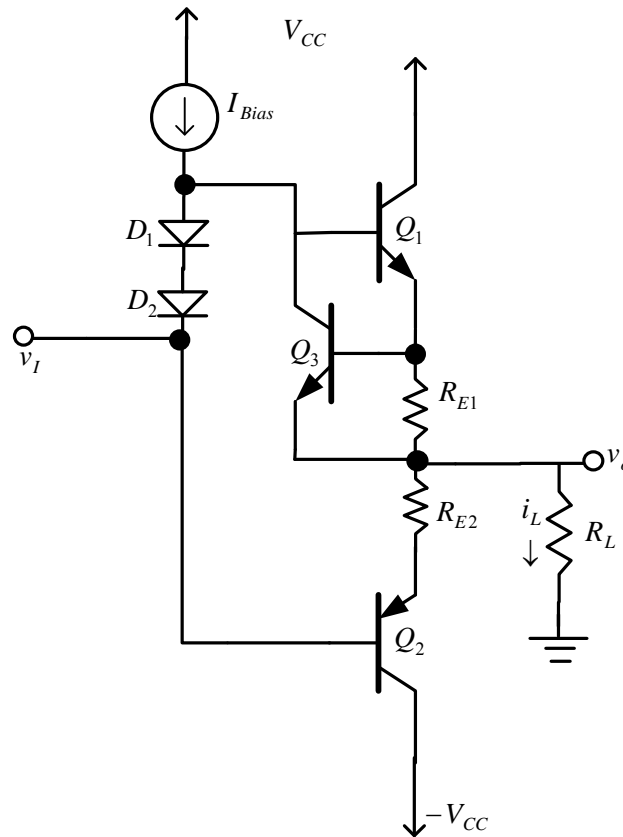


Figure 5.16: Class AB stage with short circuit protection by the transistor  $Q_3$ .

Basically any sudden surge of current in the output because of  $R_L \rightarrow 0$ , causes a drop across  $R_{E1}$  (or  $R_{E2}$ ) of such magnitude that the by-pass transistor  $Q_3$  turns ON. Then  $Q_3$  shunts away large part of the base bias drive current to  $Q_1$ . This way  $Q_1$  is saved from a burn out. Note that for accidental short circuit  $i_L > 0$ , so consideration of current in the opposite direction, i.e., protection of  $Q_2$  (the PNP) transistor does not arise. The disadvantage of the protection scheme is a slight reduction in the output voltage  $v_o$  because of series voltage drop in  $R_{E1}$ .

#### 5.4: Power BJTs

Transistors that deliver large power have to carry large amount of currents. Thus they have to be of special construction, special packaging and special mounting. Since large amount of power is dissipated in the transistor, the collector-base junction area has to be large. Such dissipation of heat increases the junction temperature. Undue rise in temperature may damage the transistor. The wafer may fuse, the thin bonding wires may melt. Transistor manufactures specify a

maximum junction temperature  $T_{jmax}$  which must not be exceeded while the device is in operation. For silicon devices this range from 150 °C to 200° C. BJTs fabricated with high power dissipation ability are called power BJTs. The power level range from few watts to hundreds of watts.

## 5.5 Thermal considerations

### 5.5.1: Thermal Resistance

As the BJT junction temperature rises, heat is generated and is dissipated in the surrounding environment. This tends to lower the junction temperature. This is analogous to flow of current through a resistance trying to lower the voltage difference between the ends of the resistance. The temperature difference may be considered as a voltage difference while the power dissipated into the medium can be considered as a current. In the steady state in which the transistor is dissipating  $P_D$  watts, the temperature rise of the junction relative to the surrounding ambience can be expressed as:  $T_j - T_A = \theta_{jA} P_D$ , where  $\theta_{jA}$  is the thermal resistance between the junction and the ambience.  $\theta_{jA}$  has the unit of °C per watt. In order that the transistor can dissipate large amount of power without raising the junction temperature above  $T_{jmax}$ , it is desirable to have as small value of  $\theta_{jA}$  as possible. What it means that  $T_j - T_A$  should be maintained constant, with  $T_j \rightarrow T_{jmax}$ , then  $\theta_{jA} P_D \rightarrow \text{constant}$ . Hence, if  $P_D$  increase,  $\theta_{jA}$  must decrease. The relationship  $T_j - T_A = \theta_{jA} P_D$  can be depicted by an equivalent electric network as shown in Fig.5.17.

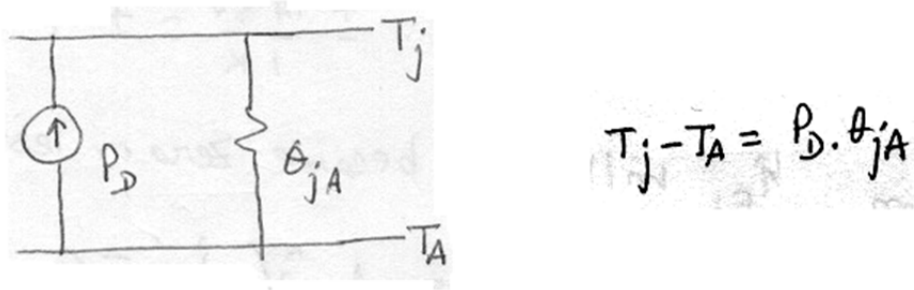


Figure 5.17: Equivalent circuit relating heat dissipation with rise of junction temperature

The transistor manufacturers usually specify  $T_{jmax}$ , the maximum power dissipation at a particular ambient temperature  $T_{AO}$  °C (usually 25° C) and the thermal resistance  $\theta_{jA}$ . These are related by

$$\theta_{jA} = \frac{T_{jmax} - T_{AO}}{P_{DO}}$$

At an ambient temperature  $T_A$  higher than  $T_{AO}$ , the maximum allowable power dissipation  $P_{Dmax}$  can be obtained from the above relation by  $P_{Dmax} = \frac{T_{jmax} - T_A}{\theta_{jA}}$ .

As  $T_A$  becomes close to  $T_{jmax}$ ,  $P_{Dmax}$  decreases. For  $T_A < T_{AO}$ , it is assumed that  $P_D$  is =  $P_{DO}$ , a steady state value. Only when  $T_A > T_{AO}$ ,  $P_D$  degrades or derates with a slope of *minus*  $\frac{1}{\theta_{jA}}$ .

Utility of the above relationships can be understood by considering the following example.

*Example 5.5.1.1:* A BJT is specified to have a maximum power dissipation  $P_{DO}$  of 2W at  $T_{Ao}=25^\circ\text{C}$ , and a maximum junction temperature  $T_{jmax}$  of  $150^\circ\text{C}$ . Find (i) the thermal resistance of the device, (ii) the maximum power that can be safely dissipated at an ambient temperature of  $50^\circ\text{C}$ .

*Solution:* (i)  $\theta_{jA} = \frac{T_{jmax} - T_{Ao}}{P_{Do}} = \frac{150 - 25}{2} = 62.5^\circ\text{C/W}$

(ii)  $P_{Dmax} = \frac{T_{jmax} - T_{Ao}}{\theta_{jA}} = \frac{150 - 50}{62.5} = 1.6\text{W}$

### 5.5.2: Transistor Case and Heat Sink

In order to improve the heat dissipation capacity of a transistor, the transistor is encapsulated in a large area case with the collector connected to the case and the case is bolted to a large metal plate called heat sink. For high power transistors these heat sinks are also made of special structure with several fins, which increases the heat dissipating surface area without undue increase in volume. See the back of the power amplifiers, of your stereo system, for example. With all these interfaces, the equivalent thermal resistance becomes sum total of the thermal resistances of the elements. Thus, one can express  $\theta_{jA}$  as  $\theta_{jA} = \theta_{jC} + \theta_{CA}$ , where  $\theta_{jC}$  is the thermal resistance between the junctions of the transistor and the transistor case (package),  $\theta_{CA}$  is the thermal resistance between the case and the ambient.  $\theta_{jC}$  can be reduced by having a large metal case for packaging the transistor.  $\theta_{CA}$  can be reducing using a *heat sink*, an option at the disposal of the amplifier and the package designer.

With a heat sink,  $\theta_{CA} = \theta_{CS} + \theta_{SA}$ . In this  $\theta_{CS}$ , is the thermal resistance between case to heat sink, and  $\theta_{SA}$ , is the heat sink to ambient thermal resistance. The overall electrical equivalent circuit can be modeled as shown in Fig.5.18. The power dissipation equation becomes:

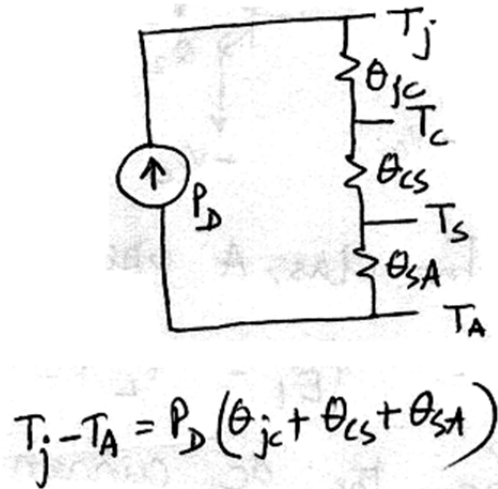
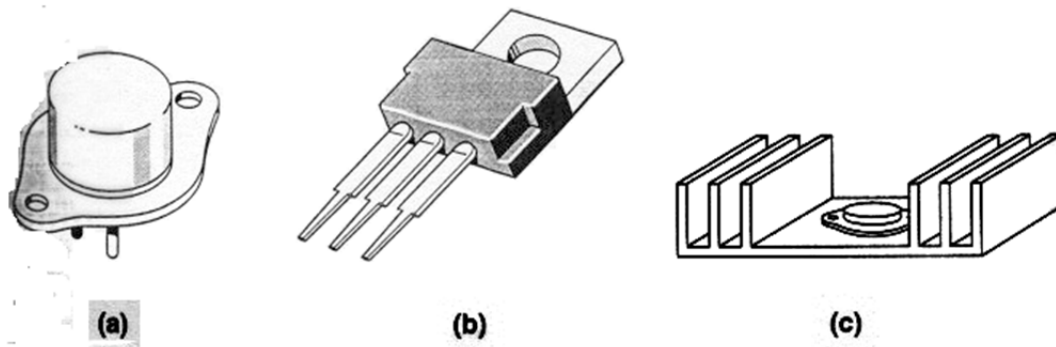
$$T_j - T_A = P_D (\theta_{jC} + \theta_{CS} + \theta_{SA}).$$


Figure 5.18: Transistor heat dissipation equivalent circuit with casing and heat sink.

It may be noted that the  $\theta$ 's in the above equation behave similar to conductances ,i.e., thermal resistances connected in parallel. Device manufacturers also supply  $\theta_{jC}$  and a derating curve of  $P_{Dmax}$  versus case temperature  $T_C$ . If the device case temperature  $T_C$  can be maintained in the range  $T_{CO} \leq T_C \leq T_{jmax}$ , the maximum safe power dissipation is obtained when  $T_j = T_{jmax}$ , with

$$P_{Dmax} = \frac{T_{jmax} - T_{CO}}{\theta_{jC}}. T_{CO} \text{ is usually taken as } 25^\circ \text{ C. Figure 5.19 depicts several packaging and}$$

heat sinking arrangements for high power transistors.



Two packaging schemes: (a) and (b) for power transistors and (c) typical heat

Figure 5.19: Packaging and heat sinking arrangements for power transistors; (a), (b) two different packaging technique, (c) typical heat sink arrangement.

#### 5.6: Large and Small signal parameters for Power BJT

1. At high currents the constant  $n$  in the exponential I-V characteristic assume a value close to 2, i.e.,  $i_C = I_S e^{v_{BE}/2V_T}$ .
2.  $\beta$  is low, typically about 50, but could be as low as 5. It must be remembered that  $\beta$  has a positive temperature coefficient.
3. At high currents  $r_\pi$  becomes very small and hence the base material resistance  $r_x$  assumes a dominant role.
4. The short circuit current gain transition frequency  $f_T$  is low (few MHz only),  $C_\mu$  becomes large (hundreds of pF) and  $C_\pi$  is even larger.
5.  $I_{CBO}$  is large (few tens of micro amps.) and doubles every  $10^\circ\text{C}$  rise in temperature.
6.  $BV_{CEO}$  is typically 50 to 100 V, but it can be as high as 500V.
7.  $I_{Cmax}$  is typically in the ampere range, but can become as high as 100A.