Laboratory Manual

Digital Electronics I
COEN 314

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IN CASE OF
EMERGENCY
REMAIN CALM

AND FOLLOW THESE INSTRUCTIONS

Fire/Evacuation

Fire:
- If you see smoke or fire activate the nearest fire alarm.

Evacuation:
- Stay calm; do not rush or panic
- Safely stop your work,
- Gather your personal belongings; coat, purse, etc...
- Close and lock your door and windows.
- Use stairs only; do not use elevators or escalators,
- Once outside, move away from the building.
- Do not re-enter the building until instructed to do so by Security.

Shelter In Place

Communication:
- Shelter-in-Place will be announced by intercom P.A. voice communication, text messaging,
- Fire alarms will not be sounded.

Procedures:
- Lock classroom, office and lab doors if possible, remain quiet and do not enter the hallway,
- Should the fire alarm sound, DO NOT evacuate the building unless:
  1. *You have first hand knowledge that there is a fire in the building,*
  2. *You are in imminent danger, or*
  3. *You have been advised by Security or Police to evacuate the building.*
- Crouch down in the areas that are out of sight from doors and windows,
- Anyone in the hallways are to seek shelter in the nearest classroom,
- Anyone outdoors on campus should immediately take cover,
- If safe you can call 514-848-(8800) for more information on the situation.

Suspicious Person/Package

Suspicious Person:
- Do not physically confront the person,
- Do not let anyone into a locked building/office,
- Call Security @ 514-848-(3717),
- Provide as much information as possible about the person and his or her direction of travel.

Suspicious Package:
- Do not touch or disturb object,
- Call Security @ 514-848-(3717),
- Notify your Supervisor.

Hazardous Materials

- If an emergency develops or if anyone is in danger, call 514-848-(3717),
- Move away from the site of the hazard to a safe location,
  Follow the instructions of Emergency
- Personnel,
- Alert others to stay clear of the area,
- Notify Emergency Personnel if you have been exposed to the hazard or have information about the release.

Medical Emergencies

- In the event of a serious or life threatening injury or illness;
- From a safe location; call Security immediately at 514-848-(3717),
- Ensure your personal security before attempting first-aid,
- Provide the victim appropriate first-aid & comforting,
- Do not give the victim anything to drink or eat.

**If the injury is the result of a fall or significant trauma: Do not move the victim unless absolutely necessary.*

Power Failure

- Remain calm and move cautiously to a lighted area,
- Do not evacuate unless asked to by Emergency Personnel,
- Do not use candles!
- For localized outages, contact Security at 514-848-(3717).

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Contents

Laboratory Rules

Considering the number of students attending the labs and in order for the lab to operate properly, the students are asked to abide by the following rules:

1. No smoking, eating, or drinking is permitted in the laboratory.
2. Overcoats, loose clothes (i.e. ties) and briefcases are not permitted in the laboratory. Shoes must hold the ankle. This means no flip flops.
3. All damaged or missing equipment and cables must be reported immediately to the demonstrator. Failure to do so will result in students being charged for damages and losses, or extra lab work can be assigned.
4. The lab bench workspace must be kept clean. Scrap paper, pencil and eraser shavings must be cleaned up and deposited in the appropriate recycling or garbage can. Disciplinary action will be taken against any student who misuses the lab, such as making marks on lab benches or on equipment, braiding patch cords, etc. Students must not be a disturbance to others in the lab.
5. Students are required to have their pre-labs completed before being admitted to the corresponding lab session (preparation and participation evaluation).
6. All data must be recorded on the laboratory sheets in ink and must be signed by the demonstrator before students leave.
7. No more than three students are allowed to occupy one laboratory workbench.
8. Any student who is more than 30 minutes late will not be permitted into the laboratory room. Furthermore, repeated tardiness will not be tolerated.
9. Demonstrators must verify all setups before any power switches are switched on.
10. Any changes even minor ones to the setup must be done when the power is off.
11. Any unusual equipment and machine operating conditions such as smoke, sparking, loud noise, or burning smell must be immediately reported to the lab demonstrator, and all power supplies should be switched off.

Overview

CD4007UB - CMOS Dual Complementary Pair Plus Inverter

Each experiment in this manual is based on `CD4007UB` - an integrated circuit with three NMOS and PMOS pairs. The datasheet for this device is included in Appendix A. As seen in the functional diagram, the first two pairs are only connected at the gate, and the third pair is setup as a CMOS inverter. The numbered terminals in this diagram correspond to the pins of the physical package whose top view is shown in Figure 2.

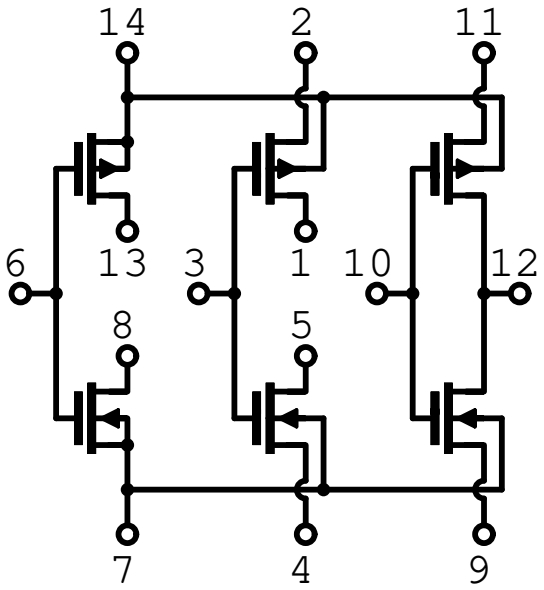


Figure 1: Functional diagram of `CD4007UB`

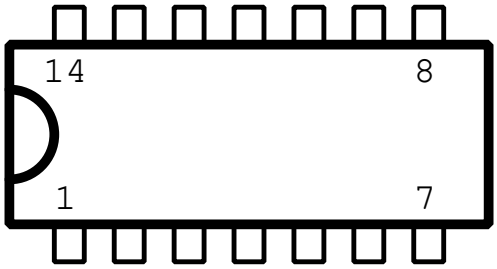
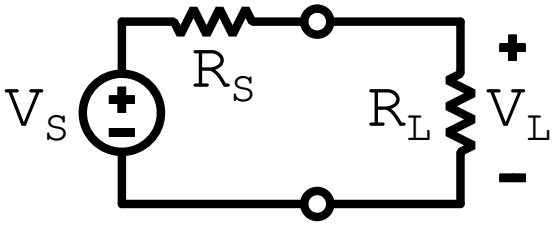


Figure 2: Dual Inline Package (DIP) with 14 pins

Probes and Channel Attenuation

When the function generator is first turned on, an output with a peak-to-peak voltage of V_{PP} appears as a signal of $2V_{PP}$ on the oscilloscope. This is because the function generator used in these experiments has a source impedance of $R_S = 50\,\Omega$ and expects a load impedance of $R_L = 50\,\Omega$, which leads to a voltage division. To compensate for this, the generator produces a waveform with a doubled swing. However, the impedances of the transistors and oscilloscope probes are much greater than $50\,\Omega$, resulting in a signal of $2V_{PP}$ appearing at the nodes of the circuits. To disable this setting, follow this sequence right after turning on the function generator:

Utility → Output Setup → High Z → Done



$$V_L = \frac{R_L}{R_S + R_L} V_S \tag{1}$$

Figure 3: Function generator driving a load

Figure 4 demonstrates the voltage divider formed between the impedance of a probe, R_P, and the input impedance of a channel connector, R_{IN}. In this laboratory, oscilloscope probes are either marked as 1X or 10X. For 1X probes, $R_P = 0\,\Omega$, and a node signal V_N is sensed directly at the oscilloscope. In this case, the voltage attenuation of the channel should be set at 1X. For 10X probes, $R_P = 9\,\mathrm{M}\Omega$, and the measured voltage is attenuated by a factor of 10. The channel attenuation should be adjusted accordingly:

CH 1/2 → Probe → Voltage → Attenuation → 1X/10X

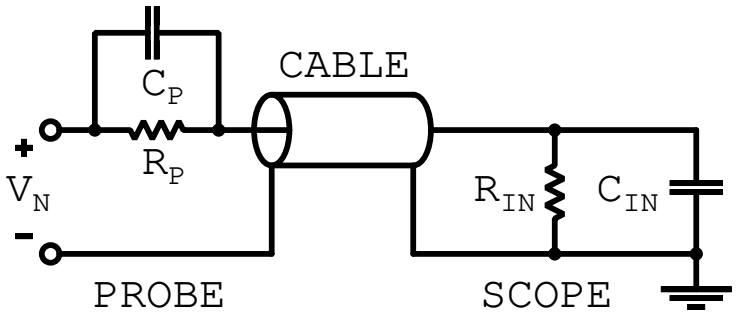


Figure 4: Oscilloscope probe and connector

Common Mistakes

In most cases, incorrect experimental results can be attributed to one or several of the following mistakes:

1. On the power supply, the black and green terminals are disconnected.
2. Power supply current limiter is too low.
3. Function generator is configured to drive $50\,\Omega$ instead of a high impedance (HighZ).
4. Function generator output is connected through a 10X oscilloscope probe.
5. Function generator voltage swing does not match the power supply.
   For example, the supply is set to $V_{DD} = 10\,\text{V}$ but the input signal toggles between $0\,\text{V}$ and $5\,\text{V}$.
6. Function generator toggles between $\pm V_{DD}$ instead of $0\,\text{V}$ and V_{DD}.
7. Ammeter is connected in parallel instead of in series.
8. Oscilloscope probe and channel attenuation do not match.
9. Breadboard connections are incorrect.
10. `CD4007` chip is faulty and needs to be replaced.

Experiment #1
CMOS Pass Transistors

Introduction

Pass Transistor Logic (PTL) offers a simple way to implement electrical switches for transferring voltage signals. Both NMOS and PMOS devices can be used for this purpose with each having its own limitations. The horizontal configurations shown in Figure 5 can help reduce the number of devices used to implement a digital function. This is illustrated with the 2-to-1 multiplexers in Figure 6. Although the smaller area is a valuable advantage, PTL devices have a significant drawback, which is to be demonstrated in this experiment.

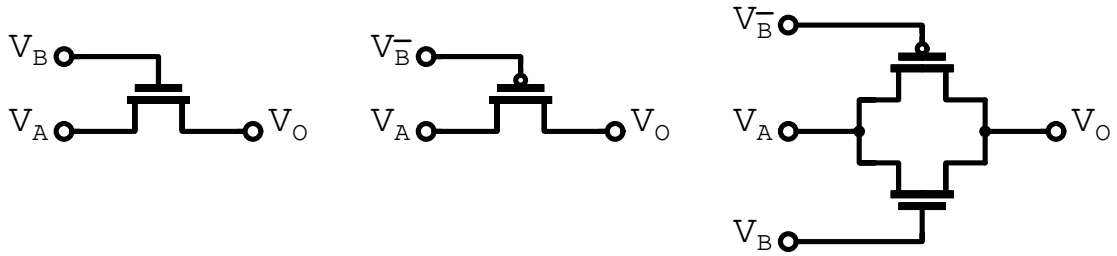
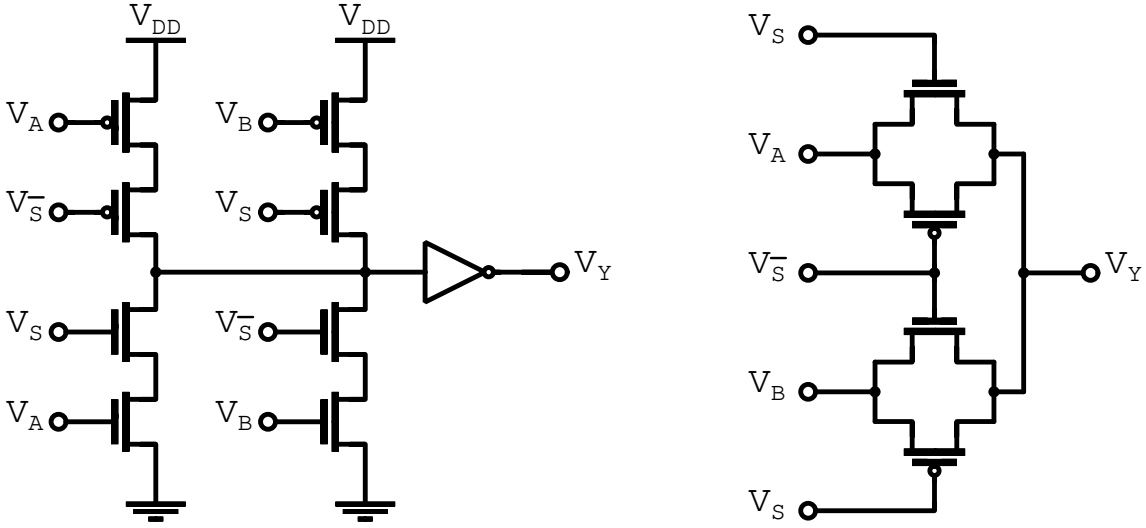


Figure 5: NMOS, PMOS and CMOS switch implementations



(a) Standard implementation

(b) Pass transistor implementation

Figure 6: Multiplexer circuits

Note that the source and drain terminals of a MOSFET are determined by their voltages and not structure. For an NMOS, the source terminal is always the one with the lower voltage;

for a PMOS, the source terminal is the one with the higher voltage. As an example, referring to the NMOS in Figure 5, if $V_A < V_O$, then V_A and V_O are the source and drain terminals, respectively.

Consider the NMOS PTL device in Figure 5. When the voltage applied to the gate is $V_B = V_{DD}$, a high logic voltage applied to the input V_A is transmitted to the output V_O. However, the NMOS turns off when $V_{GS} < V_{tn}$. Since the source terminal is always at a lower voltage, the output node stops charging when it reaches the value $V_O = V_{DD} - V_{tn}$, and cannot rise all the way to V_{DD}. This makes it a weak logic '1'. This issue does not occur for $V_A = 0\,\mathrm{V}$, rendering it a strong logic '0'.

For the case of the PMOS PTL device, the opposite is true. With a complementary (CMOS) configuration, both logic values are strong. Table 1 offers a summary.

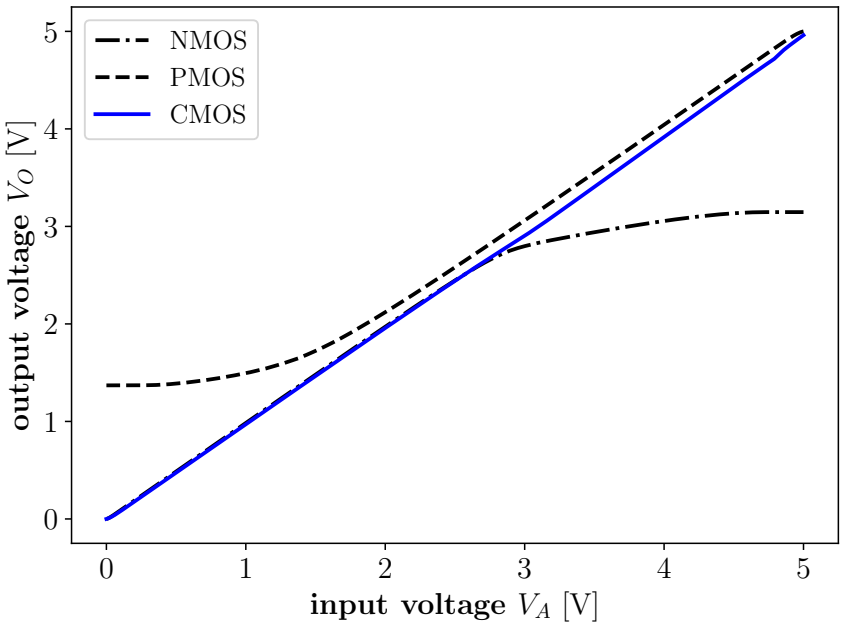


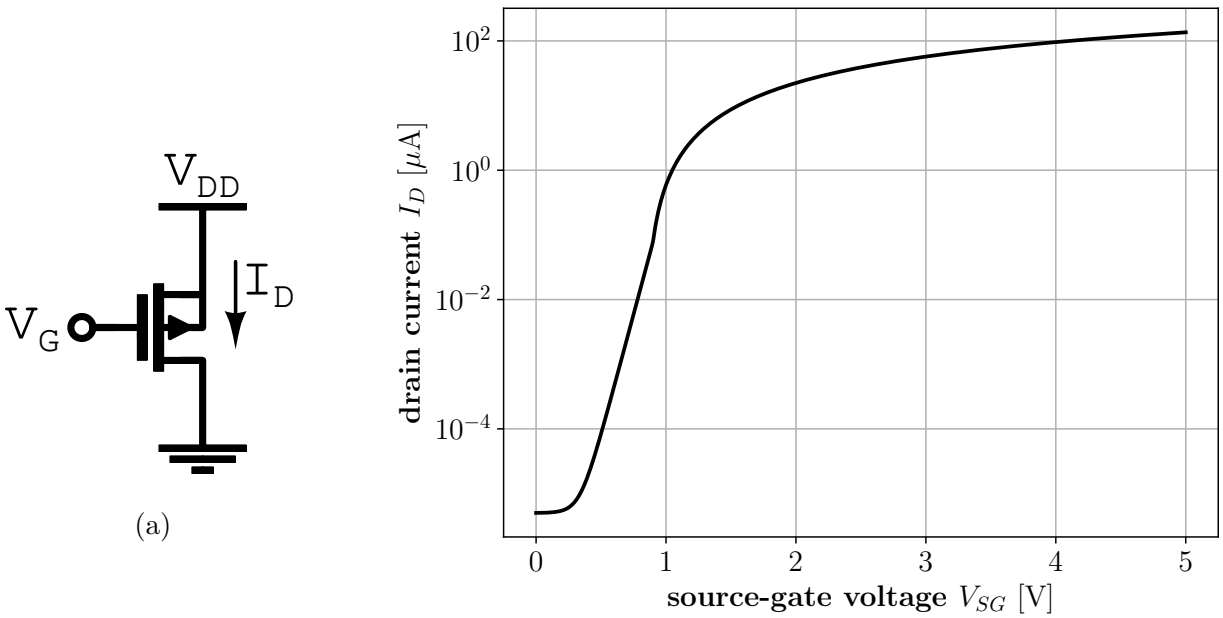
Figure 7: PTL voltage transfer characteristics

Table 1: Output quality of PTL devices

Implementation	Logic Input	Logic Output
NMOS	0	Strong 0
	1	**Weak** 1
PMOS	0	**Weak** 0
	1	Strong 1
CMOS	0	Strong 0
	1	Strong 1

Prelab

1. In Figure 5, the NMOS inputs are $V_A = V_B = 5\,\text{V}$, the threshold voltage is $V_{tn} = 2.8\,\text{V}$, and the initial output voltage is $V_O = 0\,\text{V}$. Provide an estimate for the output voltage.
2. In Figure 5, the PMOS inputs are $V_A = V_B = 0\,\text{V}$, the threshold voltage is $V_{tp} = 3.2\,\text{V}$, and the initial output voltage is $V_O = 5\,\text{V}$. Provide an estimate for the output voltage.
3. Figure 8b shows the drain current of a PMOS transistor as a function of the source-gate voltage. Note that the vertical axis is on a logarithmic scale. Assume that the threshold voltage is $V_{tp} = 1.0\,\text{V}$.
    a. Compare the theoretical and simulated values of current in the cut-off region.
    b. Explain the difference in values.
    c. Explain what would happen if the width of the transistor was doubled.
4. Figures 9 and 10 indicate the connections that need to be made with `CD4007UB`. Write the pin numbers for parts 3 and 4 of this experiment.



(a)

(b)

Figure 8: Drain current of a PMOS transistor

Note: The simulation results were not obtained using datasheet parameters, and experimental results are expected to have different values.

Procedure

Prior to the start of the experimental tasks, take note of the following:

1. To implement this experiment, you are given an IC package that contains transistor pairs. Pay attention to the connections to the bulk in the schematic.
2. When connecting the power supply, make sure that the negative terminal is connected to the common ground (i.e. the black and green terminals).
3. For this experiment, never set the power supply voltage above 10 V.
4. Monitor the current on the power supply indicator every time you turn it on. If you see the current needle above 0.1 A to 0.2 A, turn off the power supply IMMEDIATELY.
5. If the IC gets hot, turn off the power supply IMMEDIATELY.

Part 1 - NMOS Pass Transistor

1. Build the circuit shown in Figure 9. The numbers on the NMOS terminals correspond to the pins of the `CD4007` IC.
2. Set the power supply to $V_{DD} = 5\,\text{V}$.
3. Turn on the function generator, and press the following:
   Utility → **Output Setup** → **High Z** → **Done**
4. Connect the output of the function generator to the input A. Configure it to output a ramp signal with a frequency of 100 kHz, a high level equal to V_{DD}, a low level of 0 V, and a symmetry of 100%.
   - ◇ Parameters **Ampl** and **Offset** are first highlighted when the function generator is turned on.
   - ◇ Parameters **HiLevel** and **LoLevel** can be selected by pressing on either one.
5. Connect the input B to V_{DD}.
6. Use oscilloscope cursors to measure the minimum and maximum output voltage values.
7. Collect measurements in Table 2, and save the input and output waveforms.
8. Populate the remainder of Table 2. Save the oscilloscope waveforms for each row.

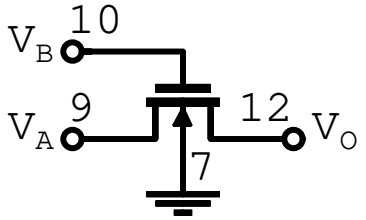


Figure 9: NMOS pass transistor gate

Table 2: Part 1 - Results

Supply Voltage	**Input Frequency**	**Output**	
V_{DD}	f_0	Min V_O	Max V_O
5 V	1 kHz		
	100 kHz		
10 V	1 kHz		
	100 kHz		

Note: Measure the voltages. Do not just write '0' or '1'.

Part 2 - PMOS Pass Transistor

1. Build the circuit shown in Figure 10. Make sure that the breadboard connections from the previous task do not interfere with the present task.
2. Set the power supply to $V_{DD} = 5$ V.
3. Turn on the function generator, and press the following:
   Utility → **Output Setup** → **High Z** → **Done**
4. Connect the output of the function generator to the input A. Configure it to output a ramp signal with a frequency of 100 kHz, a high level equal to V_{DD}, a low level of 0 V, and a symmetry of 100%.
5. Connect the input B to 0 V.
6. Use oscilloscope cursors to measure the minimum and maximum output voltage values.
7. Collect measurements in Table 3, and save the input and output waveforms.
8. Populate the remainder of Table 3. Save the oscilloscope waveforms for each row.

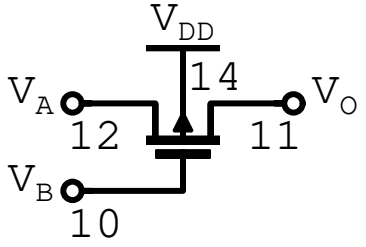


Figure 10: PMOS pass transistor gate

Table 3: Part 2 - Results

Supply Voltage	**Input Frequency**	**Output**	
V_{DD}	f_0	Min V_O	Max V_O
5 V	1 kHz		
	100 kHz		
10 V	1 kHz		
	100 kHz		

Note: Measure the voltages. Do not just write '0' or '1'.

Part 3 - Impact of a Poor '1'

The circuit in Figure 11 consists of an NMOS pass transistor gate connected to an inverter. The last column in Table 4 corresponds to the current drawn from the power supply. To read this measurement, connect an ammeter in series with the power supply and the breadboard.

1. Build the circuit.
2. Record your measurements in Table 4. When changing the connections of the circuit, turn off the power supply.

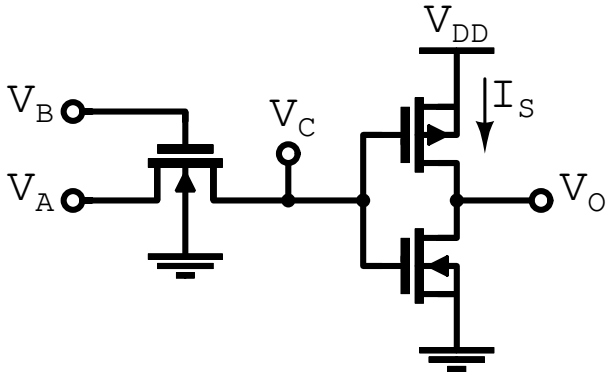


Figure 11: NMOS pass transistor connected to an inverter

Table 4: Part 3 - Results

Supply Voltage	**Inputs**		**Outputs**		**Supply Current**
V_{DD}	V_A	V_B	V_C	V_O	I_S
5 V	'0'	'1'			
	'1'	'1'			
10 V	'0'	'1'			
	'1'	'1'			

Note: Measure the voltages. Do not just write '0' or '1'.

Part 4 - CMOS Transmission Gate

The circuit in Figure 12 consists of a CMOS transmission gate connected to an inverter.

1. Build the circuit.
2. Record your measurements in Table 5. When changing the connections of the circuit, turn off the power supply.
   Note: If $V_B = V_{DD}$, then $V_{\overline{B}} = 0\,\text{V}$, and vice versa.

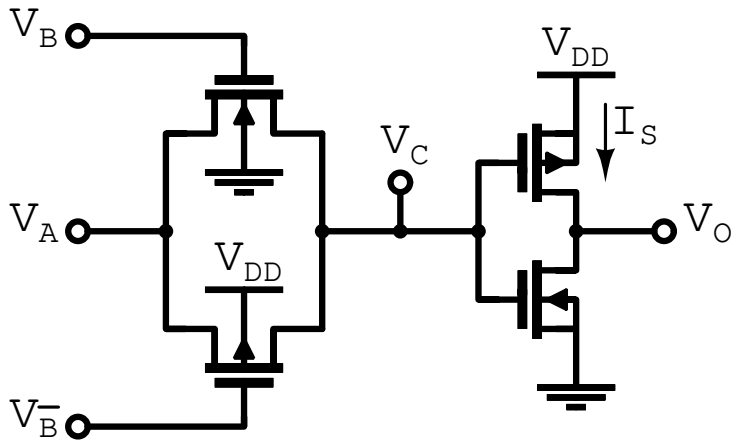


Figure 12: CMOS transmission gate connected to an inverter

Table 5: Part 4 - Results

Supply Voltage	**Inputs**		**Outputs**		**Supply Current**
V_{DD}	V_A	V_B	V_C	V_O	I_S
5 V	'0'	'1'			
	'1'	'1'			
10 V	'0'	'1'			
	'1'	'1'			

Note: Measure the voltages. Do not just write '0' or '1'.

Results & Discussion

Show the saved waveforms and answer the questions below.

1. From your measurements, how do the voltage levels of the weak '0' and the weak '1' change as the supply voltage increases? Explain.
2. In part 1, what happens when the input voltage V_B is set to logic '0'?
3. In parts 1 and 2, explain the differences in minimum and maximum values of the output voltage for different input frequencies.
4. In part 3, why is the supply current much larger when $V_A = V_{DD}$ as opposed to when $V_A = 0\,\text{V}$? How does this compare to the results from part 4? Explain.
5. In part 3, what are the operating modes (i.e. cut-off, triode, saturation) of the inverter transistors? Refer to the measurements that correspond to $V_{DD} = 5\,\text{V}$ in Table 4. Provide answers for $V_A = 0\,\text{V}$ and $V_A = 5\,\text{V}$.
6. Compare the results in Tables 4 and 5. Explain why the supply current is much smaller in part 4.

Experiment #2
CMOS Inverter

Introduction

The function of an inverter is to negate the logical value of the input (i.e. $0 \rightarrow 1$ and $1 \rightarrow 0$). In digital electronics, the logic values '0' and '1' correspond to low ($\sim 0\,\mathrm{V}$) and high ($\sim V_{DD}$) voltages, respectively. Figure 13 provides a basic implementation of this device.

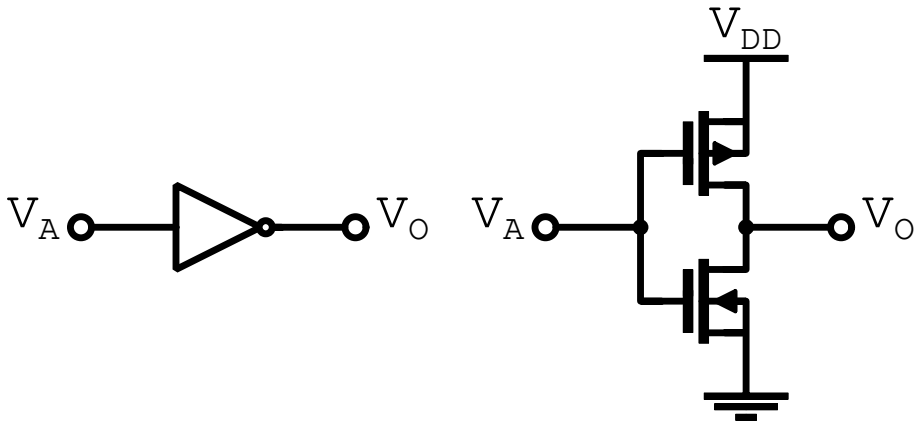


Figure 13: Inverter symbol and circuit schematic

The objective of this experiment is to study the static and dynamic characteristics of the CMOS inverter. This is to be achieved using the setup shown in Figure 14. It includes two voltage sources, two oscilloscope probes, and an ammeter **A**.

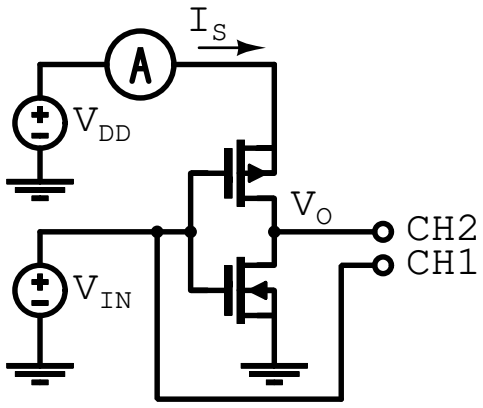
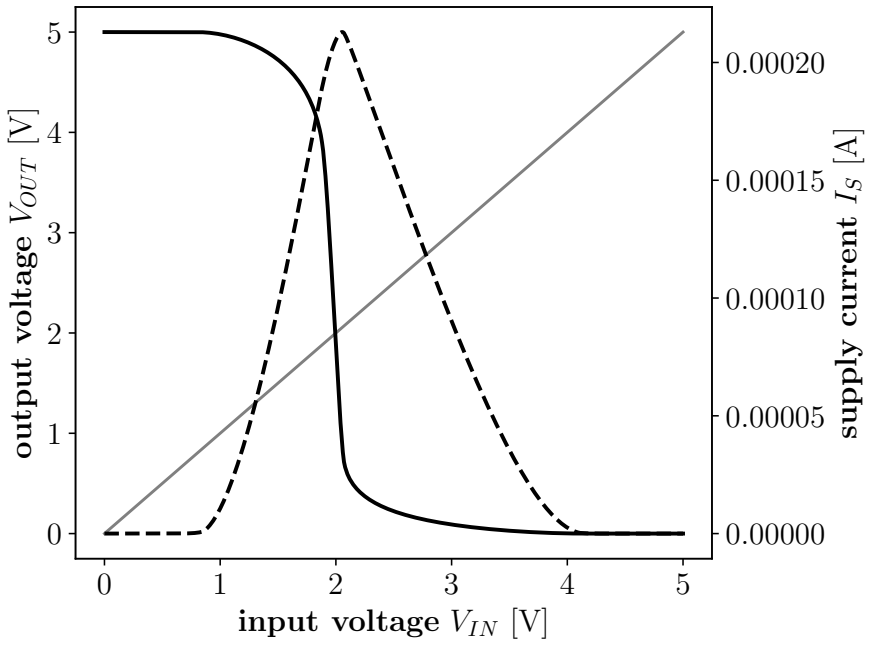


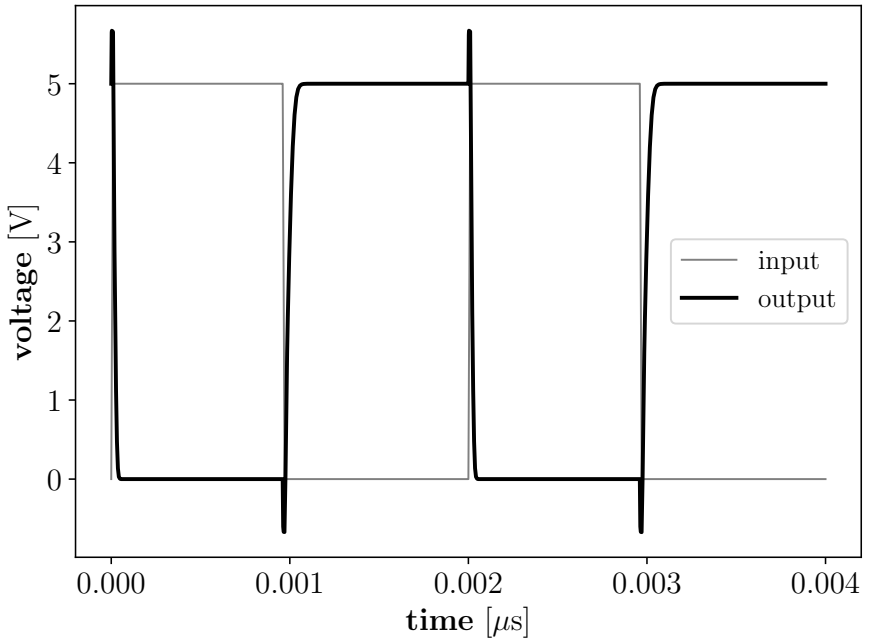
Figure 14: Experiment setup

Figure 15a shows the output voltage and the power supply current as functions of the input voltage, V_{IN}. The current drawn from the power supply is almost $0\,\mathrm{A}$ for voltages that

correspond to logic values '0' and '1'. As a result, static power dissipation is minimal. In the vicinity of the inverter threshold voltage, V_{TH}, appreciable current is drawn as the inverter switches between logic values. Figures 15a and 15b are to be reproduced experimentally.



(a) Transfer characteristics



(b) Transient operation

Figure 15: Static and dynamic characteristics

Prelab

1. One ampere corresponds to one coulomb per second ($1\,\text{A} = 1\,\text{C/s}$), and an electron charge is $q_e = 1.60217646 \times 10^{-19}\,\text{C}$. What electron flow (in terms of electrons per second) corresponds to a current of 28 pA?
2. Populate Table 7 by referring to Figure 7 of the `CD4007UB` datasheet in the appendix.
3. When the input of the inverter is $V_{IN} = 0\,\text{V}$, the PMOS is in triode and the NMOS is in cut-off. The opposite is true for $V_{IN} = V_{DD}$. Complete Table 6.
4. Why are noise margins important characteristics of a gate?
5. Consider a circuit where the output of a CMOS inverter is connected to N digital circuits, each of which have an input capacitance. What happens to the speed of the inverter as the number N is increased? Write the definition of 'fan-out'.
6. If the NMOS and PMOS devices of the inverter are sized equally, which is expected to be shorter: the rise time or the fall time? Explain.

Table 6: Regions of Operation

Regions	I	II	III	IV	V
PMOS	Triode				Cut-off
NMOS	Cut-off				Triode

Table 7: Inverter Characteristics

	$V_{DD} = 5\,\text{V}$	$V_{DD} = 10\,\text{V}$
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
V_{TH}		
NM_L		
NM_H		

Procedure

Part 1 - Static Characteristics

1. Connect the circuit shown in Figure 14. Make sure that the bulks, voltage supply, and voltage ground are properly connected.
2. Connect the negative terminals of the power supplies to common ground (i. e. black and green terminals).
3. Set the power supply to $V_{DD} = 5\,\text{V}$. You can verify this value using the voltmeter or the oscilloscope.
4. Vary the input voltage from $V_{IN} = 0\,\text{V}$ to $V_{IN} = V_{DD}$, and record the output voltage and supply current in Table 8.
   Note: Collect more samples where the output changes rapidly (i.e. the center of the curve as seen in Figure 15a).
5. Change the power supply output to $V_{DD} = 10\,\text{V}$ and collect a new set of measurements.

Part 2 - Dynamic Characteristics

1. Turn on the function generator, and press the following:
   Utility → **Output Setup** → **High Z** → **Done**
2. Connect the output of the function generator to the input of the inverter. Produce a square wave with a frequency of 100 kHz and a voltage swing between 0 V and V_{DD}.
3. Display both input and output on the oscilloscope, and save the waveforms. Populate the upper part of Table 9.

   - ◇ For the rise and fall times, t_R & t_F, use the **Measure** function.
   - ◇ For the propagation delays, t_{PLH} & t_{PHL}, use the **Cursor** function.

   To quickly find the rising or falling edge of a waveform, use the oscilloscope's trigger function:

   i To the right of the oscilloscope panel, under **Trigger**, press **Menu**.

   ii For the settings that appear on the display, set

   - ◇ **Type** → **Edge**
   - ◇ **Source** → **Ch2**
   - ◇ **Slope** → **Rising** or **Falling**

   iii Set the **Trigger Level** knob to approximately $2\,\text{V} \sim 3\,\text{V}$.

4. Connect a capacitor of $C_L = 100\,\text{pF}$ between the inverter output and ground, and save the waveforms. Populate the lower part of Table 9.
   Note: The capacitor is used to simulate fan-out.
5. Set the frequency of the function generator to 2.5 MHz and save the waveforms.

Table 8: Part 1 - Results

$V_{DD} = 5\,\text{V}$			$V_{DD} = 10\,\text{V}$		
V_{IN}	V_{OUT}	I_S	V_{IN}	V_{OUT}	I_S

Note: Do not dismantle the circuit.

Table 9: Part 2 - Results

	$V_{DD} = 5\,\text{V}$		$V_{DD} = 10\,\text{V}$	
Without Capacitive Load	t_R		t_R	
	t_F		t_F	
	t_{PLH}		t_{PLH}	
	t_{PHL}		t_{PHL}	
With Capacitive Load	t_R		t_R	
	t_F		t_F	
	t_{PLH}		t_{PLH}	
	t_{PHL}		t_{PHL}	

Results & Discussion

Complete the following:

1. Plot the data obtained for the two values of V_{DD}.
2. Populate Table 10. The errors are to be calculated using the values from Table 7.

Table 10: Part 1 - Summary

	$V_{DD} = 5\,\text{V}$		$V_{DD} = 10\,\text{V}$	
	Measured	**Error** [%]	**Measured**	**Error** [%]
V_{OH}				
V_{OL}				
V_{IH}				
V_{IL}				
V_{TH}				
NM_L				
NM_H				

Answer the following questions:

1. What causes the inverter to have non-zero current when the input voltage is either 0 V or V_{DD}?
2. Explain why the results in Table 10 differ from those in Table 7.
3. For both supply voltages, what are the largest power consumption values?
4. How does an increase in the supply voltage V_{DD} affect the rise and fall times, and the propagation delays? Explain.
5. In a practical context, name one disadvantage of increasing the power consumption of a circuit.
6. How does the addition of the load capacitor affect the rise and fall times, and the propagation delays?
7. Assuming that the input capacitance of a CMOS gate is $C_{IN} = 5\,\text{pF}$, what is the equivalent fan-out that was simulated with the load capacitance $C_L = 100\,\text{pF}$?
8. What happens to the inverter output when the input frequency is increased to 2.5 MHz? Elaborate.

Experiment #3
CMOS NAND Gate

Introduction

The CMOS inverter studied in the previous experiment corresponds to the simplest logical operation. More complex operations require gates with multiple inputs. Figure 16 presents a 3-input CMOS NAND gate. The objective of this experiment is to study the static and dynamic characteristics of this circuit.

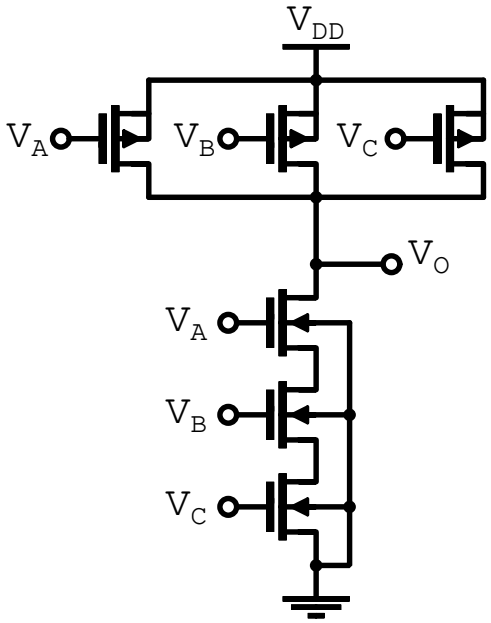
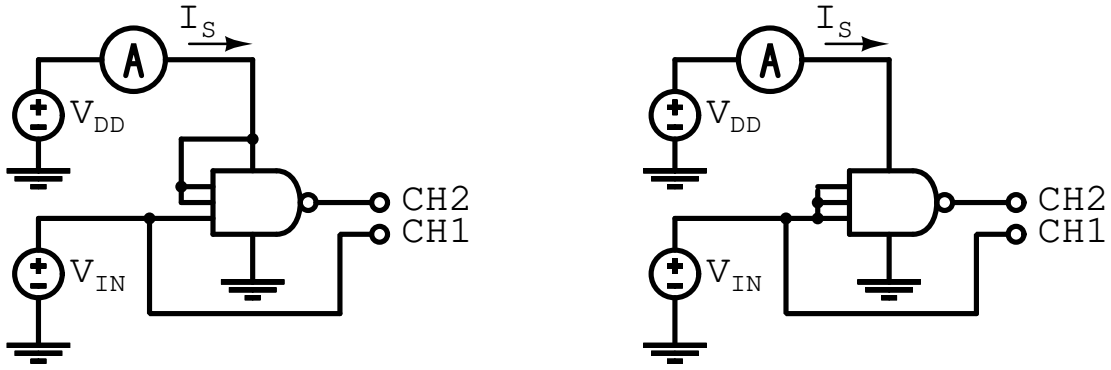


Figure 16: NAND gate circuit schematic



(a) Configuration for $V_{DD} = 5\,\mathrm{V}$ (b) Configuration for $V_{DD} = 10\,\mathrm{V}$

Figure 17: Experiment setup for part 1

Prelab

1. Draw / write the pin connections that need to be made on the `CD4007` IC in order to implement the circuit in Figure 16.
2. Fill-in the truth table of the NAND gate.
3. Provide the resulting logic function when
   a. inputs B and C are fixed at logic '1';
   b. all inputs are connected together.
4. Given that all NMOS and PMOS devices are sized equally (i.e. $(W/L)_N = (W/L)_P$)
   a. provide the sizes of the equivalent NMOS and PMOS transistors for the circuits in Figures 17a and 17b;
   b. compare the two circuits in terms of their threshold voltages, and their rise and fall times.
5. Suppose that all three inputs of the NAND gate are '1', and that the output is at '0'.
   a. How many input combinations lead to a transition of '0' $\rightarrow$ '1'?
   b. Make a comment regarding the corresponding rise times. Which combinations have the largest rise time, and which have the smallest?
   c. For this particular circuit, can a similar comment be made regarding the fall time?

Table 11: NAND gate truth table

A	B	C	O

Procedure

Part 1 - Static Characteristics

1. Connect the circuit shown in Figure 16.
2. Connect inputs B and C to V_{DD} (logic '1').
3. Connect the negative terminals of the power supplies to common ground (i. e. black and green terminals).
4. Set the power supply to $V_{DD} = 5\,\text{V}$. You can verify this value using the voltmeter or the oscilloscope.
5. Vary the voltage of input A from $V_{IN} = 0\,\text{V}$ to $V_{IN} = V_{DD}$, and record the output voltage and supply current in Table 12.
   Note: Collect more samples where the output changes rapidly.
6. Connect inputs A, B and C to V_{IN}.
7. Change the power supply output to $V_{DD} = 10\,\text{V}$, and collect a new set of measurements.

Part 2 - Dynamic Characteristics

1. Connect inputs B and C to logic '1'.
2. Turn on the function generator, and press the following:
   Utility → **Output Setup** → **High Z** → **Done**
3. Connect the output of the function generator to input A. Produce a square wave with a frequency of 100 kHz and a voltage swing between 0 V and V_{DD}.
4. Display both input and output on the oscilloscope, and save the waveforms. Populate the upper part of Table 13.

   - ◇ For the rise and fall times, t_R & t_F, use the **Measure** function.
   - ◇ For the propagation delays, t_{PLH} & t_{PHL}, use the **Cursor** function.

   Refer to the previous experiment for the oscilloscope **Trigger** function.
5. Connect a 100 pF capacitor between the output and ground, and save the waveforms. Populate the lower part of Table 13.

Table 12: Part 1 - Results

$V_{DD} = 5\,\text{V}$			$V_{DD} = 10\,\text{V}$		
V_{IN}	V_{OUT}	I_S	V_{IN}	V_{OUT}	I_S

Note: Do not dismantle the circuit.

Table 13: Part 2 - Results

	$V_{DD} = 5\,\text{V}$		$V_{DD} = 10\,\text{V}$	
Without Capacitive Load	t_R		t_R	
	t_F		t_F	
	t_{PLH}		t_{PLH}	
	t_{PHL}		t_{PHL}	
With Capacitive Load	t_R		t_R	
	t_F		t_F	
	t_{PLH}		t_{PLH}	
	t_{PHL}		t_{PHL}	

Results & Discussion

Complete the following:

1. Plot the data obtained for the two values of V_{DD}.
2. Populate Table 14.

Table 14: Part 1 - Summary

	$V_{DD} = 5\,\text{V}$	$V_{DD} = 10\,\text{V}$
V_{OH}		
V_{OL}		
V_{IH}		
V_{IL}		
V_{TH}		
NM_L		
NM_H		

Answer the following questions:

1. For the case with $V_{DD} = 10\,\text{V}$, compare the noise margins obtained during this experiment with those of the previous experiment. Justify the differences.
2. In Table 9 of Experiment #2, the rise time is greater than the fall time. Compare this with the results recorded in Table 13. Explain the differences if there are any.
3. In Experiment #2, the midpoint threshold voltage of the inverter is $V_{TH} \approx 0.4V_{DD}$. Compare this value with the results recorded in Table 14.

Experiment #4
Clocked SR Latch

Introduction

The SR latch is the simplest digital circuit with memory. As shown in Figure 18, it consists of two inverters in feedback, and three NMOS devices for the set, reset, and enable signals. Two such latches comprise a flip-flop where the enable pins are connected to two opposite clock signals.

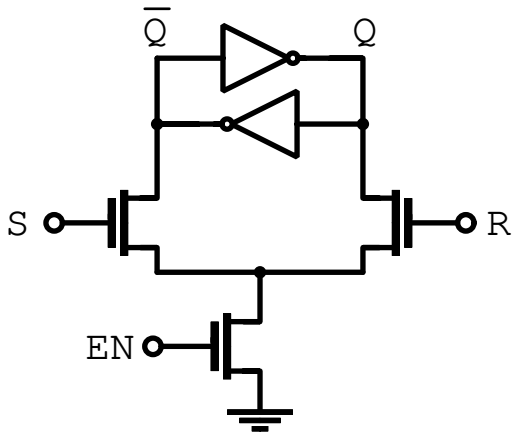
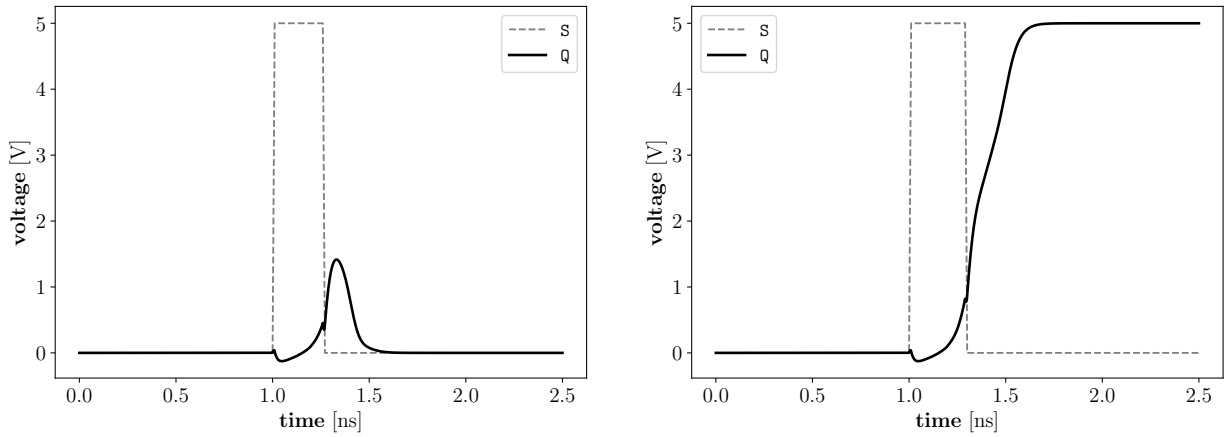


Figure 18: SR latch circuit

Figures 19a and 19b show how the duration of an input signal needs to be sufficiently long to toggle the CMOS latch. The objective of this experiment is to reproduce these figures.



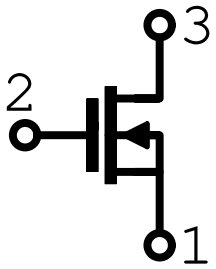
(a) Input pulse duration is too short

(b) Input pulse duration is sufficient

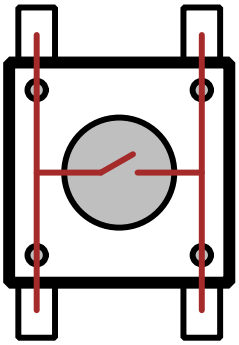
Figure 19: Programming of a CMOS latch

Prelab

1. Draw / write the pin connections that need to be made in order to implement the circuit in Figure 18. For the inverters and the `EN` transistor, use the `CD4007` IC; and, for the `S` and `R` devices, use the `VN2222` discrete MOSFETs whose pinout is given in Figure 20a.
2. Explain the purpose of the resistors added under the push buttons in Figure 21.
3. Can the `S`, `R`, and `EN` signals be applied through PMOS transistors instead? Are there any advantages or disadvantages?
4. How can an edge-triggered flip-flop be implemented using the circuit in Figure 18? Provide a high-level diagram.



(a) VN2222 (source and bulk are tied)



(b) Push button

Figure 20: Additional pinouts

Procedure

Prior to the start of the experiment, take note of the following:

1. In Figure 20a, the pins read from left to right with the flat face of the package being the front.
2. In Figure 20b, the red lines indicate the internal connections.

Part 1

1. Connect the circuit shown in Figure 21. Make sure that the bulks, voltage supply, and voltage ground are properly connected. Use resistors of $R = 1\,\text{k}\Omega$.
2. Set the power supply to $V_{DD} = 5\,\text{V}$.
3. Connect the enable pin to V_{DD}.

4. Connect CH1 of the oscilloscope to the input S, and CH2 to the output Q.
5. Verify that the circuit is functional by using the push buttons to set and reset the latch.
6. Use the trigger function of the oscilloscope to capture a low-to-high transition in the signal Q.
   - i Reset the latch so that the output Q starts at 0 V.
   - ii To the right of the oscilloscope panel, under **Trigger**, press **Menu**.
   - iii For the settings that appear on the display, set
     - ◇ **Type** → **Edge**
     - ◇ **Source** → **Ch1**
     - ◇ **Slope** → **Rising**
   - iv Set the **Trigger Level** knob to approximately 2 V ∼ 3 V.
   - v To the top right of the oscilloscope panel, press **Single**
   - vi On the breadboard, press the set button.
   - vii If done correctly, a single frame should be displayed.
   - viii If this attempt needs to be repeated, reset the latch, and press **Run / Stop** and **Single**.
7. Use cursors to measure the delay from input to output. Save the waveforms.
8. Move the probe for CH1 to the input R, and capture a high-to-low transition in the output Q.
9. Use cursors to measure the delay from input to output. Save the waveforms.
10. Connect the enable pin to 0 V. Verify that the pushbuttons have no effect on the latch output.
11. Move the probe for CH1 back to input S, and connect the enable pin back to V_{DD}.

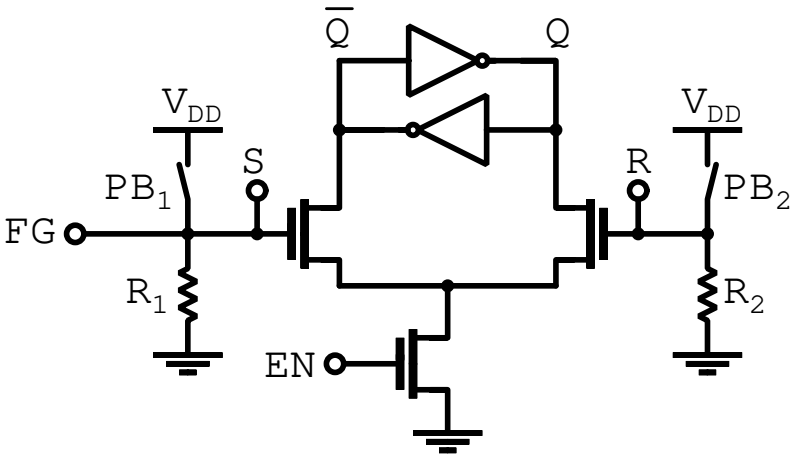


Figure 21: Experimental setup

Part 2

1. Turn on the function generator, and press the following:
   Utility → **Output Setup** → **High Z** → **Done**
2. Configure the function generator to output a **pulse** signal with a frequency of 100 kHz and a pulse width of 20 ns. Adjust the low and high levels to 0 V and 3.3 V, respectively. Connect it to the set signal.
3. Capture a low-to-high transition of signal Q with the following procedure:

   i Under **Trigger**, press **Menu**.

   ii For the settings that appear on the display, set

   - ◇ **Type** → **Edge**
   - ◇ **Source** → **Ch2**
   - ◇ **Slope** → **Rising**

   iii Set the **Trigger Level** knob to ~ 4 V.

   iv On the breadboard, press the reset button.

   v Make sure that the function generator pulse is not long enough to set the latch.

   vi To the top right of the oscilloscope panel, press **Single**

   vii On the function generator, slowly increment the pulse width until the latch is set.
4. Save two waveforms: one where the input pulse is slightly too narrow to toggle the latch, and another where it is sufficiently long. These waveforms should resemble the Figures 19a and 19b.
5. For the narrow input pulse, measure the maximum value of the output voltage.

Results & Discussion

1. Show and describe the saved waveforms.
2. Answer the questions below.

1. In Part 1, report the values of the input-to-output delays. Explain the difference.
2. In Part 2, what happens to the output signal if the input pulse is too narrow to make a full transition. Relate this to the threshold voltage of a CMOS inverter.
3. In Part 2, the magnitude of the voltage pulse is set to 3.3 V. How would your results differ if the magnitude was (a) increased or (b) decreased?
4. In Figure 18, the two inverters in feedback have three equilibrium points: $V_Q = 0$ V, $V_Q = V_{DD}$, and $V_Q = V_{TH}$, where V_{TH} is the inverter threshold. Why is this configuration referred to as a bistable circuit?

Appendices

A Datasheet for CD4007UBMS

CD4007UBMS

November 1994

CMOS Dual Complementary Pair Plus Inverter

Features

- **High-Voltage Type (20V Rating)**
- **Standardized Symmetrical Output Characteristics**
- **Medium Speed Operation**
  - **tPHL, tPLH = 30 ns (typ) at 10V**
- **100% Tested for Maximum Quiescent Current at 20V**
- **Meets All Requirements of JEDEC Tentative Standards No. 13B, "Standard Specifications for Description of "B" Series CMOS Devices"**
- **Maximum Input Current of 1μA at 18V Over Full Package-Temperature Range; 100nA at 18V and +25°C**

Applications

- **Extremely High-Input Impedance Amplifiers**
- **Shapers**
- **Inverters**
- **Threshold Detector**
- **Linear Amplifiers**
- **Crystal Oscillators**

Description

CD4007BMS types are comprised of three n-channel and three p-channel enhancement-type MOS transistors. The transistor elements are accessible through the package terminals to provide a convenient means for constructing the various typical circuits as shown in Figure 2.

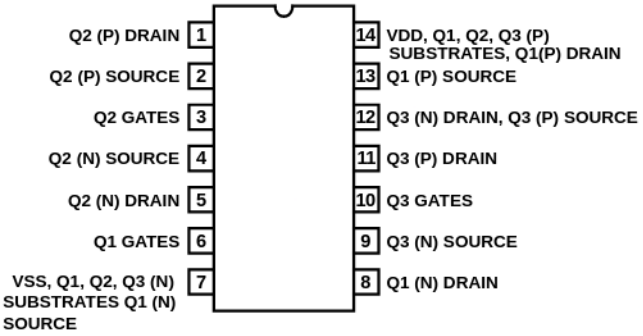
More complex functions are possible using multiple packages. Numbers shown in parentheses indicate terminals that are connected together to form the various configurations listed.

The CD4007BMS is supplied in these 14 lead outline packages:

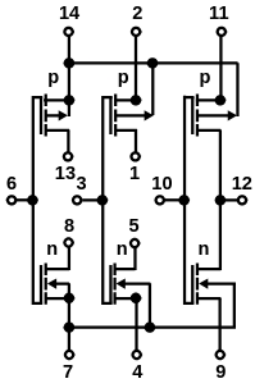
Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4007UBMS
TOP VIEW



Functional Diagram



TERMINAL NO. 14 - VDD

TERMINAL NO. 7 - VSS

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For T_A = -55°C to +100°C (Package Type D, F, K) 500mW
For T_A = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For T_A = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	0.5	µA
				2	+125°C	-	50	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	0.5	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND		7	+25°C			
		VDD = 18V, VIN = VDD or GND		8A	+125°C			
		VDD = 3V, VIN = VDD or GND		8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	-	1.0	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V		1, 2, 3	+25°C, +125°C, -55°C	4.0	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	-	2.5	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V		1, 2, 3	+25°C, +125°C, -55°C	12.5	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay	TPHL TPLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	110	ns
			10, 11	+125°C, -55°C	-	149	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. 55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.25	µA
				+125°C	-	7.5	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	15	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	0.5	µA
				+125°C	-	30	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	2	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	8	-	V
Propagation Delay	TPHL TPLH	VDD = 10V	1, 2, 3	+25°C	-	60	ns
		VDD = 15V	1, 2, 3	+25°C	-	50	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	15.0	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	2.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVPTH	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:
1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - SSI	IDD	±0.1µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Group D	Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 5, 8, 12, 13	3, 4, 6, 7, 9, 10	2, 11, 14			
Static Burn-In 2 Note 1	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14			
Dynamic Burn-In Note 1	-	4, 7, 9	2, 11, 14	1, 5, 8, 12, 13	3, 6, 10	-
Irradiation Note 2	1, 5, 8, 12, 13	4, 7, 9	2, 3, 6, 10, 11, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ±5%, VDD = 18V ±0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ±0.5V

Schematic Diagram

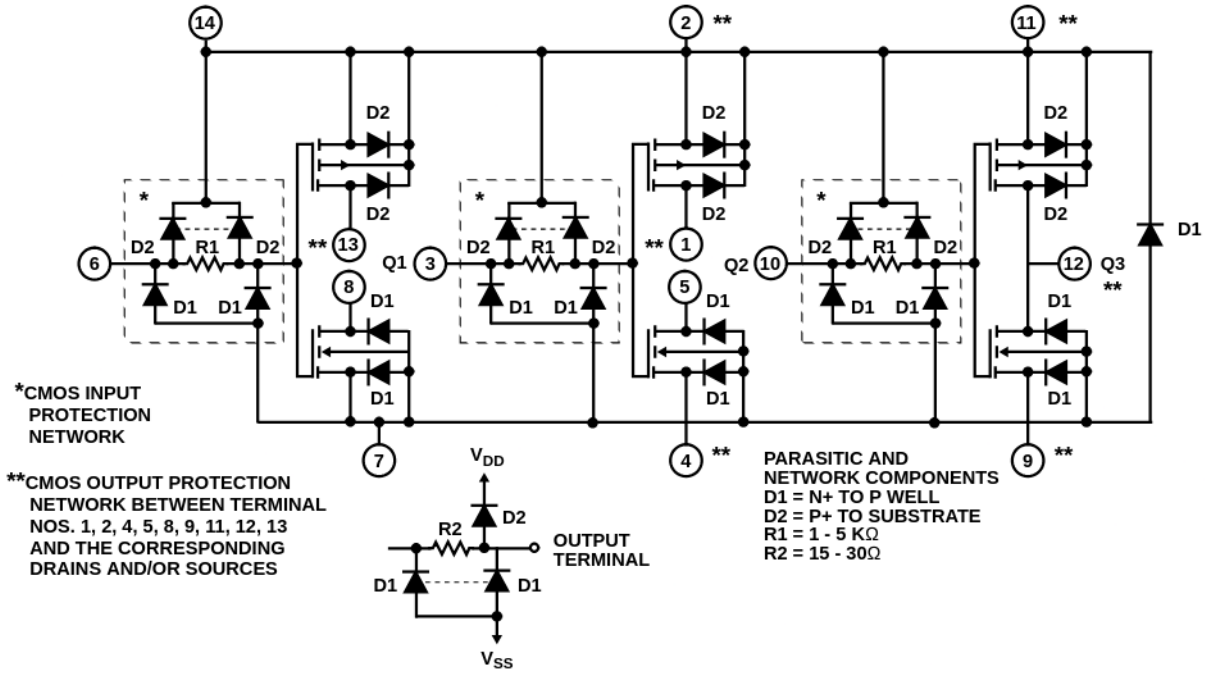
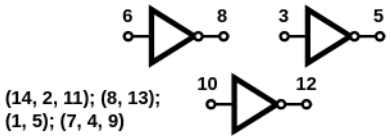


FIGURE 1. DETAILED SCHEMATIC DIAGRAM OF CD4007UBMS SHOWING INPUT, OUTPUT, AND PARASITIC DIODES

Logic Circuits



(14, 2, 11); (8, 13);
(1, 5); (7, 4, 9)

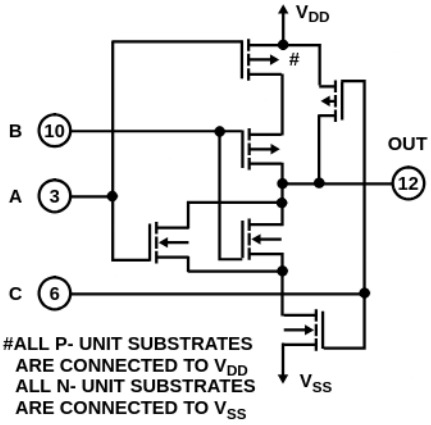
a) TRIPLE INVERTERS

(13, 2); (1, 11);
(12, 5, 8); (7, 4, 9)

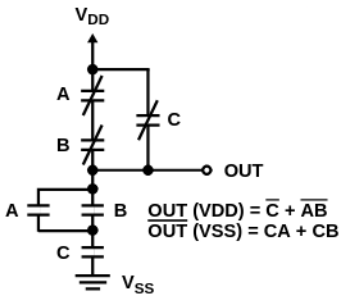
b) 3 - INPUT NOR GATE

(1, 12, 13); (2, 14, 11);
(4, 8); (5, 9)

c) 3 - INPUT NAND GATE



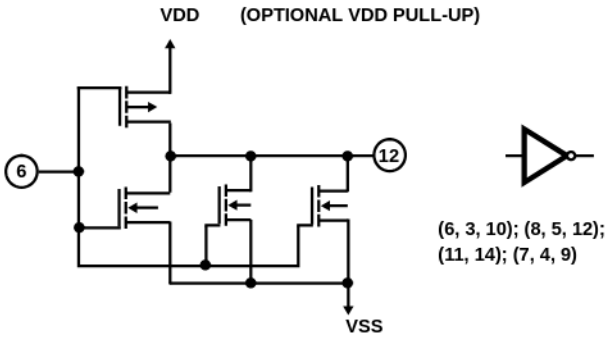
#ALL P- UNIT SUBSTRATES
ARE CONNECTED TO V_{DD}
ALL N- UNIT SUBSTRATES
ARE CONNECTED TO V_{SS}



$\overline{OUT}$ (VDD) = $\overline{C}$ + $\overline{AB}$
$\overline{OUT}$ (VSS) = CA + CB

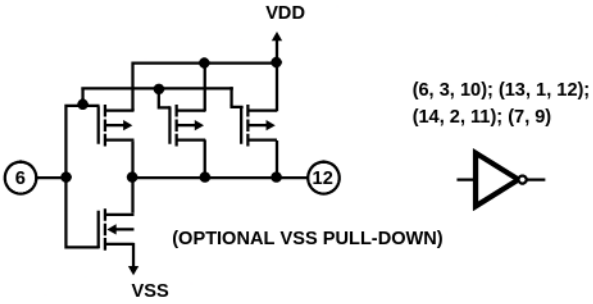
(13, 12, 5); (4, 9, 8);
(14, 2); (1, 11)

d) TREE (RELAY) LOGIC



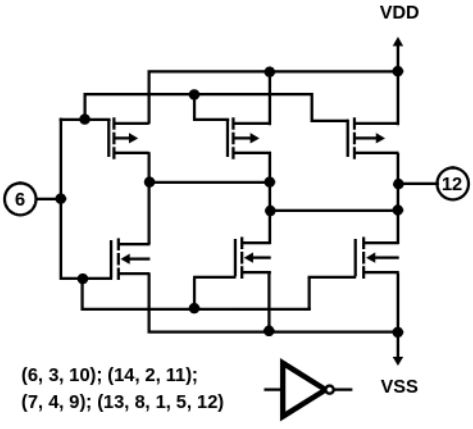
(6, 3, 10); (8, 5, 12);
(11, 14); (7, 4, 9)

e) HIGH SINK-CURRENT DRIVER



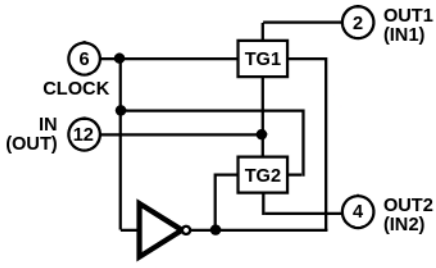
(6, 3, 10); (13, 1, 12);
(14, 2, 11); (7, 9)

f) HIGH SOURCE-CURRENT DRIVER



(6, 3, 10); (14, 2, 11);
(7, 4, 9); (13, 8, 1, 5, 12)

g) HIGH SINK - AND SOURCE-CURRENT DRIVER



(1, 5, 12); (2, 9);
(11, 4); (8, 13, 10);
(6, 3)

h) DUAL BI-DIRECTIONAL TRANSMISSION GATING

FIGURE 2. SAMPLE CMOS LOGIC CIRCUIT ARRANGEMENTS USING TYPE CD4007UBMS

Typical Performance Characteristics

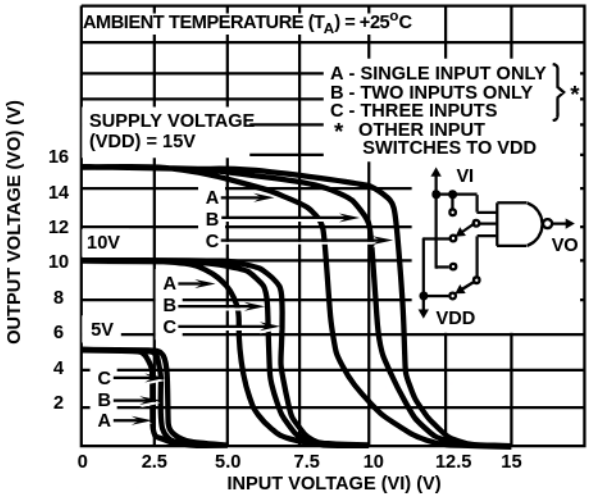


FIGURE 3. TYPICAL VOLTAGE-TRANSFER CHARACTERISTICS FOR NAND GATE

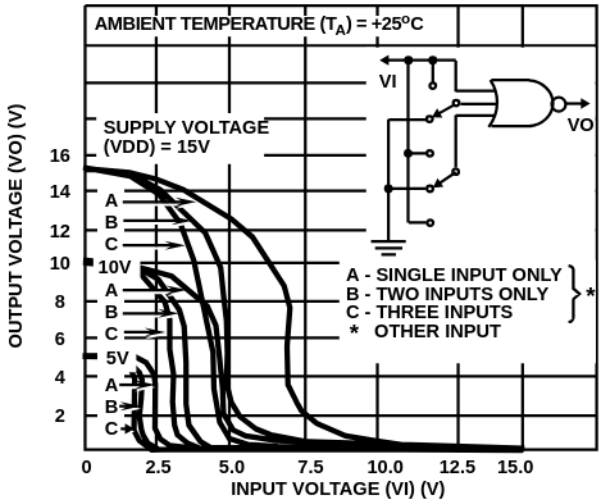


FIGURE 4. TYPICAL VOLTAGE-TRANSFER CHARACTERISTICS FOR NOR GATE

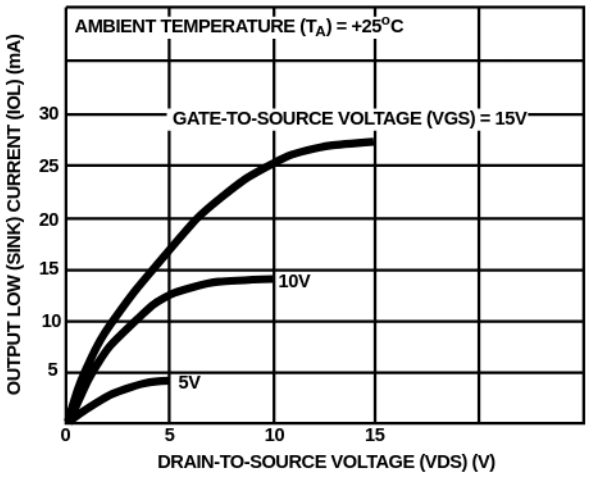


FIGURE 5. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

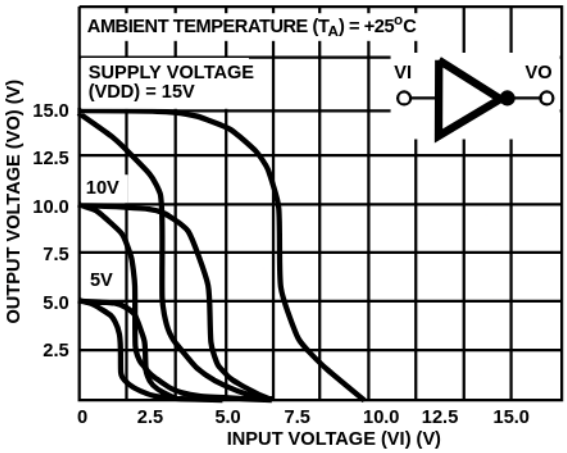


FIGURE 6. MINIMUM AND MAXIMUM VOLTAGE-TRANSFER CHARACTERISTICS FOR INVERTER

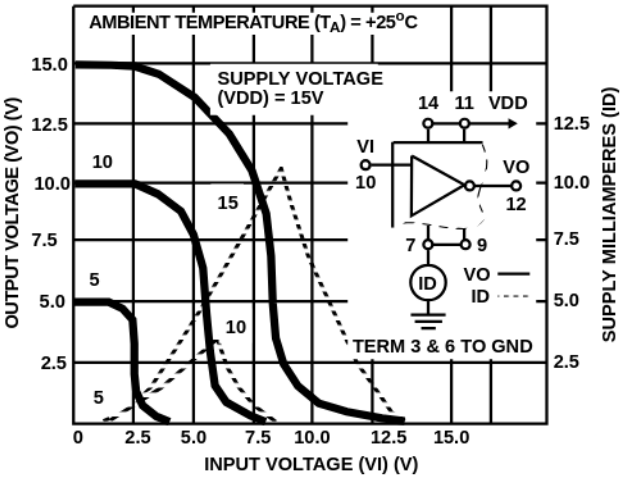


FIGURE 7. TYPICAL CURRENT AND VOLTAGE-TRANSFER CHARACTERISTICS FOR INVERTER

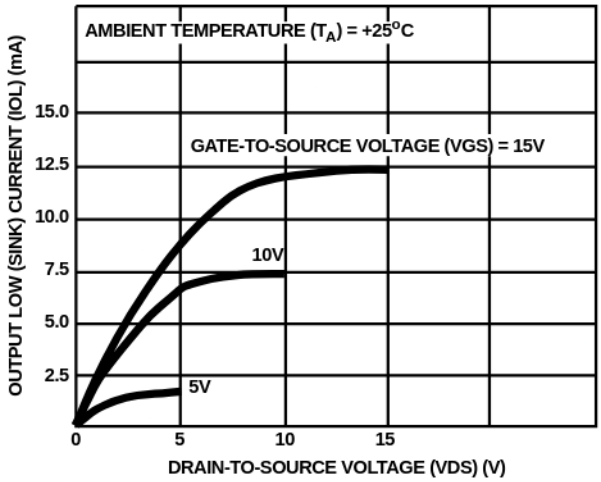


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

Typical Performance Characteristics (Continued)

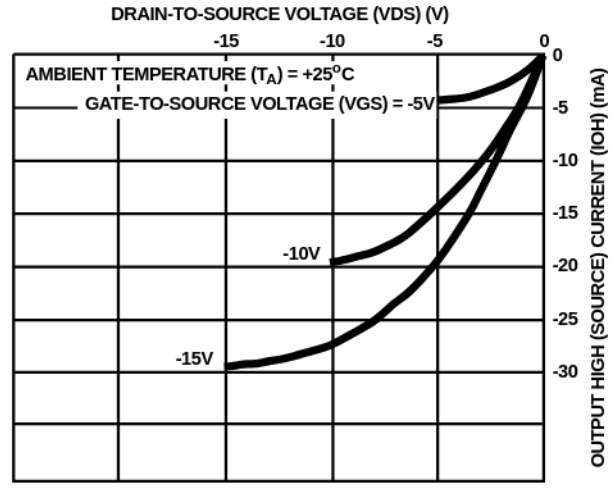


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

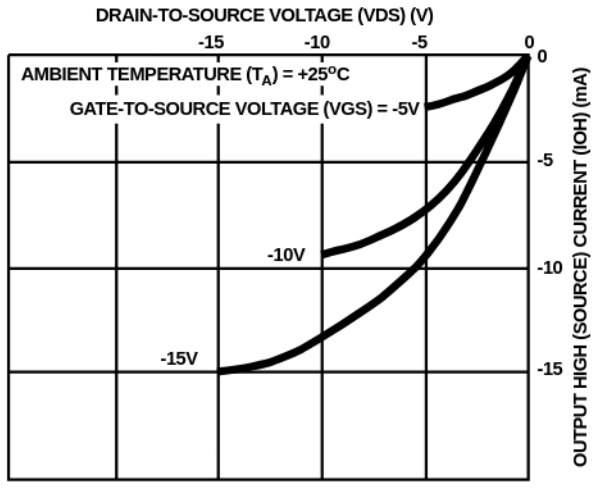


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

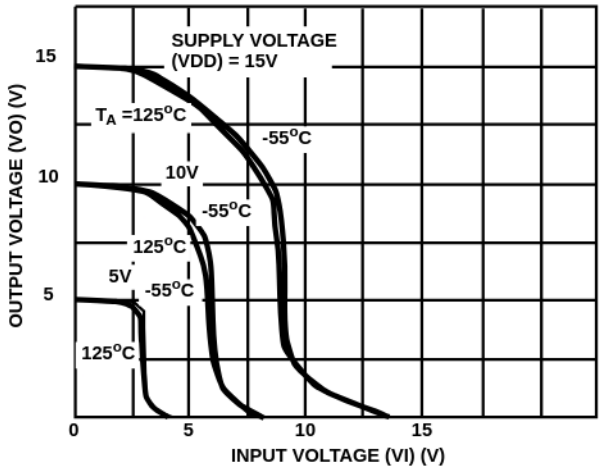


FIGURE 11. TYPICAL VOLTAGE-TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

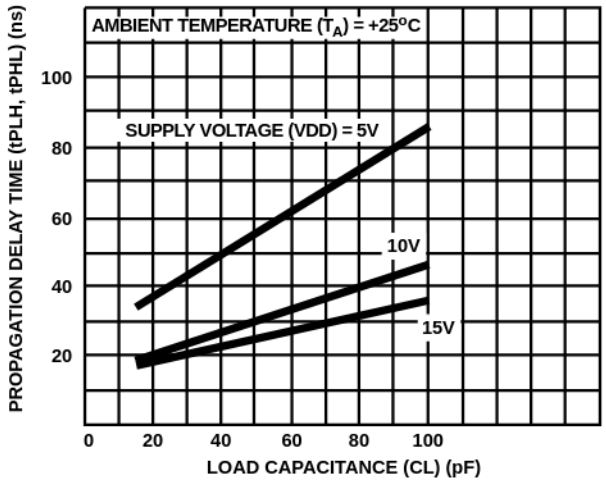


FIGURE 12. TYPICAL PROPAGATION DELAY TIME vs LOAD CAPACITANCE

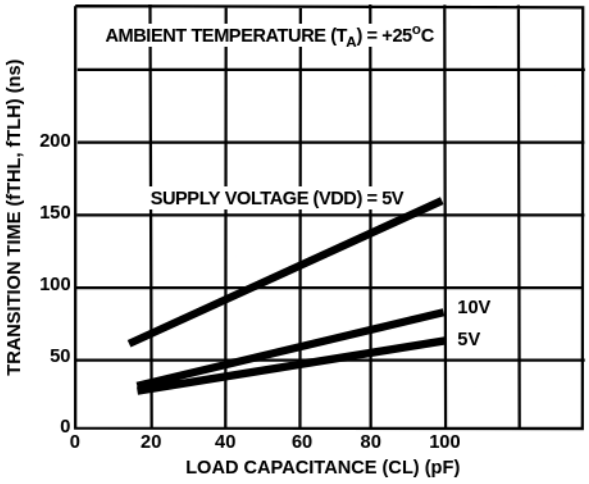


FIGURE 13. TYPICAL TRANSISTION TIME vs LOAD CAPACITANCE

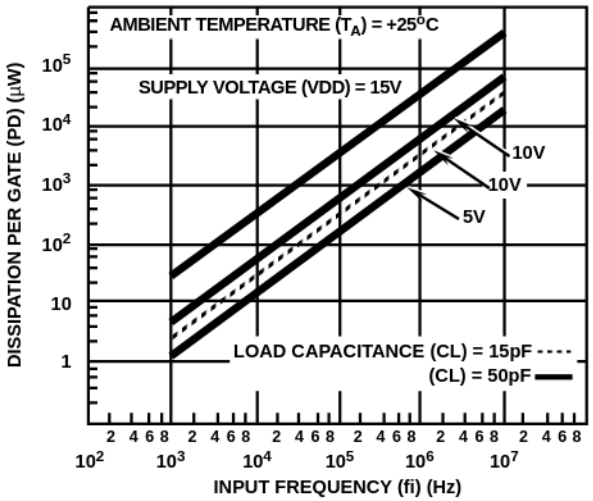
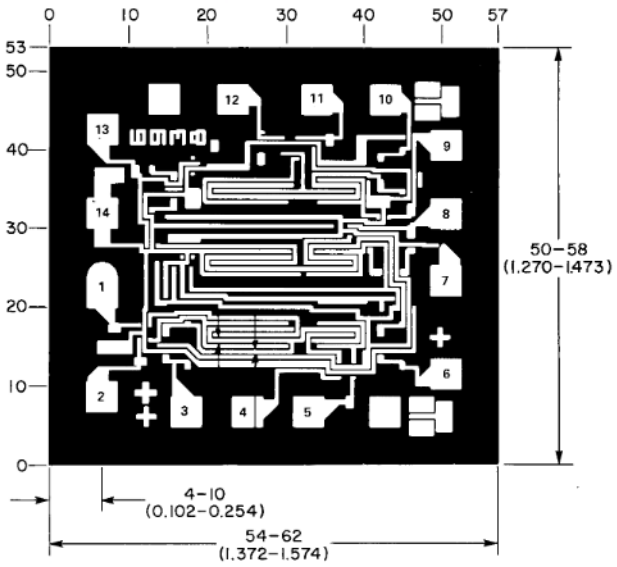


FIGURE 14. TYPICAL DISSIPATION vs FREQUENCY CHARACTERISTICS

Chip Dimension and Pad Layout



Dimensions in parentheses are in millimeters
and are derived from the basic inch dimensions
as indicated. Grid graduations are in mils (10^{-3} inch)

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

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