EXPERIMENT 3

BIPOLAR JUNCTION TRANSISTORS AND AMPLIFIERS

1. OBJECTIVES

- To conduct a DC analysis and compare the theoretical values with the values after the implementation of the circuit.
- To examine the performance of the Common Emitter BJT Single stage amplifier.

Laboratory dressing requirements: shoes must hold the ankle. It means no flip flops

2. THEORY – In order to appreciate how these circuits amplify an input, you should know the small-signal models for BJT.

The maximum rating and diagram for P2N2222A BJT is given below.

3. Pre-Lab:

a) Fill in the table below from the datasheet available online.

V_{CE}(V)	I_C(mA)	β max./typical	P_D(mW)	Freq.(MHz)

Table 1: Maximum Ratings of P2N2222A Bipolar Transistor

b) For a npn BJT, draw the hybrid-π small-signal model and define various parameters.
c) For a npn BJT, draw the small-signal T model. What are the applications of small-signal models?
d) Conduct the DC analysis for the circuit shown in figure 2. Assume $\beta = 100$, $V_{CE} = 7.5V$ and $V_B = 4.5V$. The fill out the calculated values in Table 2.
e) Assume $\beta = 100$, $\alpha = 0.99$ and $V_T = 25mV$ for the circuit shown in figure 3. Use a small signal model to analyze this circuit and calculate the voltage gain with and without the bypass capacitor. For this analysis ignore 10 μF capacitors and the biasing resistors. Also ignore the load resistor of 10 KΩ. Do you know why we make these simplifications? What is the role of biasing resistors?

4. EXPERIMENTAL PROCEDURE

The picture below shows the appearance of the BJT that you will find in the lab. The pins are described in the table below. It would be useful to mount the devices on the long-legged holders before you put together your circuit on the breadboard.

Pin No.	P2N2222A BJT	2N2222A BJT
1	Collector	Emitter
2	Base	Base
3	Emitter	Collector

Figure 1

Required components

NPN **Transistors**	**Resistors**	**Capacitors**
P2N2222A or 2N2222A	4.7, 10, 33,75 K**Ω**	10, 47 μF

4.1 DC MEASUREMENTS

The circuit shown in figure 2 is known as voltage splitter. Use the following values to locate the operating point in the active region, $V_{CE} = 7.5V$, $V_B = 4.5V$, $\beta = 100$. Choose $R_1 = 75k$, compute the value of R_2 ($\cong 33k$). Select the closest standard values for the resistors, and then construct the circuit shown in the figure 2. **Make sure you mount your BJT on the transistor-holder before you assemble your circuit on the breadboard**.

Use the DMM to measure all the DC values in the table below. Compute β and verify all the previous values.

V_{CE}	V_{BE}	V_B	I_C	I_E	I_B

Table-2

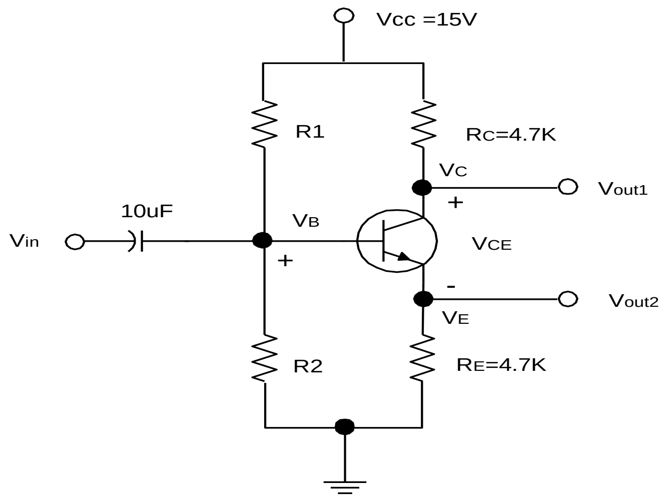

Figure 2

4.2 AC MEASUREMENTS for Common Emitter (CE) amplifier

4.2.1- Apply 4Vpeak-peak 1 kHz sine wave to the input v_{in} in Figure 2. Use channels 1& 2 of the oscilloscope to display first, v_{in} and v_{out1} and then, v_{in} and v_{out2}. Compute the gain v_{out1}/v_{in} and v_{out2}/v_{in}, record the phase shift between the input and the two outputs. The gains must be close to one. What is the phase shift due to?

4.2.2- Modify the connection of the circuit shown in figure 2 to obtain the circuit in figure 3. NOTICE that the capacitor of 47 μF is connected across the emitter resistor R_E, also a resistor is added between the signal generator and the coupling capacitor. If the circuit draws any current from the signal generator it must pass through the $10K\Omega$ resistor. The voltage across the $10K\Omega$ resistor is equal to $v_s - v_x$, and the current passing through is equal to $(v_s - v_x)/10K$. Looking at the direction indicated by the arrow, the input resistance of the amplifier can be computed from the equation below.

$$R_i = \left(\frac{v_x}{v_s - v_x}\right) * 10k$$

The amplifier bandwidth (operating frequency range) is defined as the difference in Hz between the upper and lower 3dB points. The 3dB point is known as the point where the amplifier gain falls below the mid-band gain by the factor $\frac{1}{\sqrt{2}}$ i.e. $G_{out} = \frac{G_{MID-BAND}}{\sqrt{2}}$. The following equation is used as a formal definition for the 3dB point.

$$-3dB = 10 * \log(\frac{G_{out}}{G_{MID-Band}}) = 20 * \log(\frac{1}{\sqrt{2}})$$

EXPERIMENTAL PROCEDURE

1- Apply a sinusoidal input signal with 100 mV peak-peak and 4 KHz.

2- Use the oscilloscope to measure the following peak-peak values: v_s, v_x and v_{out}. Be ready to adjust input amplitude if v_{out} saturates.

3- Display v_{in} on CH1 and v_{out} on CH2, then change the frequency (if needed) and measure the peak-to-peak value until the output reaches the maximum value. Record this result as v_{out} = $v_{MID\text{-}BAND}$. Now decrease the frequency more and observe the peak-peak values of the output signal v_{out}, when $v_{OUT} = \frac{v_{MID-BAND}}{\sqrt{2}}$ record the frequency of the input signal. This is the frequency at the lower 3dB point.

4- Set the input frequency to 50KHz. Slowly increase the frequency till the output peak-peak equal to $\frac{v_{MID-BAND}}{\sqrt{2}}$. Determine this frequency at the upper 3dB point. Determine the bandwidth.

5- From the above readings compute the following: input resistance (Ri), the gain (v_{out}/v_{in}), and the bandwidth of the CE amplifier.

6- Remove the 47μF capacitor from the circuit and obtain the maximum gain (v_{out}/v_{in}) and the bandwidth.

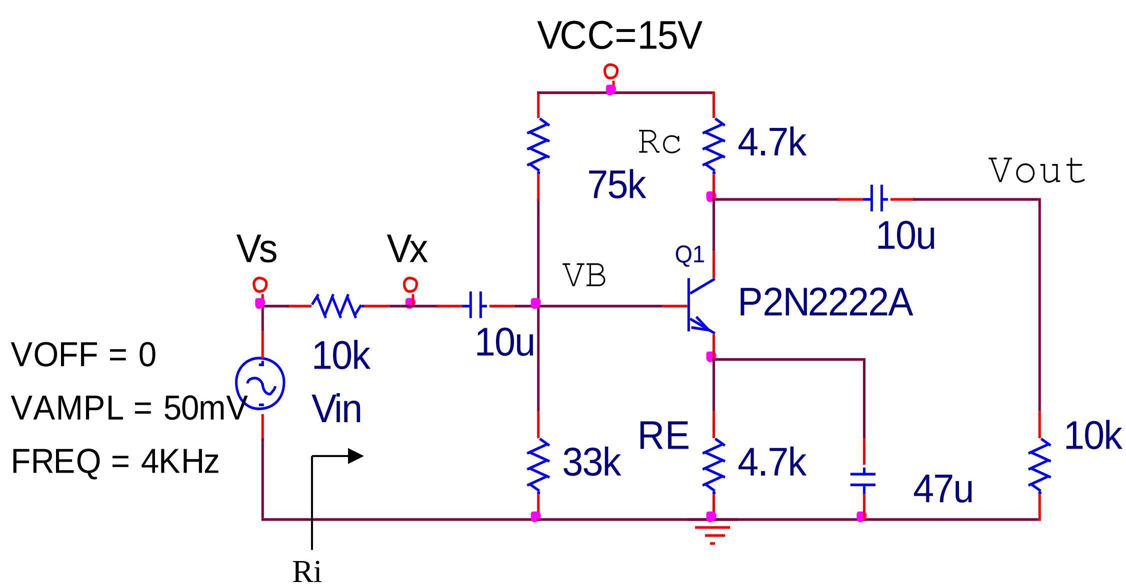

Figure 3

5. QUESTIONS AND DISCUSSION

1. Explain how the emitter resistance R_E stabilizes the Q point.

2. Which of the 3 capacitors in Fig. 3 is the bypass capacitor? What is its role? What is the role of other two 10 μF capacitors?

3. Using your DC measurement in section 4.1, calculate the power dissipation in the BJT.

4. If the small-signal model for BJT has been covered by your professor then using theoretical analysis, show that the presence of bypass capacitor in Fig 3 significantly enhances the gain in the mid-band region. In answering you may assume that the bypass capacitor creates a virtual ground at the capacitor. You may also ignore the coupling capacitors and the biasing resistors.